

20 Gb/s 1 2 Demultiplexer in 0.18 μ m CMOS*

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Abstract: A 1 2 demultiplexer is designed and realized in standard 0.18 μ m CMOS technology. A novel high-speed and low-voltage latch is used to realize the core circuit cell. Compared to the traditional source-coupled FET logic structure latch, its power supply voltage is lower and the speed is faster. In addition, the negative feedback is used in the buffer circuit to widen its bandwidth. Measurement results show that the chip can work at the data rate of 20Gb/s. The supply voltage is 1.8V and the current, including the buffer circuit, is 72mA.

Key words: demultiplexer; latch; CMOS; high-speed circuit

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1 Introduction

Giga-bit-per-second optical-fiber-link systems have become more important because of the increasing demand for high-speed communications. The demultiplexer (DEMUX) is a key component of the system. The integrated circuit (IC) must handle high-frequency signals whose frequency bands are at least half of the data rate. Fast switching speed is therefore necessary.

Usually, a DEMUX with an operating speed greater than 10Gb/s is realized in GaAs MESFETs, GaAs HBTs, Si bipolar transistors, SiGe bipolar transistors, or Si BiCMOS^[1-3]. The power consumption of these ICs, however, is relatively large because their supply voltage is high and their penetration current is large.

CMOS technologies have the advantages of low power consumption and low cost. Traditionally, it has rarely been used in such high-speed systems because the transistor's operation speed is

too low. However, using a modern deep submicron CMOS technology, the switching speed of CMOS transistor is high enough to realize ultra-high speed DEMUX. A low-power 0.18 μ m CMOS realization of 10Gb/s MUX/DEMUX has already been reported^[4]. It consumed only 102mW from a 2V power supply, which is at least 75% less than that of the designs using GaAs MESFET, InP-base HBT, or SiGe technology. However, the design can only realize the MUX/DEMUX at 10Gb/s. In this paper, we presented a CMOS 20Gb/s 1 2 DEMUX based on a novel high-speed and low-voltage latch and implemented using the standard 0.18 μ m CMOS process. The proposed DEMUX operates with a 1.8V power supply.

2 Circuit design

The whole circuit employs the input buffer, output buffer, and 1 2 DEMUX cell as shown in Fig. 1. In this architecture, the input data and clock signal are first amplified through each input buff-

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er ,and then they enter the DEMUX cell. Each output data of the DEMUX cell is also amplified through an output buffer. In order to reject the common mode noise and interferences ,all input and output signals are in differential mode.

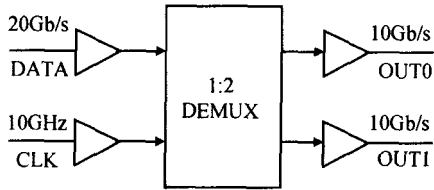


Fig. 1 Circuit diagram of the DEMUX

Figure 2 shows the architecture diagram of the 1 2 DEMUX cell. It consists of a master-slave-master flip-flop to capture the lead bit on the positive-edge of the clock and a master-slave flip-flop to capture the second bit using the negative-edge of the clock. The advantages of this architecture are as follows :

- (1) The output signals are synchronous with each other ,not needing an additional flip-flop ;
- (2) The clock frequency is half of the input data rate ,which degrades the design difficulty.

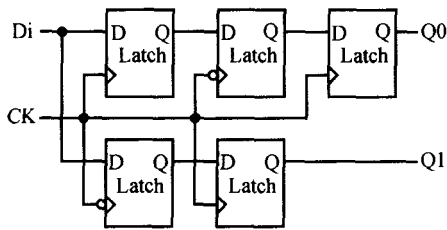


Fig. 2 Block diagram of 1 2 DEMUX

Figure 3 shows the 1 2 DEMUX 's timing chart. To obtain the maximum timing margin ,the signals should be aligned at the center of the data pulse. This can be realized by delaying the clock signal to the proper position according to the data signal.

The circuit topology of the latch is very important to the whole circuit. It affects not only the circuit speed but also the power dissipation. In this paper ,a novel low-voltage and high-speed latch is used in the DEMUX cell as shown in Fig. 4. This latch ,consisting of a differential pair and a regener-

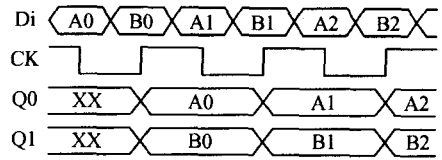


Fig. 3 1 2 DEMUX timing chart

ative pair ,achieves high speed in CMOS technologies. It results from the traditional MCML latch^[5,6] by moving the transistors which are controlled by the clock signals to the top. In the traditional latch ,the transistor working as the current source is stacked under the source-coupled pair transistors. To ensure the transistor operating correctly ,the supply voltage must be high enough for the three-level transistor structure. So ,to realize low-voltage latch ,series-gate should be avoided ,as in topology based on triple-tail cells in Fig. 4. The pair M1 ,M2 and M3 ,M4 realize two differential stages that are alternatively activated by turning off M5 and M6 ,respectively. When signal CK is high ,transistor M6 deactivates differential pair M3 ,M4 ,hence the output is equal to the input (i. e. the latch is transparent) . When the signal CK is low (i. e. signal / CK is high) ,transistor M5 deactivates the differential pair M1 ,M2 ,and the output voltage is set by cross-coupled transistors M3 ,M4 , that hold the previous result (i. e. latch is in the hold mode) . In order to increase the circuit speed ,the source follower is omitted compared to the traditional structure. This may result in the latch to degrade the ability of driving load. Thus ,the output buffer should be designed carefully.

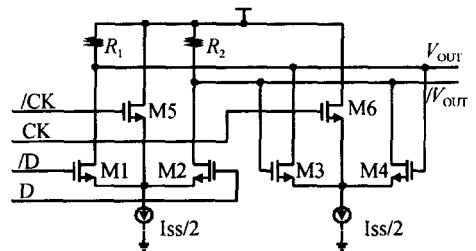


Fig. 4 Low voltage latch

As we know ,the charge/ discharge time of the output node is decided by the following formula :

$$T = \frac{CV_a}{I_c}$$

where C is the total capacitor of the output node, V_a is the amplitude of output signal, and I_c is the charge/discharge current. To increase the speed of the latch, C and V_a should be decreased, whereas I_c should be increased. However, V_a can not be too small and I_c can not be too large, because extra current leads to power consumption increment, and enough voltage swing is necessary to drive the load. So there is a trade-off among the W/L of transistors $M1 \sim M4$, the tail current, and the load resistors R_1, R_2 . In order to operate effectively, the size of clock pair ($M5, M6$) should be much larger than that of the sample and hold pair ($M1 \sim M4$).

Both data and clock inputs and outputs are terminated by on chip poly-silicon resistors. These resistors supply a 50 Ω impedance match to avoid reflection. The input buffer has been designed to amplify the input signal to the needed amplitude. The output parallel data must be buffered in order to drive the external 50 Ω load. As we have mentioned, a latch without a source follower can not drive a heavy load. So the buffer should be designed in multiple stages and the differential pair transistors' size of the first stage should be small. In the following stages, the differential pair transistors' ratio of W/L could be increased step by step. In this design, the three-stage differential amplifier structure has been introduced. Due to the large capacitance of the pads, the output signals become worse. In order to achieve a better eye diagram, the negative feedback is used by connecting a pair of resistors between the input terminals and the output terminals in the last stage amplifier.

3 Layout and fabrication

The DEMUX circuit was designed using one-poly six-metal standard 0.18 μ m CMOS technology and fabricated by Taiwan Semiconductor Manufacturing Co., Ltd. Figure 5 shows the micrograph of the chip. The chip area including bonding pads is

1mm \times 0.9mm. In fact, only 4% of the total chip area in the middle region is used for the active part.

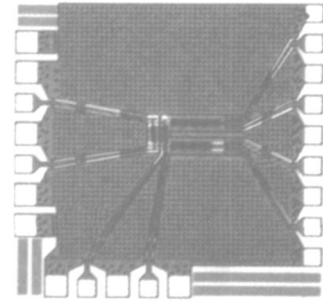


Fig.5 Chip micrograph of the 1 2 DEMUX

Because the circuit operates up to 20 Gb/s, the layout should be carefully designed. In this circuit, the following methods are used to enhance the performance. As the circuit is differential, a symmetrical layout of the differential signal path is diligently respected to suppress the common mode noise and stabilize the high frequency ground. Minimum interconnections are preferred for the signal lines especially during the key nodes, such as the drain of the differential pair transistors. In order to filter the noise of the power supply, the parasitic capacitance between supply and ground should be as large as possible. This can be realized by enlarging the overlap area of supply plane and ground plane during layout.

4 Measurement results

The performance of the fabricated DEMUX was evaluated via an on wafer test employing a Cascade Microtech probe station, an ADVENTEST D3186 Pulse Pattern Generator, an Agilent 81250 Parallel BER Tester, an ADVENTEST R6142 Programmable DC Voltage/Current Generator, a Rohde & Schwarz SMP04 Signal Generator (10MHz \sim 40GHz) and an Agilent 86100A Infinium DCA wide-bandwidth oscilloscope. The measurement diagram is shown in Fig. 6, in which both the D3186 and the 81250 are referred to the clock generated by the SMP04, then the D3186 can provide the dif-

ferential clock signal and the 81250 can provide the differential data signal.

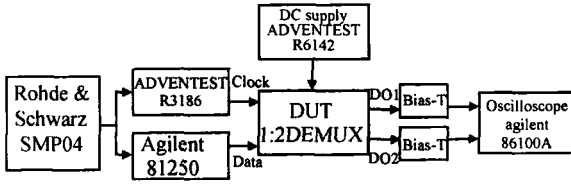


Fig. 6 Measurement diagram

Under the 1.8V DC supply voltage, a current of 72mA was measured from the whole circuit. The 20Gb/s differential input data pseudorandom bit sequences (PRBS of $2^{31} - 1$) were obtained from the 81250. The 10GHz input clock signals provided by the D3186 were also differential. The output data of the DEMUX was analyzed by the Agilent 86100A oscilloscope. In order to realize the AC coupled connection, several Bias-Ts were used. Figure 7 shows the measured eye diagram of the DEMUX output signal at the data rate of 10Gb/s. The measured eye opening is more than 100mV on the external 50 load. The double traces in the eye are due to the limited bandwidth of the output buffer. Since the rate of the output data signal from 81250 can not be adjusted continuously, this measurement scheme, with these instruments, cannot test the circuit working in limited conditions. That is, this DEMUX circuit may operate at a data rate more than 20Gb/s.

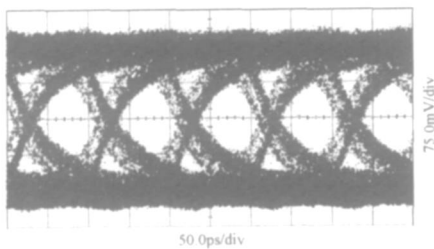


Fig. 7 Output eye diagram at 20Gb/s input

In fact, we can estimate the maximum operation speed of this circuit by the following method. Figure 8 shows the output eye diagram of this DEMUX working at 10Gb/s input. According to this figure, the rise time and fall time from 10% to 90% of the peak-to-peak voltage are 72 and 75ps respectively.

Thus the total time of rise and fall time is

$$T_t = (t_r + t_f) / 0.8 = (72 + 75) / 0.8 = 183.75(\text{ps})$$

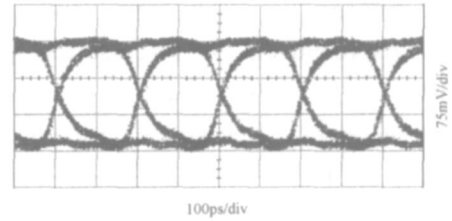


Fig. 8 Output eye diagram at 10Gb/s input

In the limited condition, this time equals to 2bit period, hence the maximum output data rate is

$$R_{\text{max}} = 2 / T_t = 2 / 183.75$$

$$0.01088(\text{Tb/s}) = 10.88(\text{Gb/s})$$

From this, the maximum input data rate of the 1:2 DEMUX is $2R_{\text{max}}$, that is 21.76Gb/s.

5 Conclusion

A 1:2 demultiplexer has been designed and fabricated using the TSMC standard 0.18μm CMOS technology. Under a 1.8V supply, this DEMUX can work at the data rate of 20Gb/s. The whole circuit consumes a power dissipation of 129mW and has an active size of 245μm × 150μm. These results show that a novel latch can be used in ultra high-speed circuit by using a deep submicron CMOS process.

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0.18 μ m CMOS 20 Gb/s 1/2 分接器设计*

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摘要: 使用标准 0.18 μ m CMOS 工艺设计并实现了 1/2 分接器. 核心电路单元采用一种新的高速、低电压锁存器结构实现. 与传统的源极耦合场效应管逻辑结构的锁存器相比, 其电源电压更低且速度更快. 此外, 为了拓展带宽, 在缓冲放大电路中采用了负反馈. 测试结果表明芯片可以工作于 20 Gb/s 数据速率下. 电源电压为 1.8V 时, 包括缓冲电路在内整个芯片的工作电流为 72mA.

关键词: 分接器; 锁存器; CMOS; 高速电路

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