Improved Breakdown Voltage of Partially Depleted SOI nMOSFETs with Half-Back-Channel Implantation

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Abstract: FB (floating-body) and BC (body-contact) partially depleted SOI nMOSFETs with HBC(half-back-channel) implantation are fabricated. Test results show that such devices have good performance in delaying the occurrence of the "kink" phenomenon and improving the breakdown voltage as compared to conventional PDSOI nMOSFETs, while not decreasing the threshold voltage of the back gate obviously. Numerical simulation shows that a reduced electrical field in the drain contributes to the improvement of the breakdown voltage and a delay of the "kink" effect. A detailed analysis is given for the cause of such improvement of breakdown voltage and the delay of the "kink" effect.

Key words: PDSOI; HBC; breakdown; kink effect
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1 Introduction

SOI technology is believed by some to be the most promising CMOS technology of the 21st century. Recent research on SOI devices has shown that they have great potential in high-speed, low-power, and low-voltage applications[1]. SOI can be divided into FD (fully depleted) SOI and PD (partially depleted) SOI according to top silicon film thickness and doping concentration in the silicon film. Due to good feasibility in the fabrication of PDSOI devices, PDSOI has received extensive attention from the industry. The existence of a neutral area in the body of the devices, especially nMOSFETs induces a series of unwanted floating effects like the parasitic bipolar effect and the single transistor latch[2]. In some circuits that require high reliability, people have to adopt some methods to reduce or eliminate floating effects induced by this neutral area. Till now, many methods have been proposed to suppress the floating effects. The most direct way is to add a contact to the body area and set this contact to a fixed voltage value (for nMOSFET, Gnd), which can elicit redundant holes (for nMOSFET) from the body area.

For PDSOI CMOS devices, including FB (floating body) ones and BC (body contact) ones, which can be used in practical circuit applications, suppressing back channel conducting is very important for improving the reliability of the circuits[3]. Generally, adding enough doping concentration in the back channel, by implanting large amount dose of impurity into the area of the back channel, is a useful way. However, such a dose of impurity would lead to other undesirable issues of reliability like a lowered breakdown voltage, especially for nMOSFETs.

In this paper, we introduce a new way to improve the breakdown voltage of FB &BC PDSOI devices. This new way is to implant impurities into half of the back channel while performing back channel doping. This method needs an extra mask to control the area of the back channel. Measure-

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ment results show that such a method can effectively delay the occurrence of the "kink" phenomenon and improve the breakdown voltage. Numerical simulation of the process and device shows that lowering channel doping concentration near the drain area leads to a reduced lateral electrical field in the drain and a reduced impact ionization, which improves the breakdown characteristics.

2 Device fabrication

PDSOI nMOSFETs with the gate length of 2μm on the SIMOX substrate were fabricated with a 400nm thick Si active layer, a 370nm thick buried oxide (BOX) and a p-type substrate. Figure 1 shows the layouts of four kinds of devices used in our experiments. In device fabrication, the devices were isolated with LOCOS (local oxidation of silicon) technology. Certain doses of BF_2^+ ion were implanted into the front channel. In back channel implantation with B^+ ion, the additional piece of mask (as shown in the shadow of Figs. 1(b) & (d)) was used in order to control the implantation area. A 20nm gate oxide was grown thermally before the deposition of the n^+ poly-gate. p^+ ion was implanted to form the source and the drain after the formation of the extension of the source and the drain. In order to activate the impurities implanted in the silicon film, a rapid thermal processing (RTP) at 1000 ℃ was performed for 4s. After the salicidation, devices were metalized using a typical backend flow. Figure 2 shows the simulated mesh structure in the channel part of the devices.

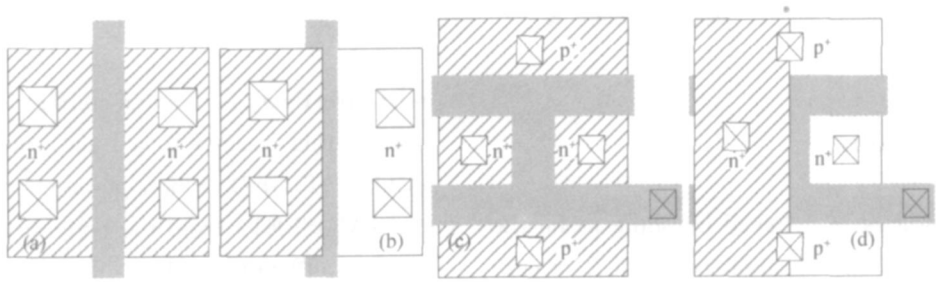

Fig. 1 Layouts of the devices (shades shows the area that should be implanted in back channel) (a) CON (conventional) FB nMOSFET; (b) HBC (half-back-channel) FB nMOSFET; (c) CON H-gate BC nMOSFET; (d) HBC H-gate BC nMOSFET

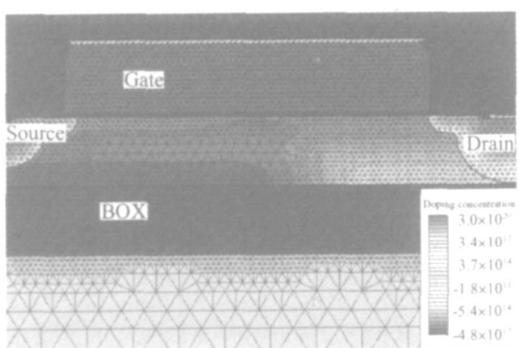

Fig. 2 Mesh structure in the channel

3 Results and discussion

3.1 Testing results

After the formation of the devices, we measured the characteristics of the devices using the Keithley 4200SCS semiconductor characteristics system. In our measurement, the source and the body (for BC devices) terminals were always grounded. Figure 3 shows the breakdown characteristics of four kinds of devices. From the figure, we can see that the breakdown voltage of conventional FB devices is the lowest (BV_{ds} = 5.5V), while the voltage in half-back-channel FB devices (BV_{ds} = 9.4V) is bigger; the break down voltage in conventional BC devices (BV_{ds} = 9.5V) is smaller than the voltage in HBC H-gate devices (BV_{ds} = 13V). This result shows that such HBC devices are more reliable for circuits which need supply voltage of 5V than conventional devices.

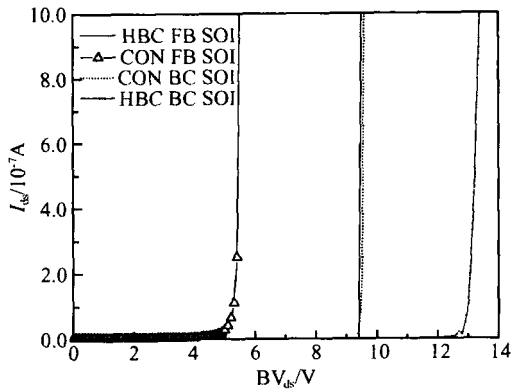

Fig. 3　Off-state breakdown characteristics of four kinds of devices

Figure 4 shows the output characteristics of four kinds of devices and the "kink" onset point extracted from the output characteristics. For HBC devices, even if under the V_{ds} = 8V, the devices still show the good characteristics, while for conventional devices, the curves show obvious sharp rising when V_{ds} > 6V. Unlike conventional FB nMOSFETs, we notice that the kink effect is not obvious under a high gate voltage for HBC FB SOI nMOSFETs. This shows that the impact ionization in HBC devices is weaker than in conventional devices in high V_{gs}. For H-gate devices, the characteristics are attractive not only because that they have good performance under high drain bias, but they also show larger overdrive ability than the conventional H-gate current (considering the different V_{th} between the HBC devices and CON devices, we compare the I_{ds}-V_{ds} curves by the parameter V_{gs}-V_{th}, not V_{gs}). For BC SOI nMOSFETs, we notice that the kink phenomenon occurs before the drain current increases suddenly. This demonstrates that strong impact ionization in a weak avalanche area causes the rapid generation of many holes. Due to the rapid generation of holes in the impact ionization and enlarged body resistance as the drain voltage increases, the generated holes accumulate in the body area and the body contact cannot elicit those holes timely. Thus the threshold voltage decreases and the saturation current suddenly increases. This causes the onset of a local parasitic bipolar transistor (far away from body contact) and further amplifies the impact ionization. At last, the breakdown phenomenon occurs.

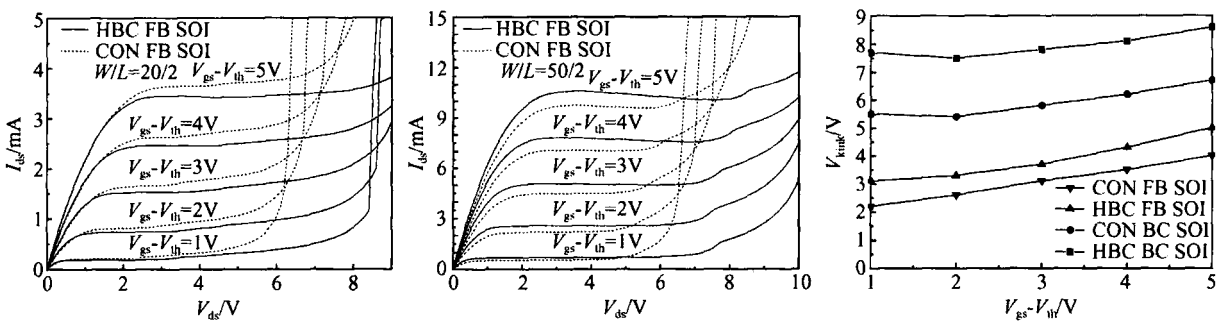

Fig. 4　Output characteristics of four kinds of devices and the onset point of the "kink" extracted from the output characteristics

Figure 5 shows the subthreshold characteristics of the back gate at V_{ds} = 0. 1V and V_{ds} = 5. 0V, respectively. Here, V_{ss} refers to the bias from the substrate (back gate) to the source of the devices. Although the back channel is half implanted, the threshold voltage of the back channel is basically the same as the devices with full implantation in the back channel. This demonstrates that although the back channel for HBC devices is only implanted in half the area, the conduction of the back channel still needs all parts of the back channel to invert and thus the threshold voltage of the back channel for HBC devices does not decrease obviously.

3.2　Discussion

To analyze the cause of this improved reliabili-

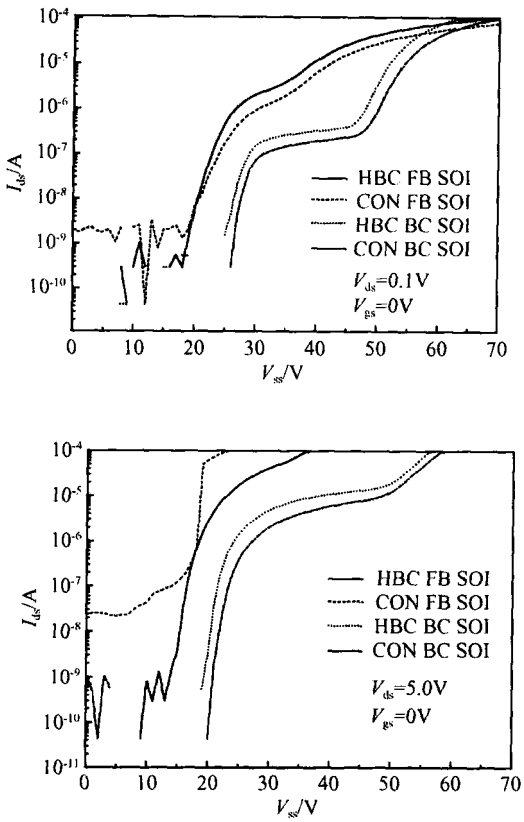

Fig. 5 Subthreshold characteristics of back gate of four kinds of devices

lectrical field around the middle of the channel, which is caused by the grades of doping concentration in the middle of the channel and such phenomenon is similar with DMG SOI devices[4]. From the figure, we can see that the peak electrical field near the drain (the place where the breakdown occurs) drops dramatically for HBC nMOSFETs as compared to CON nMOSFETs. The reduced electrical field near the drain reduces the impact ionization[5]. This means less holes will be generated in the neutral area of the body. Figure 6 plots electrostatic potential Ψ along the channel near the buried oxide. From the figure, we can see that the electrostatic potential of the HBC nMOSFETs in the channel is still lower than that of the CON nMOSFETs. This means more drain voltage is needed for HBC nMOSFETs to improve the body potential and cause the onset of the parasitic bipolar transistor, thus reducing the possibility of amplifying the bipolar transistor. There are two factors that contribute to such a situation. One is just reduced impact ionization for HBC devices. The other is that the length of low potential of the channel is

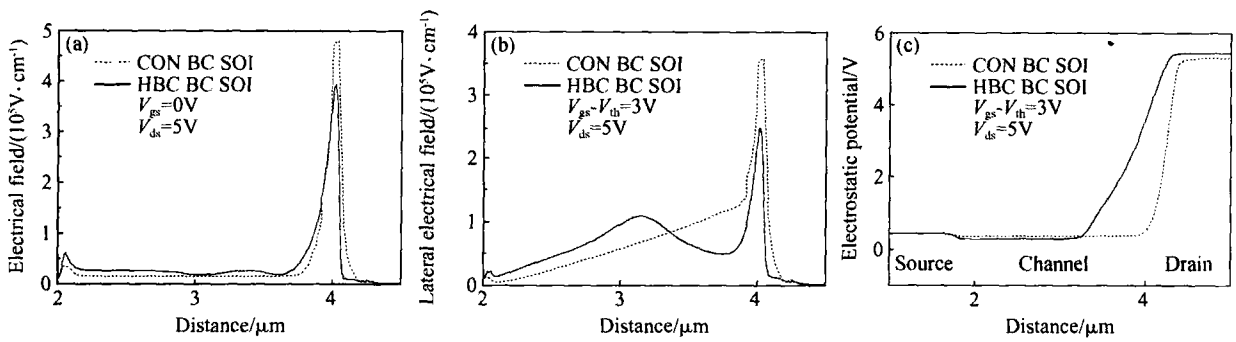

Fig. 6 Distribution of the lateral electrical field along the surface of the channel for V_{gs} = 0V (a) and V_{gs} - V_{th} = 3V (b); (c) Electrostatic potential along the back surface of the channel

ty, we performed a numerical simulation of the process and device. All the conditions in the process simulation were the same as the conditions in our fabrication process. Figure 6 shows the lateral electrical field near the surface of the silicon film along the channel for FBSOI nMOSFETs at V_{ds} = 5V, V_{gs} = 0V, and V_{gs} - V_{th} = 3V, respectively. It should be noticed that there is a second peak e-

longer for CON FBSOI devices than for HBC FBSOI devices and this means that the area of the neutral part in the channel is larger for CON devices. For the same concentration of the holes, the holes will go to large parts of the channel for HBC devices while the holes will only go to the nearly half of the channel for HBC FBSOI devices. This increases possibility for holes to diffuse into the

source in HBC FBSOI devices because of the increased grads of the hole concentration between the body and the source. It should be noticed that many holes accumulated in the reduced neural area will help improve its potential and help the onset of the parasitic bipolar transistor. So, the lowered body potential is the synthetic result of two factors. In addition, due to the reduced channel concentration, the current gain β of the bipolar transistor will be improved. The value of β extracted from the simulation has shown the slight increase ($\beta_{HBC} = 0.783 > \beta_{CON} = 0.749$) (refer to Ref. [6] for the extraction method). This shows that the reduced impact ionization is the predominant factor that determined the improvement of the breakdown characteristics in our experiment.

For BC SOI nMOSFETs, we have previously discussed the off-state breakdown characteristics in Ref. [7]. Now, we will discuss the on-regime characteristics. Because we perform a 2D numerical simulation while the practical devices are a 3D structure, there should exist some dissimilarity for simulated characteristics and practical ones, so we will only discuss this issue qualitatively. Like FB SOI devices, the reduced electrical field near the drain in HBC BC SOI devices is the fundamental reason that causes the improvement of the reliability of the devices. Figure 7 shows the simulated lateral electrical field near the surface of the silicon film along the channel at $V_{ds} = 5V$ and $V_{gs} - V_{th} = 3V$. In this figure, the plot is similar with FB SOI devices and the second peak electrical field can also be observed.

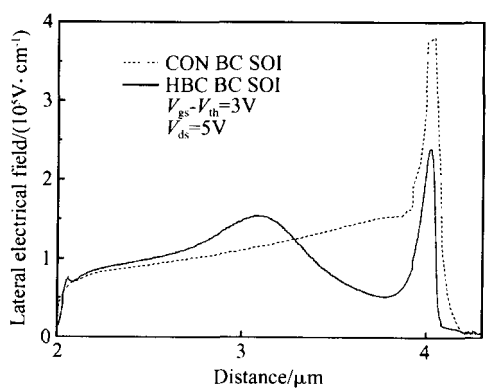

Fig. 7　Distribution of the lateral electrical field along the surface of the channel at $V_{ds} = 5V$

4　Conclusion

Our experiments show that the FB &BC PDSOI nMOSFETs with half-back-channel implantation has good performance in delaying the occurrence of the "kink" phenomenon, improving the breakdown voltage over conventional PDSOI nMOSFETs. In addition, this method does not decrease the threshold voltage of the back channel obviously. The numerical simulation shows that the reduced electrical field in the channel contributes to such improvements.

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采用半背沟注入提高部分耗尽 SOI nMOSFETs 的漏源击穿电压

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摘要: 制备了采用半背沟注入的浮体和体接触部分耗尽 SOI nMOSFETs. 测试结果表明这样的器件相对于传统的部分耗尽 SOI nMOSFETs 来说,在提高击穿电压和延缓翘曲现象发生方面有良好的表现,并且背栅阈值电压没有太大的变化. 数值模拟表明降低的电场有助于击穿特性的提高和翘曲现象的延缓. 详细分析了提高击穿特性和延缓翘曲效应的原因.

关键词: 部分耗尽 SOI; 半背沟道; 击穿; 翘曲效应

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