A DBRTD with a High PVCR and a Peak Current Density at Room Temperature *

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Abstract: AlAs/GaAs/$In_{0.1}Ga_{0.9}As$/GaAs/AlAs double-barrier resonant tunneling diodes (DBRTDs) grown on a semi-insulated GaAs substrate with molecular beam epitaxy is demonstrated. By sandwiching the $In_{0.1}Ga_{0.9}As$ layer between GaAs layers, potential wells beside the two sides of barrier are deepened, resulting in an increase of the peak-to-valley current ratio (PVCR) and a peak current density. A special shape of collector is designed in order to reduce contact resistance and non-uniformity of the current; as a result the total current density in the device is increased. The use of thin barriers is also helpful for the improvement of the PVCR and the peak current density in DBRTDs. The devices exhibit a maximum PVCR of 13.98 and a peak current density of 89kA/cm^2 at room temperature.

Key words: resonant tunneling diode; peak-to-valley current ratio; peak current density

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1 Introduction

Double barrier resonant tunneling diodes (DBRTDs) have received great attentions for their potential applications in frequency multiplication, microwave oscillation, analog-to-digital conversion, and static random access memory[1~4] because of their negative differential resistance (NDR) performance. To incorporate the DBRTD in the practical circuit, a high peak-to-valley current ratio (PVCR) larger than 5 and a high peak current density near to 10^5A/cm^2 are required.

Since Tsu and Esaki[5], and Chang *et al.*[6] first proposed and demonstrated NDR through DBRTDs, many efforts have been made to improve the performances of DBRTDs. Soderstrom *et al.*[7] fabricated InAs/AlSb DBRTD on a semi-insulated (SI) GaAs substrate with a PVCR of 11 and a peak current density of 4.3kA/cm^2 at room temperature. A pseudomorphic $In_{0.53}Ga_{0.47}As$/AlAs/InAs DBRTD on SI InP substrate with a PVCR of 50 and a peak current density of 5.8kA/cm^2 at room temperature has also been reported[8].

The option and preparation of different materials and structures are crucial to the performance of DBRTDs. Low electron effective mass in material and high conduction-band offset (ΔE_C) between barrier and well can improve the PVCR in DBRTDs resulting from reduction of the valley current. Due to lower electron effective mass, properties of InP-substrate RTDs are generally better than those of GaAs-substrate ones, and some novel materials of barrier and well have also been adopted[9] so as to obtain the same aims. However, consequent difficulty in MBE growth of new materials, and high fragility of InP resulting in rigorous process, baffle them into real application.

In this paper, in order to deepen the wells beside the two sides of the barrier, sub-well lays are

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used through the introduction of an $In_{0.1}Ga_{0.9}As$ layer between GaAs layers. Due to the reduction of the non-tunneling current, a high PVCR is obtained. Thin barriers and a special shape of collector are used for enlargement of the peak current density and the total current density, respectively. Device performance with a maximum PVCR of 13.98 and a peak current density of 89kA/cm^2 are demonstrated at room temperature successfully.

2 Material structure and device fabrication

The AlAs/GaAs/$In_{0.1}Ga_{0.9}As$/GaAs/AlAs DBRTDs are grown on SI GaAs (100) substrate by using JEN-Ⅱ molecular beam epitaxy (MBE) equipment. The growth sequence begins with four step-graded n^+-GaAs buffer layers, followed by an undoped GaAs spacer layer, an undoped $In_{0.1}Ga_{0.9}As$ strained layer, and an undoped GaAs spacer layer. The well-barrier structure consists of an $In_{0.1}Ga_{0.9}As$ sub-well layer, two GaAs well layers, and two AlAs barrier layers. Then there are symmetrical structures that are composed of a same spacer layer, a strained layer, a spacer layer, and buffer layers in turn. Table 1 shows the structure and doping profiles of the DBRTD.

Table 1 Schematic MBE structure of the DBRTD

500nm	GaAs	$3\times10^{18}cm^{-3}$
5nm	GaAs	$1\times10^{18}cm^{-3}$
5nm	GaAs	$5\times10^{17}cm^{-3}$
5nm	GaAs	$1\times10^{17}cm^{-3}$
5nm	GaAs	
5nm	$In_{0.1}Ga_{0.9}As$	
0.5nm	GaAs	
4nm	$In_{0.1}Ga_{0.9}As$	
0.5nm	GaAs	
1.7nm	AlAs	
0.5nm	GaAs	
1.7nm	AlAs	
0.5nm	GaAs	
5nm	$In_{0.1}Ga_{0.9}As$	
5nm	GaAs	
5nm	GaAs	$1\times10^{17}cm^{-3}$
5nm	GaAs	$5\times10^{17}cm^{-3}$
5nm	GaAs	$1\times10^{18}cm^{-3}$
1000nm	GaAs	$3\times10^{18}cm^{-3}$
(100) SI-GaAs substrate		

Isolated mesa structures are formed by contact photolithography (Suss Microtec) and non-selective wet etching techniques (citric acid solution: hydrogen peroxide = 10 ∶1). Resist is used for mask in etching. AuGeNiAgAu and TiAu metalization (DMDE450 film evaporation station) are made for the ohmic contacts and connect line, respectively, by metal lift-off. SiO_2 and Si_3N_4 are deposited through Nextral PECVD to form insulated layers and then are removed partly by wet etching (NH_4F ∶ice acetic acid = 1 ∶1) and RIE dry etching respectively to open windows for connect lines. Figure 1 shows the schematic mesa structure of the DBRTD without the SiO_2/Si_3N_4 layer in order to view easily.

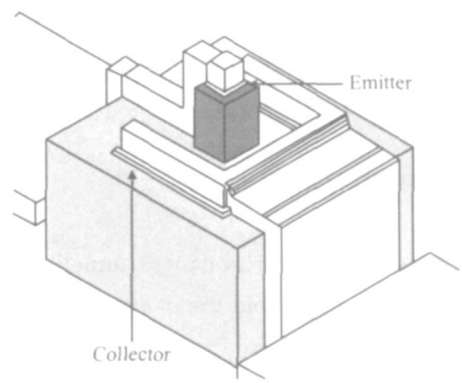

Fig. 1 Schematic mesa structure of the DBRTD

3 Device measurements and discussion of results

The current-voltage (I-V) characteristics of the diodes are measured at room temperature by a semi-conductor parameter analyzer. Figure 2 shows the I-V characteristic of the DBRTD with a 4μm × 4μm emitter at room temperature. The I-V characteristic of the DBRTD is measured with a negative bias, which refers to an electron injection from the bottom contact, i.e. bottom buffer. For the negative bias the PVCR is 13.98 and the peak current density is 89kA/cm^2. The performances of the DBRTDs are much better than those of Wang *et al*.[10], with roughly identical materials structure, as well as

other reported DBRTDs with GaAs substrate so far.

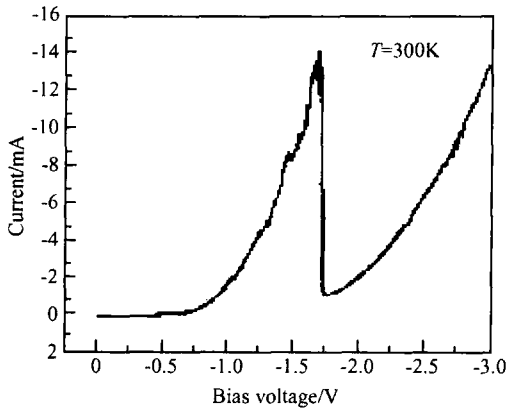

Fig. 2 *I-V* curve of RTD with a 4μm ×4μm emitter PVCR = 13. 98 with I_p = - 0. 014309A, V_p = - 1. 68V, I_v = - 0. 0010236A, V_v = - 1. 707V

The great improvement of performance can be attributed to the use of $In_{0.1}Ga_{0.9}As$ layers, better quality material, and fabrication flows. As shown in Fig. 3, the conduction band energy level of $In_{0.1}Ga_{0.9}As$ is lower than that of GaAs, so when $In_{0.1}Ga_{0.9}As$ layer is introduced between GaAs layers, the potential well of GaAs layer is deepened, resulting in an increase of relative height of AlAs barriers. It is helpful to enlarge both the PVCR and the peak current density, and at the same time non-tunneling current components are depressed efficiently. The roles of $In_{0.1}Ga_{0.9}As$ layers can be similar to sub-well[11] when $In_{0.1}Ga_{0.9}As$ layers lie in GaAs space layers and GaAs well respectively. The thicknesses of the AlAs barrier layers are as thin as 1. 7nm and are also helpful to increase the PVCR and the peak current density, since the thinner the barriers are, the higher the peak current densities are, and the PVCRs of devices are then enlarged[12].

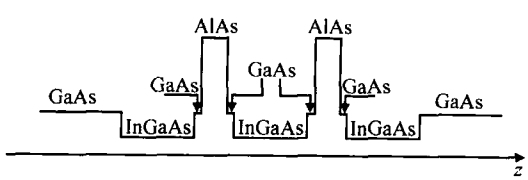

Fig. 3 Schematic conduction band diagram with *z* direction that parallels the current one in DBRTD

As shown in Fig. 4, the emitter of the RTD is surrounded by its collector. This unique layout is used for the reduction of contact resistance and non-uniformity in the emitter current, resulting in large current density in the DBRTDs.

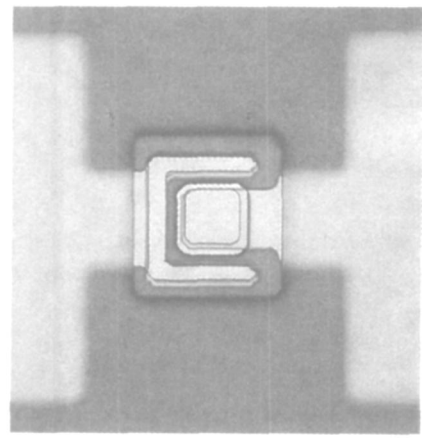

Fig. 4 Top picture of RTD

4 Conclusion

Through introducing the $In_{0.1}Ga_{0.9}As$ layer between the GaAs layers in AlAs/ GaAs/ $In_{0.1}Ga_{0.9}As$/ GaAs/ AlAs DBRTDs with SI-GaAs substrate, the potential well of GaAs layer is deepened, and the height of barriers is functionally able to be enhanced, resulting in the realization of a high PVCR and a peak current density. Thin barriers and a special shape of collector are presented and used for increasing the peak current density and the total current density respectively. The characteristic of DBRTDs at room temperature in this work are much better than all other reported GaAs-substrate DBRTDs. From a practical point of view, this is very encouraging.

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室温下高峰谷电流比、高峰电流密度的双势垒共振隧穿二极管*

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摘要: 在半绝缘 GaAs 衬底上制作了 AlAs/GaAs/$In_{0.1}Ga_{0.9}As$/GaAs/AlAs 双势垒共振隧穿二极管. 在 GaAs 层中加入 $In_{0.1}Ga_{0.9}As$ 层用以降低势垒两边的势阱深度, 从而提高了器件的峰谷电流比和峰电流密度. 为了减小器件的接触电阻和电流的非均匀性, 使用了独特形状的集电极, 总的电流密度也因此提高. 薄栅也有助于提高器件的 PVCR 和峰电流密度. 在室温下测得其峰谷电流比高达 13.98, 峰电流密度大于 89kA/cm^2.

关键词: 共振隧穿二极管; 峰谷电流比; 峰电流密度

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