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Characteristics of a 0.1μm SOI Grooved Gate pMOSFET

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Abstract: A 0.1μm SOI grooved gate pMOSFET with 5.6nm gate oxide is fabricated and demonstrated. The groove depth is 180nm. The transfer characteristics and the output characteristics are shown. At $V_{ds} = -1.5V$, the drain saturation current is 380μA and the off-state leakage current is 1.9nA; the sub-threshold slope is 115mV/dec at $V_{ds} = -0.1V$ and DIBL factor is 70.7mV/V. The electrical characteristic comparison between the 0.1μm SOI grooved-gate pMOSFET and the 0.1μm bulk grooved gate one with the same process demonstrates that a 0.1μm SOI grooved gate pMOSFET has better characteristics in current-driving capability and sub-threshold slope.

Key words: SOI; grooved gate pMOSFET; sub-threshold slope

EEACC: 2520M; 2560Z

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1 Introduction

In the deep-sub-micron field, the small dimensional effects, such as the SCE (short-channel-effect) and the DIBL (drain-induced-barrier-lowering) effect, have been the great obstacle for the scaling-down rule. However, traditional methods, such as increasing the substrate impurity, reducing the gate oxide thickness, and lowering the power supply, cannot suppress these effects effectively. To try and overcome these small dimensional effects, other researches have been performed, focusing on two aspects: substrate material research and new device structure development.

In the field of substrate material, SOI (silicon-on-insulator) technology has been accepted and used widely for its low power supply, low power consumption, high speed, and high driving capability, in comparison with the bulk one. SOI technology realizes the fully dielectric isolation between devices, so that the latch-up effect is concealed completely. Furthermore, a shallow junction can be shaped automatically in SOI technology. In addition, perfect performance in resisting radiation and temperature reliability ensures a wide application field for SOI technology.

In the field of new device structures, grooved-gate devices attract the industry's attention for the good match it has with planar device process. In this structure, S/D regions are isolated by the groove, and the electric field spreading of the drain region to the source region is decreased, so that the SCE and punching-through effect are suppressed. Furthermore, for the electrical line concentrating at the groove corner, two potential barriers, which resist the HCE and the threshold voltage lowering with the channel length decreasing, arise. Some literatures reported the 10nm dimension grooved-gate devices is without an obvious SCE obstacle.

In this paper, a 0.1μm SOI grooved gate pMOSFET with 5.6nm gate oxide is fabricated and demonstrated. The groove depth is 180nm. The transfer characteristics and the output characteris-

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2 Device structure & fabrication

0.1μm PD-SOI grooved gate pMOSFETs on implanted oxygen (SIMOX) were fabricated with a 500nm thick silicon active layer, 370nm thick buried oxide (BOX) and a p-type substrate. In the device fabrication, devices were isolated with LOCOS technology. Certain dose of P^{31} implantation and drive-in at 1150 ℃ are to shape n-well region, where S/D implantation is carried out with a layer of S/D mask to form the S/D junction region. Then E-beam lithography to pattern the groove and an RIE etch step is followed to construct the gate groove. To get a suitable threshold voltage, a threshold adjusting step is added. Next step, 5nm thin film gate oxide is generated and 260nm poly-silicon is deposited consequently to shape the gate electrode. A key process we would encounter here is the poly-gate patterning, which is different from planar devices. We should leave a wider space than the groove width to ensure a full-filled groove and ensure that a reasonable poly-gate is formed. After the salicidation, devices were metalized using a typical backend flow. Table 1 shows the counterpart process parameters in this process flow. Bulk grooved gate pMOSFET devices of the same dimension with SOI devices were fabricated with the same process conditions.

Table 1　Process parameters of a 0.1μm dimension SOI grooved gate pMOSFET

n-well implant	P^{31} 80keV, 7 × 10^{12} cm^{-2}
Threshold implant	P^{31} 80keV, 8 × 10^{11} cm^{-2}
p^{+} S/D implant	BF_2, 25keV, 3 × 10^{15} cm^{-2}
p^{+} poly-silicon implant	BF_2, 25keV, 3 × 10^{15} cm^{-2}

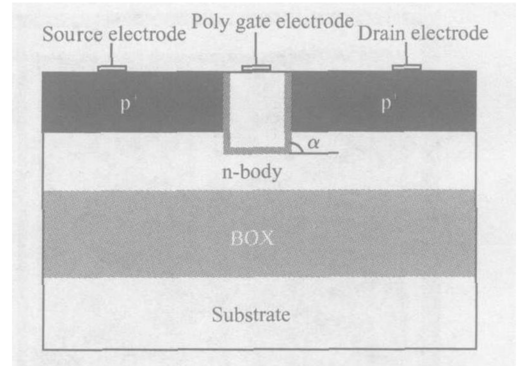

Fig. 1　Device structure of SOI grooved gate pMOSFET

The fabricated device structure parameters are shown in Table 2. Here, the gate length, the groove depth, the gate oxide thickness were measured from SEM, and the S/D junction depth was from the data from the TSUPREM4 simulation with calibrated process parameters. The SEM photos of the groove structure are shown in Fig. 2.

Table 2　Device structure parameters of a 0.1μm dimension SOI grooved gate pMOSFET

Gate length	0.1μm
Groove depth	0.18μm
Gate oxide thickness	5.6nm
S/D junction depth	0.13μm

3 Results & analysis

After the fabrication of the devices, we measured the characteristics with a Keithley 4200 SCS semiconductor characteristics system. The source and the substrate are grounded. Figure 3(a) shows the transfer characteristics of a 0.1μm dimension SOI grooved gate pMOSFET at $V_{ds} = -0.1V$. The threshold voltage measured at $I_{ds} = 1μA$ is $-0.92V$, which is much higher than the same dimension planar one. The reason lies in two aspects: one is the groove corner potential barrier, which interrupts the carriers to flow in the channel. The other is a slightly deeper gate groove, which prevents the S/D regions from punching through, and generates a larger negative junction depth, so a weaker control ability of gate to channel contrib-

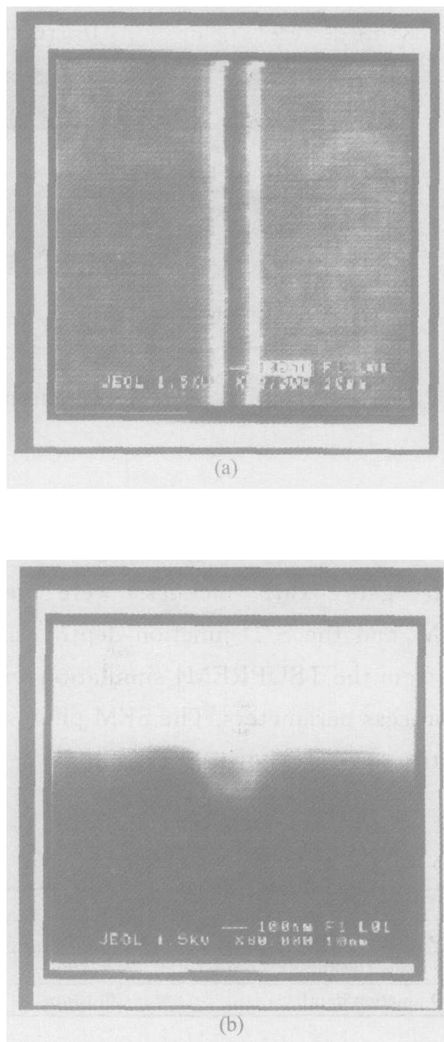

Fig. 2 SEM photos of the groove structure (a) Planar photo; (b) Cross-section photo

utes to a higher threshold voltage. A sub-threshold slope of 115mV/dec is measured at Fig. 3(b) and the off-state leakage current is 1.9nA.

For DIBL, we use the $\gamma_{DIBL} = V_{th}(0.8) - V_{th}(0.1)/(0.8 - 0.1)$ to get the DIBL factor of 70.7mV/V.

Figure 4 shows the output characteristics of a 0.1μm dimension SOI grooved gate pMOSFET measured at $V_{gs} = 0 \sim -3V$ with the step of 0.3V. The saturation drain current measured at $V_{gs} = V_{ds} = -1.5V$ is 380μA, and at $V_{gs} = V_{ds} = -3V$ is -2.9mA.

Table 3 shows the characteristics comparison result of a planar pMOSFET, bulk grooved gate pMOSFET and a SOI grooved gate pMOSFET

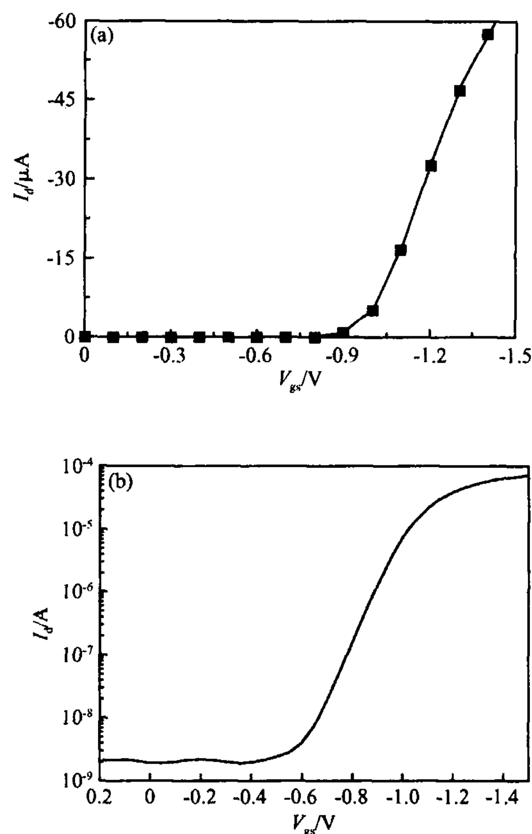

Fig. 3 Electrical characteristics of 0.1μm dimension SOI grooved gate pMOSFET (a) Transfer characteristics; (b) Sub-threshold characteristics

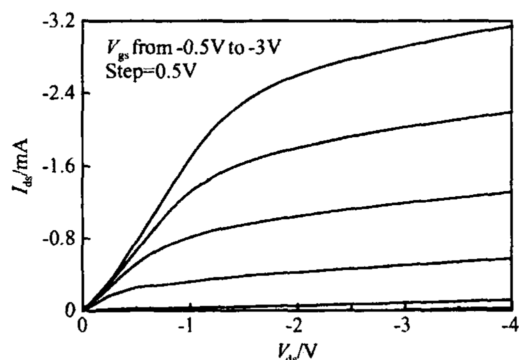

Fig. 4 Output characteristics of 0.1μm dimension SOI grooved gate pMOSFET

with the same dimensions. We can find that SOI grooved gate devices have almost equivalent sub-threshold slope and DIBL factor as the planar one, which are better than those in the bulk grooved gate devices. Measured at $V_{gs} = V_{ds} = -1.5V$, the saturation drain current of a SOI grooved gate pMOSFET is larger than that of the bulk one, but

is a little smaller than the planar devices due to the high threshold voltage of a grooved gate pMOSFET. That means based on the BOX isolation technology, a SOI grooved gate pMOSFET makes much progress in saturation drain current and sub-threshold characteristics compared to the bulk one. In addition, for the high barrier at the groove corner, the threshold voltages of both bulk and SOI grooved gate devices are much higher than the planar devices, which demonstrate the advantage of grooved gate devices in suppressing the SCE.

Table 3　Comparison of three kinds of device structure

Electrical parameter	SOI grooved gate	Bulk grooved gate	Planar devices
Threshold voltage/V	-0.9	-0.8	-0.09
Sub-threshold slope/(mV·dec^{-1})	115	240	113
DIBL factor/(mV·V^{-1})	70.7	83	75
Saturation current/μA	380	160	572

In the process of the device fabrication, the perpendicularity of the groove is influenced by the flow of reactive gas and the proportion of the reactive gases in etching and thus both sides of the groove may not be exactly perpendicular, which will influence the performance of the devices. Here, by the simulator TSUPREM4 and MEDICI, we simulate the transfer characteristics and the output characteristics of the devices according to the angles of the side of the groove. We choose the α of 30°, 60°, 90° in the simulation (α is shown in Fig. 1). Figure 5 shows the simulated transfer characteristics and the output characteristics of the devices. From the figure, we notice that as α is increasing, the threshold voltage is increased and the saturated current is lowered. This is because when α is increasing, the influence of the groove is enhanced, the potential barrier in the corner of the groove is increased and thus needs more gate voltage to cause the conduction of the channel.

4　Conclusion

A 0.1μm SOI grooved gate pMOSFET with 5.6nm gate oxide was fabricated successfully. The experimental result shows excellent characteristics in sub-threshold slope, DIBL factor, and saturation drain current. According to the experimental results, the sub-threshold slope of a SOI grooved gate pMOSFET is 115mV/dec, the saturation current is 380μA, the DIBL factor is 70.7mV/V, while the sub-threshold slopes of a bulk grooved gate pMOSFET and planar devices are 240mV/dec, 113mV/dec, the saturation currents are 160μA, 572μA, the DIBL factors are 83mV/V, 75mV/V, respectively. This demonstrates that among the three kinds of devices, the SOI grooved gate MOSFET shows the best sub-threshold slope and saturation drain current characteristics, and retains the best characteristics in suppressing SCE.

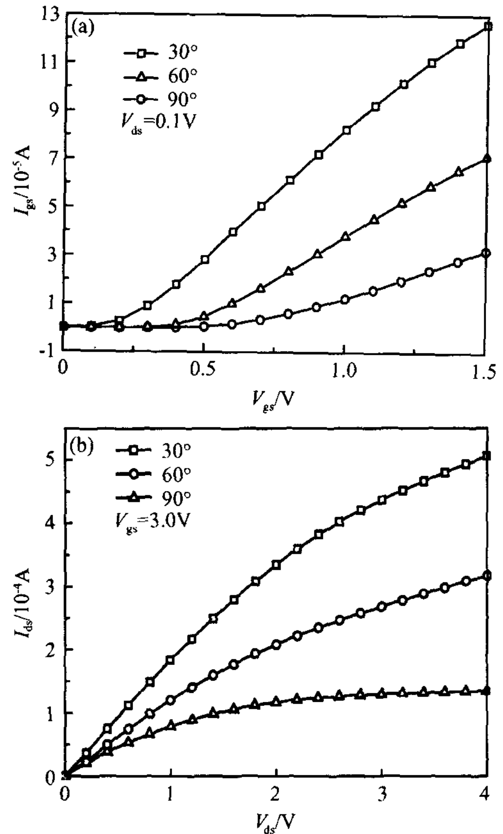

Fig. 5　Simulated transfer characteristics (a) and output characteristics (b) of the devices

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0. 1μm SOI 槽栅 pMOS 器件特性

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摘要: 制造了栅长 0. 1μm ,栅氧厚度 5. 6nm ,栅槽 180nm 的 SOI 槽栅 pMOSFET. 给出了器件的转移特性和输出特性. 在 V_{ds} = - 1. 5V 时,其饱和漏电流为 380μA ,关态泄漏电流为 1. 9nA ;在 V_{ds} = - 0. 1V 下的亚阈值斜率为 115mV/ dec ,DIBL 因子为 70. 7mV/ V. 实验结果表明 ,0. 1μm SOI 槽栅 pMOSFET 比同尺寸体硅槽栅 pMOSFET 拥有更好的电流驱动能力和亚阈值特性.

关键词: SOI; 槽栅 pMOSFET; 亚阈值

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