# A Fractional-N CMOS DPLL with Self-Calibration *

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**Abstract:** A digital phase-locked loop (DPLL) based on a new digital phase-frequency detector is presented. The self-calibration technique is employed to acquire wide lock range, low jitter, and fast acquisition. The DPLL works from 60 to 600MHz at a supply voltage of 1.8V. It also features a fractional-N synthesizer with digital 2nd-order sigma-delta noise shaping, which can achieve a short lock time, a high frequency resolution, and an improved phase-noise spectrum. The DPLL has been implemented in SMIC 0.18μm 1.8V 1P6M CMOS technology. The peak-to-peak jitter is less than 0.8% of the output clock period and the lock time is less than 150 times of the reference clock period after the pre-divider.

**Key words:** digital phase-locked loop; phase-frequency detector; self-calibration; voltage controlled oscillator; fractional-N

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## 1 Introduction

Phase-locked loops (PLLs) are widely used for clock generation in digital and mixed analog/digital chips designed for wireless communication and other applications. Low frequency and phase jitter are very important performance requirements for PLLs. The wide lock range is another key requirement in PLLs because of the constant device for more bandwidth in modern communication[1]. Considerable work has been put into reducing jitter. In 1996, Maneatis introduced a self-biased technique to achieve minimal jitter accumulation in PLL[2]. Optimizing the parameters of the phase-locked loop also improves the jitter performance to some extent[3]. However, when the lock range increases, the jitter of the output clock also increases[4,5]. So, this design focuses on presenting a method to meet wide lock range and low jitter requirements at the same time. The proposed digital PLL (DPLL) uses a digital phase-frequency detector (DPFD) and a self-calibration technique to get wide lock range, low jitter, and fast acquisition. It also features a fractional-N synthesizer with digital 2nd-order sigma-delta noise shaping to achieve a high frequency resolution and an improved phase-noise spectrum.

## 2 DPLL structure and operating principles

A DPLL functional block diagram is shown in Fig. 1. DPFD detects the phase and frequency

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difference between the reference and the output clock from the programmable divider. In this design, the difference is a five-bit multi-level pulse from the digital up/down counter. The multi-level pulse is fed to a digital-to-analog converter (DAC) to be converted into an analog signal. The low-pass filter smoothes the analog signal and the output is the control voltage of the voltage-controlled oscillator (VCO). The VCO changes its output frequency according to the control voltage and the output frequency is proportional to the average value of the multi-level pulse. The feedback loop is closed via the dividers, which forces the system to go to a steady state.

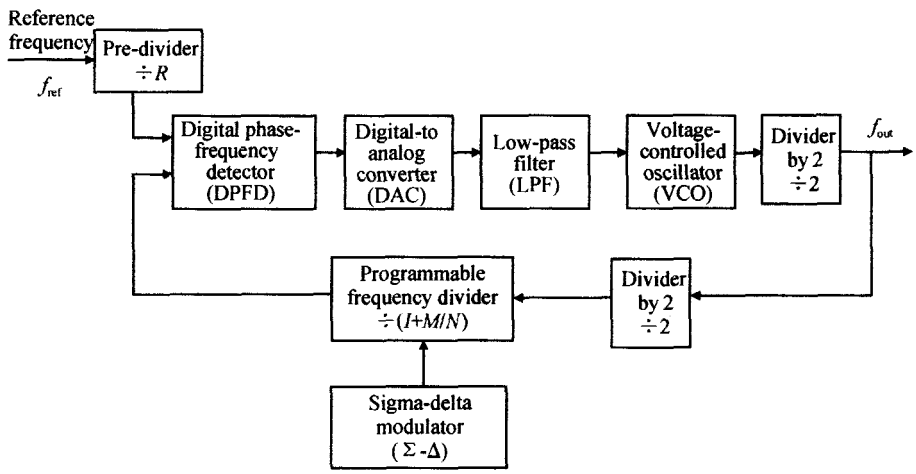


Fig. 1 DPLL functional block diagram

The frequency of the VCO is twice the output frequency. The first divider by two is utilized to achieve a 50 % duty cycle, which is critical in most applications. The second divider by two assures that the programmable divider operates on a lower frequency and reduces the multiplication factor range. The programmable divider is connected between the VCO and the DPFD to generate the various output frequencies. From Fig. 1, the DPLL produces an output clock at the frequency:

$$f_{out} = \frac{2}{R}\left(I + \frac{M}{N}\right) f_{ref} \qquad (1)$$

where $f_{ref}$ is the reference frequency, its range is 10～100MHz, $f_{out}$ is the output frequency, its range is 60～600MHz, $R$ is the pre-division factor, the integer from 1 to 16, $I$ is the integer part of the multiplication factor $F(F = I + M/N)$, $I$ is in range from 5 to 16, if it is less than 5, the DPLL accepts 5, $M/N$ is the fraction part of the multiplication factor $F$. Here $M$ and $N$ are integer, respectively in the ranges of 0～1023 and 1～1024.

## 3 Circuit description

### 3.1 Digital phase-frequency detector

In this design, the DPFD is implemented as a 5bit asynchronous up/down counter (Fig. 2). During the lock-in process the frequency of the reference clock and feedback clock is different. The counter is incremented by 1 at the positive edge of the reference clock and decremented by 1 at the positive edge of the feedback clock. Thus, the DPFD generates a multi-level pulse MP〈4 :0〉 (as shown in Fig. 3). If the reference clock frequency is higher, MP〈4 :0〉 increases to raise the frequency of the VCO. If the feedback clock frequency is higher, MP〈4 :0〉 decreases to lower the frequency of the VCO. When the reference clock and the feedback clock have equal frequency, the multi-level pulse MP〈4 :0〉 has a constant duty cycle and the VCO is exactly tuned to the required frequency.

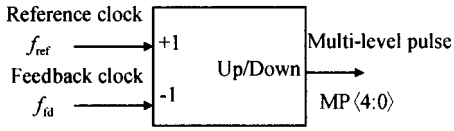


Fig. 2　Digital frequency-phase detector

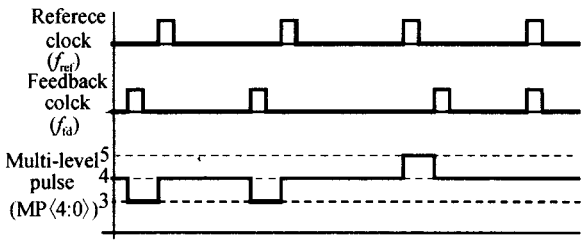


Fig. 3　Reference clock ,feedback clock ,and multi-level pulse MP⟨4 ∶0⟩

The self-calibration technique is employed to speed-up the lock-in process. The self-calibration is performed by two DACs (DAC _ 1 and DAC _ 2) and illustrated by Fig. 4. The higher bits of MP⟨4 ∶0⟩,MP⟨4 ∶1⟩,after being calculated and converted from digital to analog ,functions as the calibration current (Cal _ i). The lower bits MP⟨3 ∶0⟩, after being decoded and converted from digital to analog ,functions as the control voltage (Ctr _ v). Control voltage (Ctr _ v) is fed to a low-pass filter and the output voltage controls the VCO frequency.

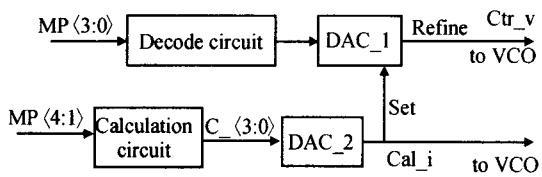


Fig. 4　Block diagram of self-calibration

The self-calibration process is described as follows. At first ,the DPLL is reset and enabled respectively by the reset and enabling signals. And then ,the DPLL calculates the calibration current (Cal _ i) according to the reference clock ($f_{ref}$) and the multiplication factor ($F$).

After that , the calibration current (Cal _ i) sets the control voltage (Ctr _ v) to a special range and assures that the VCO will be close to the center of the frequency range. At the same time , the calibration current (Cal _ i) adjusts the VCO 's step size and makes it proportional to the reference clock. All these help the DPLL get the wider frequency range and the reduced lock time.

After calibration ,the control voltage (Ctr _ v) will have a small vibration due to the vibration of the MP⟨3 ∶0⟩. The feedback loop refines them according to the control voltage (Ctr _ v) until the loop is locked with low jitter.

Through the three steps the DPLL acquires the wide frequency range , short frequency lock time ,and low jitter.

Figure 5 is the core structure of the DAC _ 2 , which is a 4 bits current scaling DAC using binary-weighted current sources with input codes C _⟨3 ∶0⟩. C _⟨3 ∶0⟩ are the outputs of the MP⟨4 ∶1⟩after being calculated ;bias _ 1 and bias _ 2 are the bias voltage generated by the internal bias block. Current scaling is implemented by the $2^1$ (2) to $2^4$ (16) matched MOSFETs. The conversion time of DAC _ 2 is very short and insensitive to parasitics because there are no floating nodes compared with the generic current scaling DAC. The output current ,Cal _ i ,is sent to DAC _ 1 and VCO to set the control voltage and adjust the step size of the VCO. The DAC _ 1 is a parallel-input monolithic multiplying DAC with very high-speed performance and its output is control voltage ,Ctr _ v. The conversion time of the DAC _ 1 is less than 20ns.

The DPLL also has a phase adjusting block , which generates a control signal that minimizes the phase jitter and skews between reference and output clocks. The phase adjusting block starts after frequency lock is achieved. This work mode is the frequency/ phase lock mode and can be selected by the user. The frequency/ phase lock mode is used for synchronous applications and sampling A/ D and D/ A precision converters ,where a phase error can be very important. The frequency/ phase lock mode will be introduced in later work.

### 3.2　Voltage-controlled oscillator

In this design ,a ring-based voltage-controlled

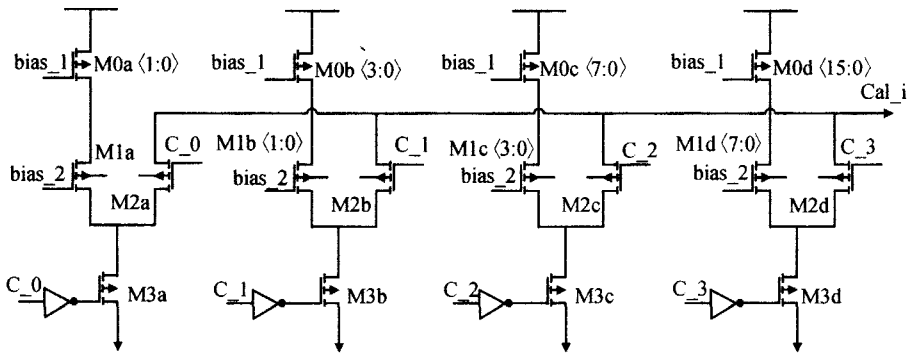


Fig. 5 Core structure of DAC_2

oscillator (VCO) is chosen because it has no external components and is well suitable for integration. Its intrinsic phase noise is relatively high and the dominant noise source is actually due to the power supply. Such noise typically appears as steps or impulses on the power supply of the oscillator, and it affects both the frequency and phase of the VCO, causing cycle-to-cycle jitter[6].

The VCO core structure is shown in Fig. 6. It is based on an inverter-type ring oscillator supplied by a current $I_{ctr}$ coming from the voltage-to-current converter. The voltage-to-current converter is a simple MOS device M4 in the quadratic region, making the overall VCO transfer function approximately linear. A current controlled oscillator (CCO) is the basic element of the VCO, which allows high-frequency operation at low voltage operation.

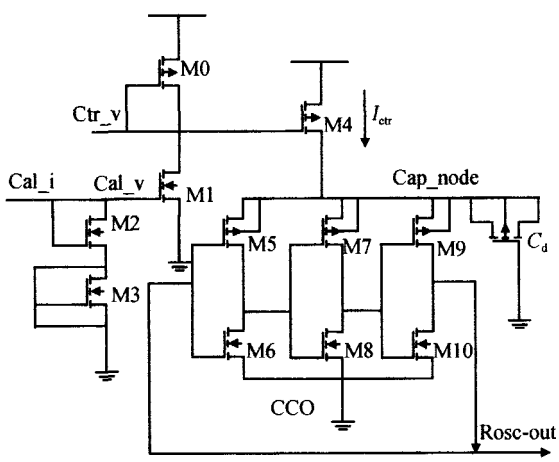


Fig. 6 Core structure of VCO

Transistors M4 and M0 of the current mirror are perfectly matched. Ctr_v controls current $I_{ctr}$ and current $I_{ctr}$ controls the delay time $t_d$ of the CCO. For the equivalent small-signal circuit, $t_d \propto \frac{V_{dd}}{I_{ctr}}$ while $I_{ctr} \propto V_{dd}$, so the effects of the power supply noise can be partly counteracted.

A decoupling capacitance $C_d$ composed of a set of pMOS transistors across the CCO helps to reduce the supply noise injected through parasitic capacitance. The sources and bulks of the transistor M5, M7, and M9 connected to the node cap_node not to $V_{dd}$ assures that the CCO is not sensitive to the supply voltage. All these improve the power supply noise rejection ratio (PSNR) of the VCO.

Rosc_res is the reset signal of the ring oscillator. Cal_i sets the control voltage and adjusts the step size of the VCO after self-calibration. The Ctr_v refines the VCO until the VCO is exactly tuned to the required frequency. The Cal_v is the output of the Cal_i through the current-to-voltage converter.

The VCO output frequency as a function of control voltage is shown in Fig. 7.

### 3.3 Implementation of fractional-N synthesizer

The fractional-N synthesizer is implemented by the programmable divider selecting the division factor $I$ or $I+1$ through the divider modulus control. Equation (2) can be deduced from Eq. (1).

$$f_{out} = \frac{2}{R} \times \left[ \frac{M}{N}(I+1) + \frac{N-M}{N} I \right] f_{ref} \quad (2)$$

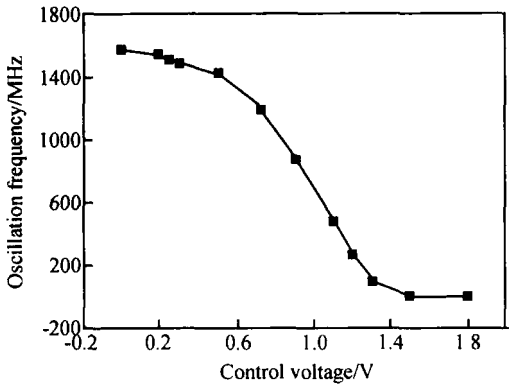


Fig. 7　VCO frequency versus the control voltage Ctr _ v

During $M$ work cycles ,the division factor is set to $I$ + 1 ,while during the $N$ - $M$ work cycles ,the division factor is set to $I$. The fraction part is converted by a digital accumulator to a sequence of "1" and "0".

This technique can get a high frequency resolution with a reduced lock time. However ,because of a switch of the division factor from $I$ to $I+1$, this technique generates undesired spurs. The output is at $\frac{2}{R}(I+\frac{M}{N})f_{\text{ref}}$ with the spurs at offset frequencies equal to multiples of $\frac{M}{N}f_{\text{ref}}$. So in this design ,a sigma-delta modulator is used to eliminate the spurs. The basic structure of the first order sigma-delta modulator is shown in Fig. 8. Equation (3) can be deduced from Fig. 8.

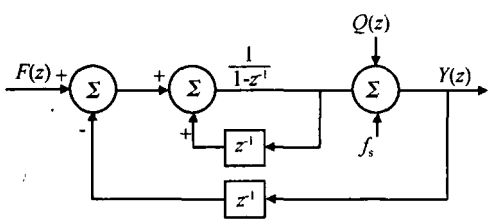


Fig. 8　First-order sigma-delta modulator

$$Y(z) = F(z) + H_n(z)\,Q(z) \qquad (3)$$

$H_n(z)$ and $Q(z)$ respectively is the phase noise and quantization noise.

$$|H_n(f)| = \left|2\sin(\frac{\pi f}{f_s})\right|, \quad 0 \le f \le \frac{f_s}{2} \qquad (4)$$

At low frequencies ,$|H_n(f)|$ tends to go to zero , and when the frequency is near $\frac{f_s}{2}$ ,$|H_n(f)|$ tends to go to the maximum value of 2. The sigma-delta modulator moves the phase noises to higher frequencies ,where it would be filtered by the loop[7].

To get better phase noise spectral ,a higher order sigma-delta modulator is used to shape progressively to a high degree. However the higher order sigma-delta modulator with several feedbacks is not always stable[8]. So ,in this design a second order sigma-delta modulator is employed.

## 4　Results

The DPLL has been simulated by SMIC SPICE model for 0. 18μm logic 1. 8V 1P6M process and the simulation tool is HSPICE. The chip is fabricated in SMIC 0. 18μm , 1. 8V , 1P6M , standard digital CMOS process. Table 1 summarizes the preliminary DPLL performance measurement results.

Table 1　DPLL performance measurement results

| | |
|---|---|
| Output frequency range | 60～600MHz |
| Power consumption | < 3. 5mW at supply voltage of 1. 8V |
| Lock time | < 150 $T_{\text{pre}}$ ( < 15μs) |
| Frequency jitter(peak to peak) | < 0. 8 % of $T_{\text{out}}$ |
| Phase noise | - 102. 6dBC/ Hz @10kHz offset |
| Minimum frequency resolution | 10kHz |

Figure 9 is the simulated results of Cal _ v ,Ctr _ v , and lock flag when the DPLL locks at 400MHz. The DPLL also has a lock control module. The lock control module contains a set of timers indented to generate all necessary control signals during the lock-in time. The lock flag being "1" indicates that the loop is locked. In Fig. 9 ,the lock flag becomes "1" at 7. 659μs and the loop is locked.

Figure 10 shows the measured frequency peak-to-peak jitter versus the output frequency. Jitter is the percent of the absolute jitter/ output clock period. It shows that jitter is less than 0. 5 % of the output clock period for operating frequencies greater than 200MHz. At lowest frequency ( at 60MHz) ,jitter increased to the maximum 0. 8 %,

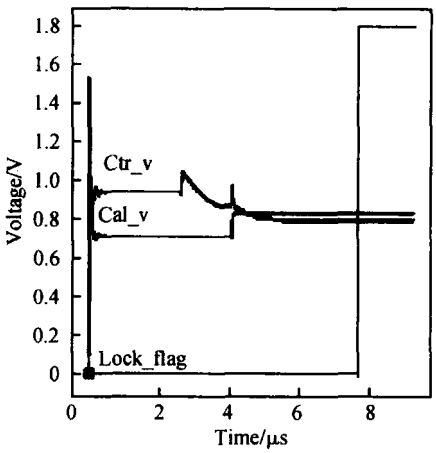


Fig. 9 Simulated Cal_v, Ctr_v, and lock flag

mainly because the loop bandwidth of the DPLL still needs to optimize. Figure 11 is the output spectrum of the proposed DPLL. Figure 12 is the microphotograph of the proposed DPLL core structure.

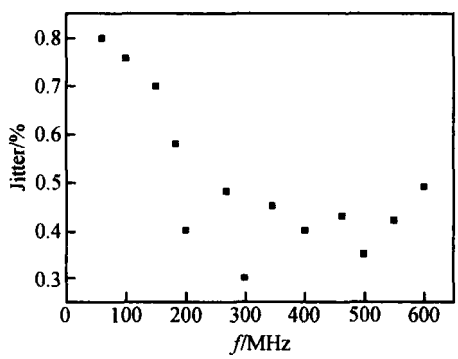


Fig. 10 Measured frequency peak-to-peak jitter versus DPLL output frequency

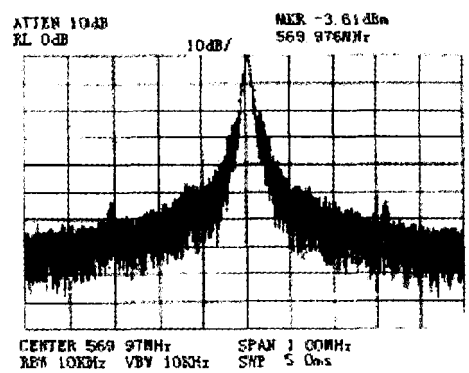


Fig. 11 Output spectrum of the DPLL

Here $T_{out}$ is the output clock period and $T_{pre}$ is the reference clock period after the pre-divider.

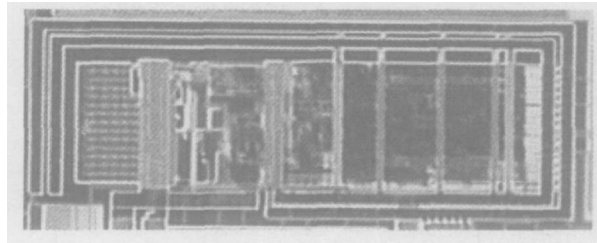

Fig. 12 Microphotograph of the proposed DPLL core structure

## 5 Conclusion

A digital phase-locked loop based on a new phase-frequency detector is fabricated in SMIC 0.18μm, 1.8V, 1P6M, standard digital CMOS process. The self-calibration technique is employed to acquire a wide locking range, low jitter, and fast acquisition. The DPLL works from 60 to 600MHz with the VCO output frequency from 100 to 1500MHz at a supply voltage of 1.8V. The peak-to-peak jitter is less than 0.8% of the output clock period and the lock time is less than 150 times of the reference clock period after the pre-divider.

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# 一种具有自校准功能的 CMOS 分数数字锁相环 *

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**摘要**: 提出了一种数字锁相环(DPLL),它的相频检测器采用全新的设计方法和自校准技术,具有工作频率范围宽,抖动低,快速锁定的优点. 锁相环在 1. 8V 外加电源电压时,工作在 60～600MHz 的频率范围内. 采用分数分频技术,加速锁定过程并具有较小的输出频率间隔,利用 $\Sigma\Delta$ 调制改善相位噪声性能. 设计在 SMIC 0. 18μm,1. 8V, 1P6M 标准 CMOS 工艺上实现,峰-峰相位抖动小于输出信号周期的 0. 8%,锁相环的锁定时间小于参考频率预分频后信号周期的 150 倍.

**关键词**: 数字锁相环; 相频检测器; 自校准; 压控振荡器; 分数分频
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