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Thin-Film Accumulation-Mode SOI pMOSFET

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Abstract: Thin-film accumulation-mode SOI pMOSFETs are fabricated and investigated. Their characteristics are compared with those of thin-film inversion-mode pMOSFETs. The subthreshold slope is 69mV/decade, and it almost has no DIBL effect. The breakdown voltage is 10.5V, which is increased by 40% relative to thin-film inversion-mode pMOSFET. The saturation current is 130μA/μm, which is enhanced by 27% compared with inversion-mode pMOSFET. The per-stage propagation delay of 101-stage SOI CMOS ring oscillator is 56ps with 3V supply voltage.

Key words: accumulation-mode; SOI; pMOS
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1 Introduction

Thin-film silicon on insulator (SOI) is very attractive for deep sub-quarter micron CMOS applications because of reduction of junction capacitance, immunity for radiation, latch up-free for CMOS, suppression of the short-channel effects[1], process simplicity, higher device packing density, high saturation current, absence of the kink effect[2] and so on. A low threshold voltage together with small leakage currents can be obtained which is of major importance for low power-low voltage integrated circuits used in portable electronic systems[3]. Thin-film n-channel SOI MOSFETs have been extensively investigated, and interesting properties such as absence of kink effect, reduced short-channel effect, and reduced hot-electron degradation have been demonstrated[4,5]. The properties of thin-film pMOSFETs have not yet been investigated as thoroughly as those of nMOSFETs. And much less attention has been paid to the accumulation-mode p-channel SOI MOSFETs[6].

Thanks to the buried oxide isolation structure, in addition to the inversion-mode devices, accumulation-mode devices are also possible in the SOI CMOS structure. Accumulation-mode SOI pMOS devices have advantages in high-temperature operation[7], breakdown voltage[8], hot electron effect[9], floating body effect[10], and mobility[11]. It is well-known that both bulk and thick-film SOI p-channel transistors fabricated with thin gate oxides and n^+-polysilicon gate are buried-channel devices. Indeed, a superficial implant of boron must be performed in the channel region in order to bring threshold voltage down to useful values[12]. In the case of a thin-film (<100nm) p-channel device, p-type doping of the body of the transistor must be used in order to obtain useful values of threshold voltage (around -0.7V) when a thin gate oxide ($<$

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20nm) and an n^+-polysilicon gate are used[13].

It is found that, unlike that which occurs in thin-film fully depleted n-channel devices, there is little or no coupling between the front and back gates, unless the surface-state density is very high. When a zero bias is applied to the gate, the film is fully depleted due to both the presence of positive charges at the Si-SiO_2 interface and the negative value of the work function difference between the n^+ polysilicon gate and the p-type body of the device[14]. The gate material-silicon work function difference is given by

$$\Phi_{MS} = -E_g/2 - \ln(N_a/n_i)\, kT/q$$

where n_i is the intrinsic carrier concentration in silicon. When negative gate voltage is applied, the overall hole concentration in the silicon film is increased. Because the device contains no p-n junction, conduction occurs in the body of the device when the film is not fully depleted of carriers. In addition to this "body current", an accumulation channel is created below the gate oxide-silicon interface when the gate voltage is smaller (more negative) than a given "accumulation threshold voltage". If the doping in the film is low enough, and if the (positive) charge density is large enough, the film may still be fully depleted while an accumulation layer is formed[15] at the silicon surface.

2 Device fabrication

The thin-film accumulation-mode SOI pMOSFET structure is shown in Fig. 1. The thin silicon film structure is p^+-p-p^+. The SIMOX wafers used were fabricated by Shanghai Simgui Technology Co., Ltd. The SIMOX wafer was buried oxide layer thickness of 370nm and SOI film layer thickness of 190nm.

The SOI film thickness was thinned down to ~60nm by two-step oxidation and oxide strip. The isolation technology used is LOCOS. BF_2^+ was implanted with energy of 40keV and dose of $6\times10^{11}\,cm^{-2}$ as V_T implant. After growing a 12nm gate oxide, 300nm polysilicon layer is deposited. p^+ with energy of 70keV and dose of $6\times10^{15}\,cm^{-2}$ was implanted into the polysilicon. The gate was patterned and etched to 1.2μm. BF_2^+ with energy of 10keV and dose of $3\times10^{13}cm^{-2}$ was implanted. The purpose of the implantation is to form LDD structure. After a 300nm TEOS oxide spacer formation, BF_2^+ was implanted

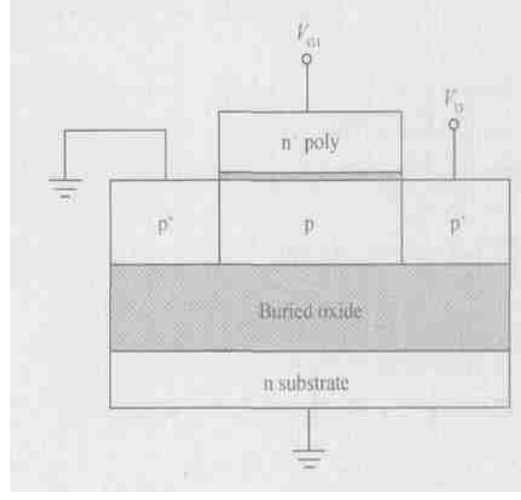

Fig. 1 Cross-section scheme of accumulation-mode SOI pMOSFET structure

with energy of 40keV and dose of $2\times10^{15}cm^{-2}$ as p^+ implantation. After a RTA process, 22nm Ti was deposited. Then $TiSi_2$ was formed using a conventional silicide process. The gate and S/D sheet resistance is about 5Ω/□.

3 Results and discussion

In order to evaluate the basic characteristics of thin-film accumulation-mode SOI pMOSFETs, several characteristics such as subthreshold characteristics, breakdown voltage, and saturation current are shown in the figures below. Breakdown voltage and saturation current are compared with those of the thin-film inversion-mode SOI pMOSFETs. The thin-film inversion-mode SOI pMOSFETs were fabricated formerly using the same wafer and similar technology except the channel doping type.

Figure 2 is the subthreshold characteristic of thin-film accumulation-mode SOI pMOSFET. It is obviously that the accumulation-mode SOI pMOSFET has quasi-ideal subthreshold properties; its subthreshold slope is 69mV/decade. Furthermore, we can see from Fig. 2 that

the accumulation-mode SOI pMOSFETs almost have no DIBL effect. This is mainly because the gate length is not very short. Therefore, as drain voltage increases, the drain to body junction diode expands its space charge-depletion region, but the remaining channel is still relatively long. Therefore the two subthreshold curves are almost identical before V_T.

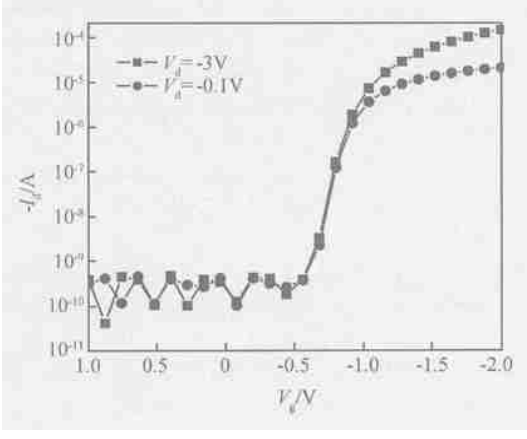

Fig. 2 Subthreshold characteristic of thin-film accumulation-mode SOI pMOSFET

It is shown in Fig. 3 that the drain breakdown voltage of thin-film accumulation-mode SOI pMOSFET is 10.5V, while that of inversion-mode SOI pMOSFET is 7.5V. The drain breakdown voltage of pMOSFET can be enhanced by 40 % by using accumulation-mode.

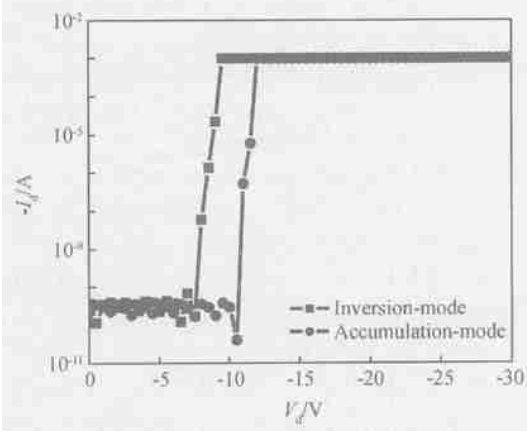

Fig. 3 Breakdown voltage of thin-film accumulation-mode SOI pMOSFET and inversion-mode SOI pMOSFET

Figure 4 shows the output characteristics of thin-film accumulation-mode and inversion-mode SOI pMOSFETs. The saturation current of former is about 130μA/μm, while that of latter is only 102μA/μm. The output characteristics of both accumulation-mode and inversion-mode SOI pMOSFETs are simulated with Tsuprem4 and Medici, too. Figure 5 shows the simulation results of them. The saturation current of accumulation-mode and inversion-mode SOI pMOSFETs is 145, 105μA/μm, respectively. It can be seen that the experiment results are almost consistent with the simulation results. The higher saturation current are due to the reduced scattering encountered by the body current and a lower doping density. Therefore, a higher mobility and thus a larger drain current can be expected, which leads to a smaller difference in the mobilities between pMOS and nMOS devices.

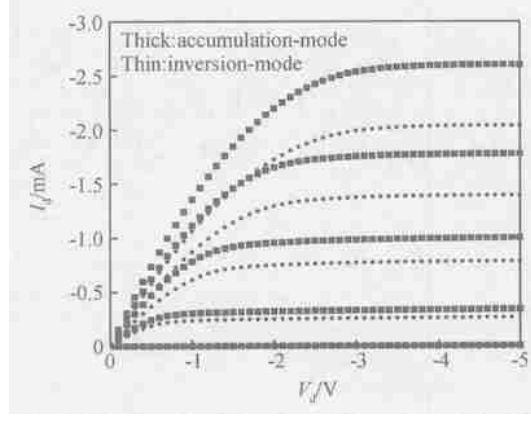

Fig. 4 Output characteristics of thin-film accumulation-mode SOI pMOSFET and inversion-mode SOI pMOSFET

Figure 6 shows the propagation delay of 101-stage SOI CMOS ring oscillator. The ring oscillator was fabricated with inversion-mode nMOSFET and accumulation-mode pMOSFET. The per-stage propagation delay is 56ps with 3V supply voltage.

4 Conclusion

In this paper, thin-film accumulation-mode SOI pMOSFETs have been investigated in detail. The subthreshold slope of thin-film accumulation-mode SOI

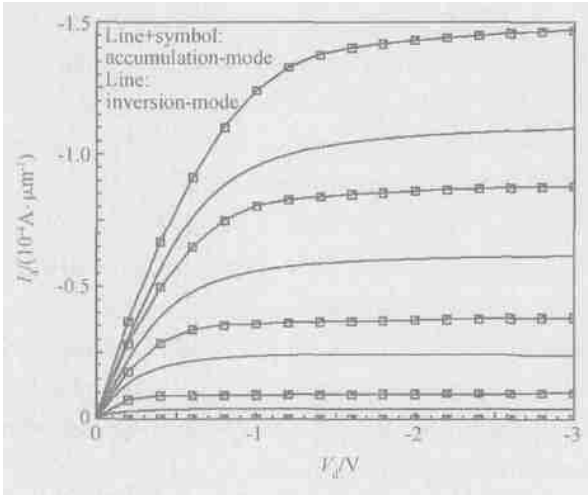

Fig. 5 Simulated output characteristics of thin-film accumulation-mode SOI pMOSFET and inversion-mode SOI pMOSFET

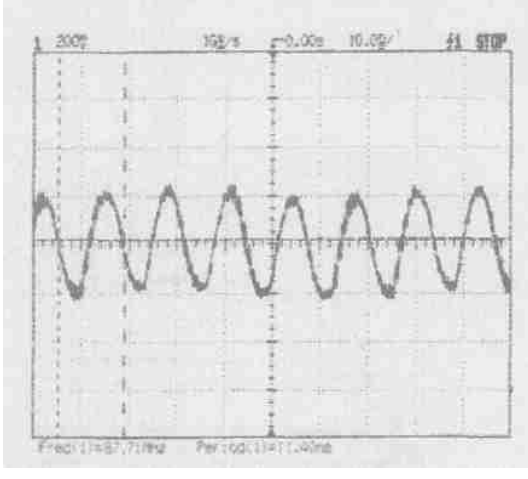

Fig. 6 Propagation delay of 101 stage SOI CMOS ring oscillator

pMOSFET is 69mV/ decade, and it almost has no DIBL effect. The breakdown voltage is 10.5V, which is increased by 40 % relative to inversion-mode pMOSFET. Drive current of 130μA/μm enhanced by 27 % by using inversion-mode has been achieved. The per-stage propagation delay of 101-stage SOI CMOS ring oscillator fabricated with inversion-mode nMOSFET and accumulation-mode pMOSFET is 56ps with 3V supply voltage.

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薄膜积累型 SOI pMOSFET

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摘要: 对薄膜积累型 SOI pMOSFET 的制备和特性进行了研究. 把一些特性和反掺杂型 SOI pMOSFET 进行了比较. 其亚阈值斜率只有 69mV/ decade, 而且几乎没有 DIBL 效应. 漏击穿电压为 10. 5V, 与反掺杂型相比, 提高了 40 %. 饱和电流为 130μA/μm, 比反掺杂型提高了 27 %以上. 在 3V 工作电压下, 101 级 SOI CMOS 环形振荡器的单级门延迟为 56ps.

关键词: 积累型; 绝缘体上硅; pMOS

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