Fabrication of Ultra Deep Electrical Isolation Trenches with High Aspect Ratio Using DRIE and Dielectric Refill

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Abstract: A novel technique to fabricate ultra deep high aspect ratio electrical isolation trenches with DRIE and dielectric refill is presented. The relationship between trench profile and DRIE parameters is discussed. By optimizing DRIE parameters and RIE etching the trenches' opening, the ideal trench profile is obtained to ensure that the trenches are fully refilled without voids. The electrical isolation trenches are 5μm wide and 92μm deep with 0.5μm thick oxide layers on the sidewall as isolation material. The measured *I-V* result shows that the trench structure has good electrical isolation performance: the average resistance in the range of 0～100V is more than $10^{11}\Omega$ and no breakdown appears under 100V. This isolation trench structure has been used in fabrication of the bulk integrated micromachined gyroscope, which shows high performance.

Key words: deep reactive ion etching; electrical isolation trenches; bulk microstructures; monolithic integration

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1 Introduction

Micro-electro-mechanical systems (MEMS) technology has received increasing attention in recent years[1,2]. Compared with conventional devices, MEMS devices have an advantage of size, weight, cost, and power consumption. However, the performance of present MEMS sensors (such as MEMS gyroscopes), especially the accuracy, is not as good as that of conventional sensors. Integrating IC and MEMS devices into one chip can increase the precision and the reliability of MEMS sensors. Both surface microstructures and bulk microstructures can be integrated with circuits. Surface integrated micromachined gyroscopes with on-chip read-out circuits have been reported[3,4], but they have small proof mass, which induces too weak output signal, and they may suffer from thin-film residual stress and sacrificial layer release problems. These drawbacks common in surface MEMS sensors limit their applications. In view of the foregoing, there is a need to fabricate the integrated bulk microstructures, which have large proof mass (the thickness is of the order of 20～100μm). However, integrating microelectronic circuits and bulk MEMS structures on a single chip is difficult in fabrication. In particular, the most difficult is how to realize the electrical isolation between mechanically interconnected units. Some efforts to insulate a moveable microstructure from a fixed structure have been reported[5]. However, ultra-deep isolation trenches (over 50μm) have not been fabricated.

In present work, deep trench etching, thermal oxida-

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tion ,and polysilicon refilling technology are used to fabricate ultra-deep (over 80μm) high aspect ratio isolation trenches. The process to fabricate isolation structures mainly consists of the following two steps :firstly ,use deep reactive ion etching (DRIE) technology to create deep and narrow silicon trenches whose sidewall profile is suitable to refill polysilicon without voids. Secondly ,a thermal oxide is grown on the trench sidewall surface as an isolation layer and then a LPCVD undoped polysilicon is deposited to refill the trenches.

2 Fabrication

The starting materials are 〈100〉 moderately doped n-type ,100mm. single crystal silicon wafers. The fabrication process combines DRIE , thermal oxidation , and polysilicon refill. Firstly ,5μm wide and 92μm deep silicon trenches are etched by DRIE technology. Since the trenches are very deep (over 80μm) ,the thick photoresist is used as a mask (more than 2μm) . In order to acquire desired isolation trenches without voids in the coming refill process ,the trench profile must be controlled carefully by selecting optimal DRIE process parameters ,which will be discussed in the section 3. Secondly ,a 0. 5μm thick thermal oxide layer is formed on both the surface of wafer and the sidewall of trenches ,which acts as an isolation layer between the polysilicon and the substrate. After oxide growth , a conformal LPCVD undoped polysilicon is deposited to refill the trenches. The thickness of the polysilicon depends on the width of the trenches (more than half of the trench width) . Then reactive ion etching (RIE) is used to etch the photoresist and the polysilicon to realize the planarity of surface after the wafer is coated with photoresist. Finally , a 1. 0μm thick thermal oxide layer is formed on the surface of substrate to cover the undoped polysilicon bars.

3 Results and discussion

This work is performed with a surface technology systems (STS) multiplex ICP as the DRIE equipment. This etching system uses the high aspect ratio Si etching (HARSE) process , ensuring the achievement of features with high vertical aspect ratio ,anisotropic profiles ,high Si etched rates , and good dimensional precision[6 ,7] . This DRIE technique is a patented process developed by Robert Bosch GmbH ,called the Bosch process. Unlike the previous simultaneous sidewall passivation technique ,the Bosch process uses an alternation between separated etching and passivation (polymerization) to achieve its technical targets.

In order to obtain desired isolation structures without voids in bulk fabrication ,the silicon trenches etching is the most important step. The sidewall profile should be controlled carefully to make sure that the trenches are refilled well without voids. Therefore ,we select carefully operating conditions of DRIE to fabricate ideal profile of silicon trenches. The depth of silicon trenches depends on the demands of MEMS device structures.

According to the process in section 2 ,the trench profile has to be controlled carefully with DRIE. Therefore , numerous experiments have been carried out to fabricate the silicon trenches with satisfactory profile. As we know , many variables can tailor trench profile in the ICP system of STS , such as SF_6 flow rate , etching active time , etch overlap , electrode power during etching , C_4F_8 flow rate , passivation active time , electrode power during passivation , and APC orientation[8 ,9] . In our work , experiments have been carried out to investigate the relationship between the trench profiles and the duration of the active etching cycle. The experiments show that by changing the passivation/ etching time configuration in one cycle , the profile of the trenches can be adjusted.

Figure 1 shows the experimental results of trenches by etching steps with different passivation/ etching time

configurations in the same experiment. The 7s/7s, 7s/9s and 7s/5s passivation/etching time configurations are used sequentially, each for 5min. The profiles of the trenches first maintain vertical as shown in Fig. 1(a), then

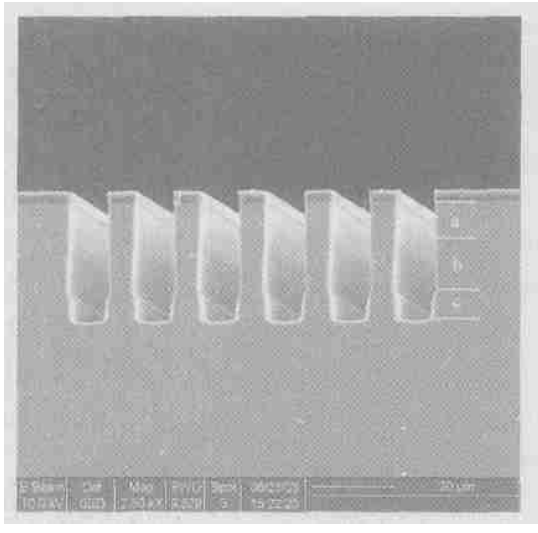

Fig. 1 Experimental result of trenches using three etching steps with different passivation/etching time configurations in the same experiment The 7s/7s, 7s/9s, and 7s/5s passivation/etching time configurations are used sequentially, each for 5min.

become wider (Fig. 1(b)), at last become narrower (Fig. 1(c)). The profile differences can be explained by Fig. 2. As we know, the time multiplexed deep etching (TMDE) technique utilizes an etching cycle flowing SF_6 and then switches to a sidewall passivation cycle using C_4F_8. In the TMDE process, an inhibiting film is first deposited on both the surface of sidewall and the bottom of the trenches, as shown in Fig. 2(a). During the subsequent etching cycle, the passivation film is completely removed from the bottom of the trenches due to the ion bombardment, while the etching of the sidewalls are prevented. After many such cycles, anisotropic etching can be realized. Thus the balance between etching and inhibiting the sidewall is the key mechanism of the different trench profiles we obtained. For example, in Fig. 2(b), as soon as the sidewall is etched right to the position where the sidewall has been etched in the previous cycle, the process switches to the sidewall passivation cycle immediately. If the process is controlled carefully, we can fabricate ideal vertical trench profiles (Fig. 1(a)). If the sidewall is etched more than the previous sidewall etched (Fig. 2(c)), the reentrant slope trenches (Fig. 1(b)) will be created. Furthermore, if the sidewall is etched less than the previous one (Fig. 2(d)), the V-shape profile (Fig. 1(c)) will be created. The passivation/etching time configuration in one cycle can reflect the balance between etching and inhibiting the sidewall. Therefore, we can tailor the trench profile by adjusting passivation/etching time configuration.

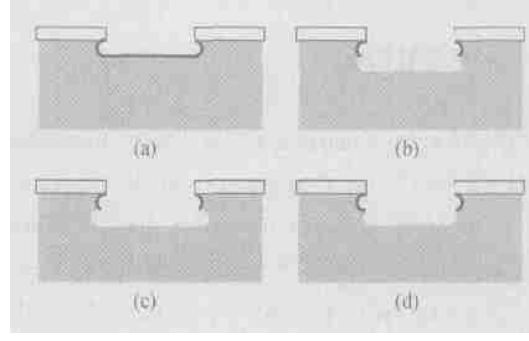

Fig. 2 Schemes illustrating the trenches profile results

Figure 3 shows the SEM micrograph of deep trenches with two different widths (5μm and 50μm) after DRIE. It is well known that DRIE technology has a lag effect (so-called microloading effect), namely the depth is smaller for a narrower trench than for a wider trench[10]. In our experiment, the width of the trench is 5μm and 50μm, the depth of the trench is 98μm and 126μm, respectively. In order to acquire satisfying trench profile, the etching process is divided into two steps. Firstly, a 4～5μm, about 80μm deep trench is formed with 7s/6s passivation/etching time configurations for 1h. However we find that the bottom of the trench is too narrow which is not suitable for isolation. So in the second step, the active etching time is increased from 6s to 10s in order to widen the bottom of the trench. Unfortunately, as shown in Fig. 3, both the bottom and the middle of the narrow trenches are enlarged. However, the results of the wider trenches nearby are different: the bottoms of trenches are widened obviously as respect, but the middle of the trenches do not change in

the whole. The difference of the trench profiles in the trenches with different widths can be explained as following: in the case of wider trench, the etching ions can transport easily to the bottom of trenches even if the trench is very deep. On the other hand, in the case of narrow trenches (less than 10μm), the etching ion cannot reach the bottom freely and the etching byproducts in the trench bottom cannot be removed quickly because the trench is too narrow. As a result, the etching ions accumulate at the middle of trench and enlarge the trench middle. In conclusion, in the shallow trench situation (less than about 40μm), the profiles of narrow and wide trenches are similar because the etch ions can reach the trench bottom freely to react with the silicon at the bottom. Oppositely, in the deep trench situation (more than about 40μm), the results are different. In the narrow trench, the react ions and the etching byproducts cannot transport freely in the trench, so the profile is devastated, while the profile of wide trench is the same as the profile of shallow situation due to the react ions can reach the trench bottom easily.

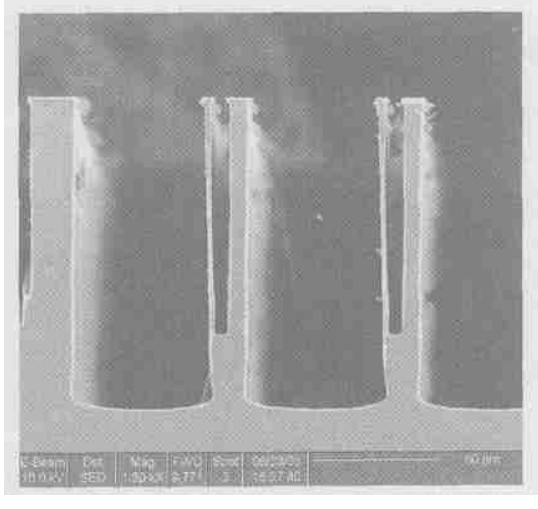

Fig. 3　SEM micrograph of deep trenches of different widths (5μm and 50μm) after DRIE　The trench depths with widths of 5μm and 50μm are about 98μm and 126μm, respectively.

Figure 4 shows the etching results obtained after optimization of the above operating conditions for etching narrow deep trenches. The trenches are 5μm wide and 92μm deep. However, the profile in Fig. 4 is not suitable to refill dielectric fully because the entrance of the trenches is narrower than the middle of trench. To ensure the trench be refill without voids, an additional RIE etching process is adopted after DRIE in order to enlarge the entrance of the trenches. Figure 5 shows the isolation trench structures after RIE, thermal oxidation, and polysilicon refill. The entrance of the trenches is enlarged from 3.5μm to 5μm after RIE. No void is found, so the structure is good enough to be used for mechanical connection and electrical isolation.

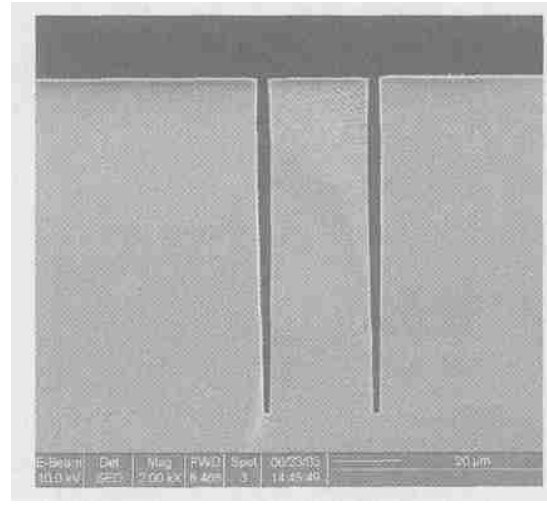

Fig. 4　SEM micrograph of the etching results obtained after optimization of the operating conditions for etching narrow deep trenches　The trenches are 5μm wide and 92μm deep.

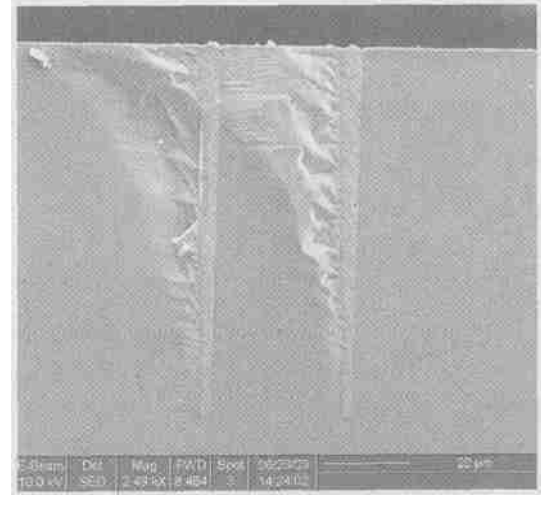

Fig. 5　SEM micrograph of the isolation trench structures after RIE, thermal oxidation, and polysilicon refill

With HP4156b, we measure the *I-V* curve of the electrical isolation trench structures after backside TMAH silicon etching to expose the bottoms of isolation trenches. The curve of current versus applied voltage in the range of 0～100V is shown in Fig. 6. The average resistance is more than $10^{11}\Omega$ and no breakdown appears up to 100V. So the result indicates that the structure has good electrical isolation performance.

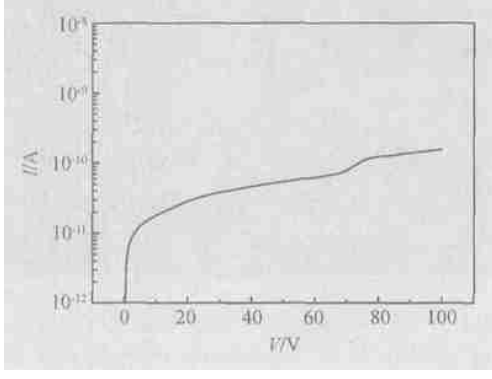

Fig. 6 *I-V* curve of the electrical isolation trench structures after backside TMAH silicon etching to expose the bottoms of isolation trenches

This isolation trench structure has been used in the fabrication of integrated bulk micromachined gyroscopes, which has shown high performance. Figure 7 is the SEM front close-up view of the integrated bulk gyroscope with deep isolation trenches. In this figure, the diodes (upper) and the sensing combs (lower) are electrically isolated by the isolation trenches (middle) to realize the monolithic integration of MEMS with signal processing electronics.

4 Conclusion

With trench etch and polysilicon refill technology, we have developed a novel isolation technology on bulk micromachining. With this technology, ultra deep (over 80μm) high aspect ratio electrical isolation structures are fabricated. The isolation structures can be used to not only mechanically connect, but also electrically isolate, MEMS structure region, and IC region in the integrated bulk silicon MEMS sensors. The result indicates the structure has good isolation performance.

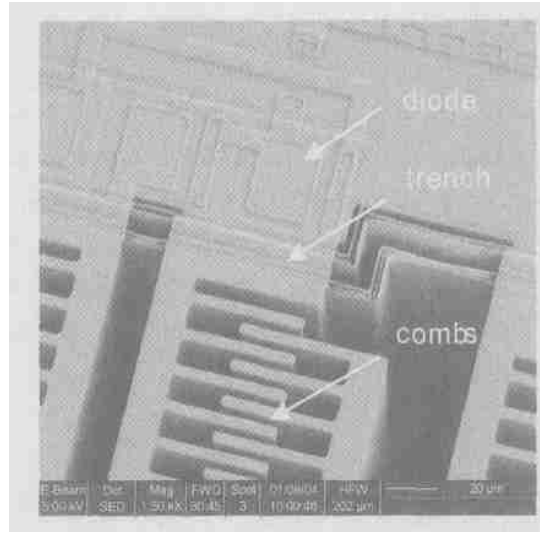

Fig. 7 SEM front view micrographs of the gyroscope structure after DRIE release The comb size: about 4μm width, 4μm gap, and 100μm thickness.

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References

[1] Bryzek J. Impact of MEMS technology on society. Sensors and Actuators, 1996, A56: 1

[2] Bao Minhang, Wang Weiyuan. Future of microelectromechanical systems. Sensors and Actuators, 1996, A56: 135

[3] Clark W A, Howe R T, Horowitz R. Surface micromachined *z*-axis vibratory rate gyroscope. Technical Digest Solid-State Sensor and Actuator Workshop, 1996: 283

[4] John A G, Steven J S, John F C, et al. Single-chip micromachined integrated gyroscope with 50°/h allan deviation. IEEE J Solid-State Circuits, 2002, 37(12): 1860

[5] Xie H, Fedder G K. A DRIE CMOS-MEMS gyroscope. IEEE Sensors Conference, Orlando, Florida, 2002: 12

[6] Lärmer F, Schilp A. Method of anisotropically etching silicon. German Patent, DE4241045

[7] Bhardwaj J K, Ashraf H. Advanced silicon etching using high density plasmas. Proc SPIE Microfabrication Process Technology, 1995, 2639: 224

[8] Ayón A A, Braff R, Lin C C, et al. Characterization of a time multiplexed inductively coupled plasma etcher. J Electrochem Soc, 1999, 146(1): 339

[9] Ayón A A, Zhang X, Khanna R. Anisotropic silicon trenches 300～500μm deep employing time multiplexed deep etching (TMDE). Sensors and Actuators, 2001, A91: 381

[10] Ayón A A, Zhang X, Khanna R. Ultra deep anisotropic silicon trenches using deep reactive ion etching (DRIE). Solid-State Sensor and Actuator Workshop, 2000: 339

用深反应离子刻蚀和介质填充技术制造具有高深宽比的超深电隔离槽

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摘要: 提出了一种利用深反应离子刻蚀(DRIE)和电介质填充方法来制造具有高深宽比的深电学隔离槽的新型技术. 还详细讨论了 DRIE 刻蚀参数与深槽侧壁形状之间的关系, 并作了理论上的阐述. 采用经过参数优化的 DRIE 刻蚀深硅槽, 并用反应离子刻蚀(RIE)对深槽开口形状进行修正, 制造了具有理想侧壁形状的深槽, 利于介质的完全填充, 避免产生空洞. 电隔离槽宽 5μm, 深 92μm, 侧壁上有 0.5μm 厚的氧化层作为电隔离材料. *I-V* 测试结果表明该隔离结构具有很好的电绝缘特性: 0～100V 偏压范围内, 电阻大于 $10^{11}\Omega$, 击穿电压大于 100V. 电隔离深槽被首次应用于体硅集成微机械陀螺仪上的微机械结构与电路之间的电气隔离与机械连接, 该陀螺的性能得到了显著提高.

关键词: 深反应离子刻蚀; 电隔离槽; 体微结构; 单片集成

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