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W/ TiN Gate Thin-Film Fully-Depleted SOI CMOS Devices

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Abstract : TiN gate thin-film fully-depleted SOI CMOS devices are fabricated and discussed. Key process technologies are demonstrated. Compared with the dual polysilicon gate devices ,the channel doping concentration of nMOS and pMOS can be reduced without changing threshold voltage (V_T) ,which enhances the mobility. Symmetrical V_T is achieved by nearly the same V_T implant dose because of the near mid-gap workfunction of TiN gate. The SCE effect is improved when the thin-film thickness is reduced.

Key words : FDSOI; CMOS; mid-gap workfunction; TiN
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1 Introduction

As microelectronics technology enters the deep-submicron arena ,fully-depleted SOI(FDSOI) technology assumes a prominent position as a potential solution to the problems associated with continued device scaling[1]. Some of the benefits of using FDSOI are the reduction of the junction capacitance , the immunity for radiation , the latch up-free for complementary metal-oxide-semiconductor (CMOS) , the suppression of the short-channel effects[2] ,the process simplicity ,higher device packing density ,and so on. FDSOI devices are also superior to thick-film ,partially-depleted SOI(PDSOI) devices ,because FDSOI MOSFETs have no body effect[3].

A problem of FDSOI is threshold voltage (V_T) control. Since complete depletion of the channel region under normal device operation requires an ultra-thin silicon film with a low doping in the channel region[4] ,it is very difficult to obtain desirable V_T with low channel doping by using conventional polysilicon gates. The inverse dual-poly gate ,i. e. p^+ poly for nMOS and n^+ poly for pMOS ,can provide symmetrical V_T ,but the absolute V_T values are too large for operation at low supply voltage[5]. Furthermore , the threshold voltage variation can be caused by silicon film non-uniformity in FDSOI devices. These problems can be solved through using mid-gap work function gate materials. Further performance improving of CMOS devices also has encountered a series of problems such as high gate resistance , boron penetration , and polysilicon gate depletion[6]. Using metal gate can avoid these disadvantages.

Different gate materials , W/ TiN , SiGe , Ta , Mo , and so on , have been proposed to replace polyisilicon. Metal gate electrode is a superior candidate for CMOS devices because it has no gate depletion and has a low sheet resistance. We choose W/ TiN as the gate material because of its high thermal stability ,low resistivity ,and high process compatibility[7]. Another advantage is its mid-gap work

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function, approximately 4.8eV for TiN film, locating in the middle of the silicon band gap.

2 Device fabrication

2.1 Fabrication flow

The SIMOX wafers used were fabricated by Shanghai Simgui Technology Co., Ltd. The SIMOX wafer has 370nm of buried oxide layer and 190nm of SOI film layer.

Figure 1 shows an abbreviated process flow of the thin-film FDSOI device with W/ TiN gate. Except for the gate stack deposition and definition steps, the metal gate devices have the same process flow with conventional poly gate devices. The SOI film thickness was thinned down to

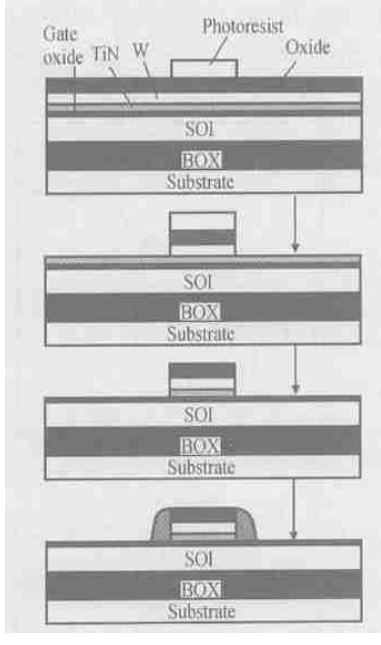

Fig. 1 Abbreviated process flow of the thin-film FDSOI device with W/ TiN gate

60nm by two-step oxidation and oxide strip. The isolation technology used is LOCOS. BF_2^+ was implanted with energy of 40keV and dose of $6 \times 10^{11} cm^{-2}$ as nMOSFETs V_T adjust implant. Phosphorus was implanted with energy of 30keV and dose of $5 \times 10^{11} cm^{-2}$ as pMOSFETs V_T adjust implant. After growing a 12nm gate oxide, the W/ TiN layers were sputtered. A 100nm SiO_2 layer was deposited on the metal layers. After gate patterning to 1.2μm, the etching of W and TiN were done separately to ensure no etch damage to the underlying gate oxide. Little gate oxide loss was observed after TiN etching. Then phosphorus with energy of 10keV and dose of $3 \times 10^{13} cm^{-2}$ was implanted in nMOSFETs. BF_2^+ with energy of 10keV and dose of $3 \times 10^{13} cm^{-2}$ was implanted in pMOSFETs. The purpose of the implantation is to form LDD structure. After a 300nm TEOS oxide spacer formation, BF_2^+ was implanted with energy of 40keV and dose of $2 \times 10^{15} cm^{-2}$ as p^+ implantation. As^+ was implanted with energy of 60keV and dose of $2 \times 10^{15} cm^{-2}$ as n^+ implantation. After RTA process, 20nm-Ti was deposited. Then $TiSi_2$ was formed using a conventional silicide process to reduce the source/ drain sheet resistance.

2.2 Key technology

We choose sputtering deposition because it is more favorable than chemical vapor deposited (CVD) for the conventional CMOS process. The impurity contained in the CVD metal degrades the gate dielectric reliability at high-temperature annealing process[8]. Physical vapor deposition (PVD) usually induces damage to gate dielectric, so how to reduce the degradation of gate oxide and to lower the surface states are the key factors. Smaller RF power and higher N_2/ Ar ratio will lead to a smaller sputtering rate. By reducing the sputtering rate, the surface state density (N_{ss}) can be reduced, too[9]. This indicates less damage to the gate dielectric. Therefore, we reduce the sputtering rate from 8.6nm/ min to 2.2nm/ min. Increasing N_2/ Ar ratio also helps to terminate the dangling bonds by nitridation, which occurs on the dielectric surface during sputtering deposition[10] and reduces the resistivity of TiN. The thickness of TiN is 35nm. When TiN thickness was changed from 20nm to 35nm, the compressive stress of the TiN film was changed into a small tensile stress[11] and induced less damage to the gate dielectric. The thickness of SiO_2 on the stack metal layers is 100nm. The purpose of this layer is to protect the stack gate from damage

in implantation. If the layer is too thick, the depth of contact hole on the gate will be too much deferent with that on the source/ drain. Contrarily, appropriate thickness can help reduce the depth deference of contact hole after annealing. Because in conventional poly gate devices, the dielectric layer thickness on the gate is thinner than that of the source/ drain after annealing.

3 Results and discussion

In order to evaluate the basic characteristics of the TiN gate electrode on the surface channel, subthreshold characteristics of TiN gate and dual-polysilicon gate FD-SOI devices were simulated first as shown in Fig. 2. Both the devices have 0.25μm-length gate and 60nm-thickness SOI film. The simulations were performed using Tsuprem4 and Medici. It is obviously observed that the TiN gate electrode enhances the absolute V_T of both the nMOS and pMOS with the same V_T implant dose. V_T is higher than that of dual-polysilicon gate devices by 180mV and

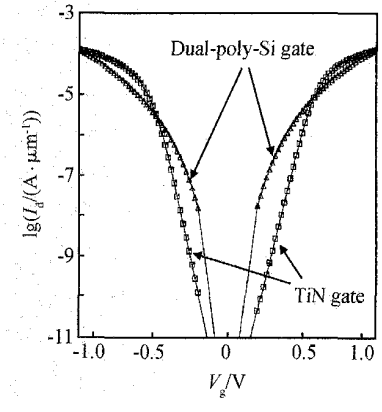

Fig. 2 Subthreshold characteristics for the W/ TiN gate and dual-poly-Si gate

130mV for nMOS and pMOS, respectively. Appropriate V_T with TiN gate FDSOI can be achieved with significantly lower doping. The mobility can also be increased with lower doping. The threshold voltage can be simply expressed as follow:

$$V_T = V_{fb} + 2\phi_f + qN_{ch}T_{Si}/C_{fox}$$

N_{ch} is the impurity concentration, T_{Si} is the thickness of SOI film, C_{fox} is the front gate capacitance, V_{fb} is the flat-band voltage of the front gate. The increase of V_T for TiN gate is primarily due to the near mid-gap work function of TiN. dV_T/T_{Si} is also smaller due to the lower channel doping concentration. Therefore, the V_T dependence on T_{Si} is not significant.

Figures 3 and 4 show the subthreshold characteristic of nMOS and pMOS, respectively. We can see from the figures that the V_T of nMOS and pMOS is 0.845V and -0.840V, respectively. V_T is symmetrical with nearly the same V_T implant dose. This is also due to the near mid-gap work function of TiN. The leakage current in the off region is smaller than the noise current of the test equipment (between 10^{-9}A and 10^{-10}A). This is helpful to reduce the power consumption of the circuits.

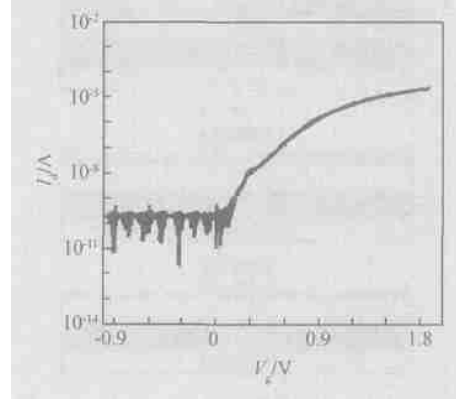

Fig. 3 Subthreshold characteristics of nMOS

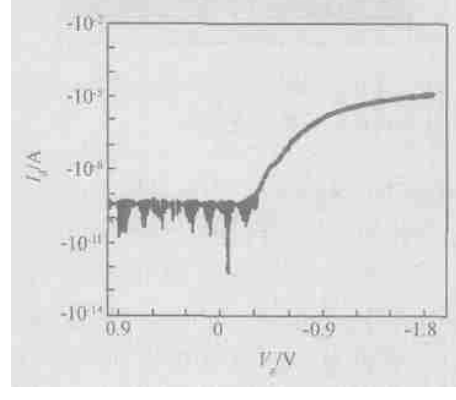

Fig. 4 Subthreshold characteristics of pMOS

The I_d-V_d characteristics of nMOS and pMOS are shown in Figs. 5 and 6. The saturation currents are about

174μA/μm for nMOS and 94μA/μm for pMOS. The saturation currents are not very big. This may due to the high source/drain series resistance of thin SOI film. Higher saturation current can be obtained by using elevated source/drain structure[12].

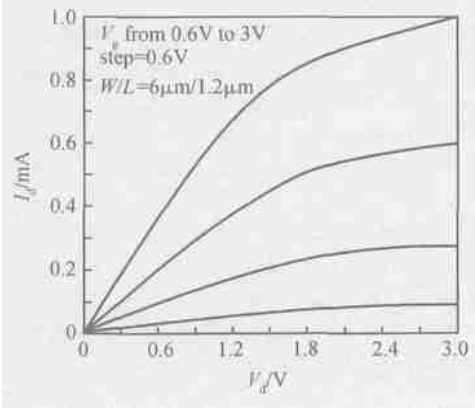

Fig. 5 Output characteristics of nMOS

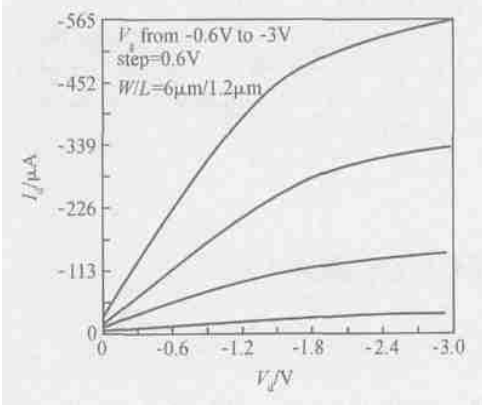

Fig. 6 Output characteristics of pMOS

In order to evaluate the impact of the thickness of thin-film SOI on the short channel effect (SCE), the relationship between V_T and L_{eff} was simulated using Tsuprem4 and Medici with the same V_T implant dose density at the given thickness of SOI. Figure 7 shows V_T versus L_{eff} when T_{Si} is 50nm. Figure 8 shows the V_T versus L_{eff} when T_{Si} is 27nm. We can see from the figures that the V_T roll-off is still quite serious when T_{Si} is around 50nm range, but this condition can be much improved by thinning T_{Si} to about 27nm. For both nMOS and pMOS devices, when the thin-film thickness is reduced, their SCE becomes smaller since the controllability of the front gate over the active channel region is stronger and the source/drain has a less influence on the channel. However, the thinner SOI film can bring the higher source/drain sheet resistance, which reduces the output current. Fully-depleted SOI CMOS devices with elevated source/drain structure can take the advantage of thin-film without raising the source/drain sheet resistance.

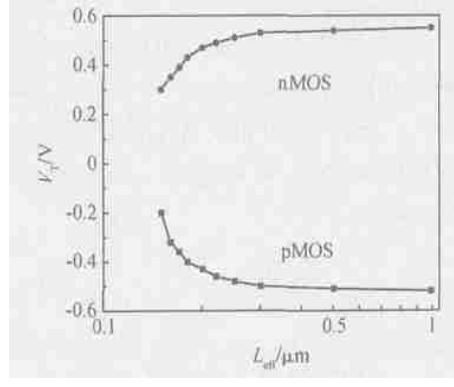

Fig. 7 V_T versus L_{eff} when the thickness of SOI film is 50nm

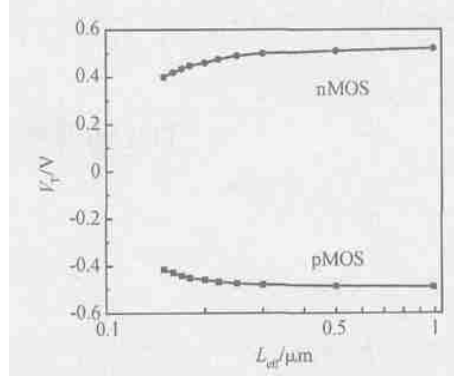

FIg. 8 V_T versus L_{eff} when the thickness of SOI film is 27nm

4 Conclusion

We have successfully fabricated the thin-film FDSOI devices with W/TiN gate. Key process technologies such as deposition mode, sputtering process, and TiN thickness were demonstrated. Under the condition of same V_T implant dose, absolute value of V_T of both nMOS and pMOS by using the TiN gate is higher than that of the dual

polysilicon gate CMOS devices. Therefore, appropriate V_T value can be achieved with lower V_T implant dose. As a result, the mobility is increased, and the saturation current can be increased, too. With the near mid-gap work function of TiN, symmetrical V_T values have been achieved with low V_T implant dose. Furthermore, we can solve the problems such as high gate resistance, boron penetration, and polysilicon gate depletion of conventional poly gate devices. The saturation currents are 174μA/μm for nMOS and 94μA/μm for pMOS. However, the thinner SOI film is, the better to control the SCE effect. The problem of high source/drain resistance of thin SOI film can be solved by elevated source/drain structure.

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TiN 栅薄膜全耗尽 SOI CMOS 器件

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摘要: 制备并研究了 TiN 栅薄膜全耗尽 SOI CMOS 器件, 并对其关键工艺进行了详细阐述. 相对于双多晶硅栅器件, 在不改变阈值电压的前提下, 可以减小 nMOS 和 pMOS 的沟道掺杂浓度, 进而提高迁移率. 由于 TiN 的功函数处于中间禁带, 在几乎相同的调整阈值注入剂量下, 可以得到对称的阈值电压. 当顶层硅膜厚度减小时, 可以改善短沟道效应.

关键词: FDSOI; CMOS; 中间禁带功函数; TiN

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