Design and Fabrication of Schottky Diode with Standard CMOS Process *

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Abstract: Design and fabrication of Schottky barrier diodes (SBD) with a commercial standard 0.35μm CMOS process are described. In order to reduce the series resistor of Schottky contact, interdigitating the fingers of schottky diode layout is adopted. The *I-V*, *C-V*, and *S* parameter are measured. The parameters of realized SBD such as the saturation current, breakdown voltage, and the Schottky barrier height are given. The SPICE simulation model of the realized SBDs is given.

Key words: CMOS; Schottky diode; integration
EEACC: 2560H; 2570D
CLC number: TN311+.7 **Document code:** A **Article ID:** 0253-4177(2005)02-0238-05

1 Introduction

Schottky diodes have advantages such as fast switching speed and low forward voltage drop. Due to these excellent high frequency performance, they have been widely used in power detection and microwave network circuit[1]. Schottky diodes are often fabricated by depositing metals on n-type or p-type semiconductor materials such as GaAs and SiC[2~4]. The properties of forward-biased Schottky diodes are determined by majority carrier, while minority carrier primarily determine those properties of p-n diodes. In order to improve high frequency performance and decrease supply voltage of IC, integrating the Schottky diode into modern IC is very important. But the process that can integrate Schottky diode is often not commercially available and not to integrate with CMOS circuits monolithically. Design about it has ever been introduced and the fabrication of Schottky in standard CMOS process with the additional CMOS process has been repoted while not shown the measured results[5,6]. In this paper we describe the way to design and layout a Schottky diode in a low cost commercial standard CMOS process without any process modification. The measured results and SPICE simulation model are offered.

2 Design and layout of Schottky diode

This design was performed through MPW(multi project wafer) in charted 0.35μm CMOS process. A Schottky diode is formed when a metal layer is deposited directly onto a low doped n-type or p-type semiconductor region. When these two materials are brought into contact with each other, the difference in potential gives rise to a barrier height that the electrons have to overcome for current to flow. The metal on the low-doped semiconductor is the anode and the semiconductor material, which contacted through an ohmic contact, is the cathode. In our design only n-type Schottky diodes were used. A cross section of the Al-Si Schottky diode is shown in Fig. 1.

* Project supported by National High Technology Research and Development Program of China (No. 2003AA1Z1280)
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Received 24 May 2004, revised manuscript received 2 August 2004

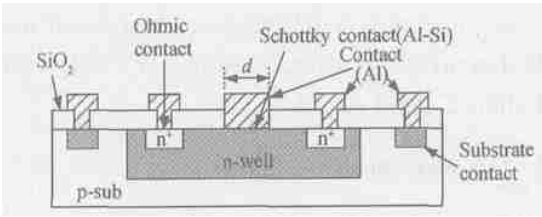

Fig. 1　Cross section of Al-Si Schottky

In our design ,there was no p^+ active region under the contact in n-well ,the contact material is aluminum with area A (equal to $d \times d$) . Therefore ,the metal layer will connect directly to the low-doped n-well. As a result there forms a Al-Si Schottky diode contact. For the foundry process determines most of the parameters such as work function of metal and density of n-well ,we can only control the area A of Schottky diode to modify the I-V curve or other parameters of the diode.

Figure 2 shows the layout of designed Schottky diode. In order to reduce the series resistance of the Schottky diode , firstly , the distance between the Schottky and ohmic contacts was set to the minimum allowable according to the design rules. Secondly ,interdigitating the fingers of Schottky diode layout was adopted. The interdigitated layout offers the advantage of parallel connecting of each series resistance under Schottky contact.

3　Measurement results of the fabricated diode

Three types of interdigitating fingers Schottky diodes with different area have been fabricated in the charted standard 0.35μm CMOS process through MPW. The measured results are discussed.

3.1　I-V performance

Considering the series resistor ,the I-V function of Schottky diode can be express as[7]

$$I = I_s \exp\left(\frac{V - IR_s}{nV_t}\right)\left[1 - \exp\left(\frac{V - IR_s}{V_t}\right)\right] \quad (1)$$

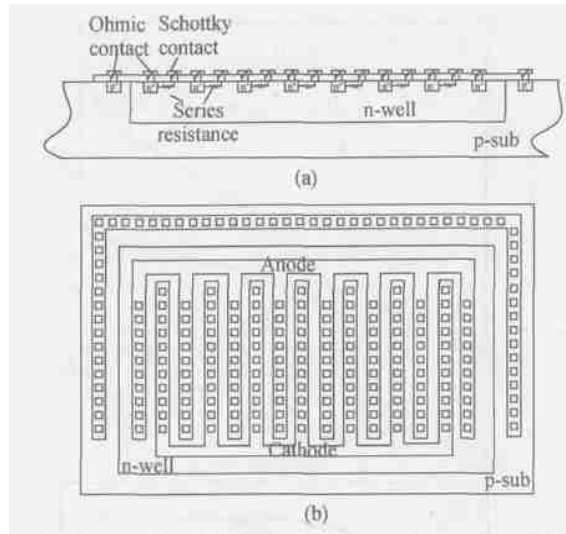

Fig. 2　(a) Cross section layout of the realized Schottky diode; (b) Plane section layout of the realized Schottky diode

where V is the bias voltage , I_s is the saturation current , R_s is the series resistor , V_t is the thermal voltage which equals to kT/q ,and n is the SBD ideality factor which can be calculated as:

$$n = I/\left(V_t \frac{dI}{dV}\right) \quad (2)$$

If the bias voltage is larger than $3kT/q$,Equation (1) can be simplified as

$$I = I_s \exp\left(\frac{V - IR_s}{nV_t}\right) \quad (3)$$

And the Schottky barrier height ϕ_B can be calculated as

$$\phi_B = V_t \ln\left(\frac{AA^* T^2}{I_s}\right) \quad (4)$$

where A^* is the effective Richardson constant.

The measured I-V curve is shown in Fig. 3.

By fitting Eq. (3) and the measured results ,we can get the parameters of the realized SBDs ,which are shown in Table 1.

Table 1　Parameters of the realized SBD

	Area/μm²	Finger number	I_s/A	R_s/Ω
SBD1	16	10	2×10^{-8}	10
SBD2	1.6	2	5×10^{-9}	90
SBD3	0.64	0	1×10^{-9}	200

From Table 1 , we can observe that with the number of interdigitating fingers increasing ,the series resistance can be reduced evidently.

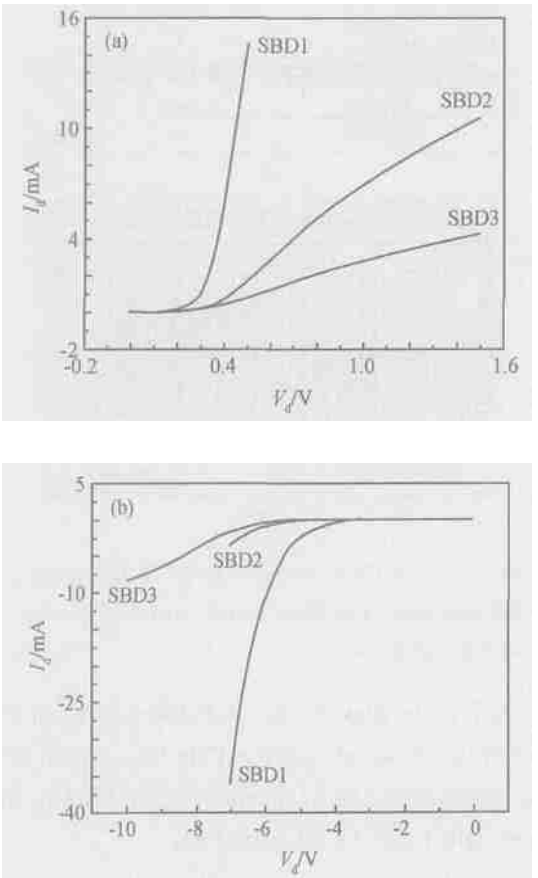

Fig. 3 (a) Measured I-V curves at forward bias; (b) Measured I-V curves at reverse bias Area of SBD1, SBD2, and SBD3 are respectively 16, 1.6, and 0.64μm^2.

The measured statistic result of barrier height ϕ_B for the realized SBD is shown in Fig. 4. There are total 90 samples that have been measured (30 samples for each of SBD1, SBD2, SBD3). And the barrier height of the realized SBD is about 0.44eV.

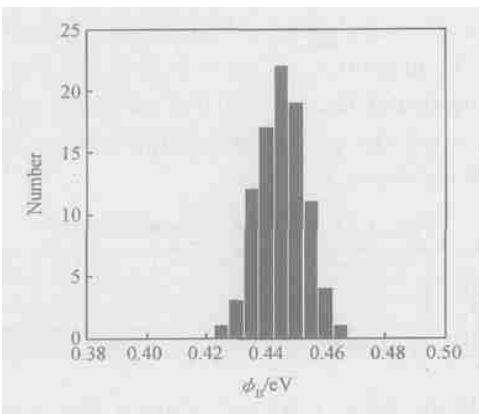

Fig. 4 Statistic result of ϕ_B for the measured SBD (total 90 samples)

The breakdown voltage is about 4.5V. In future work, the breakdown voltage can be extended by some methods that have been used in normal SBD design, such as the fabrication of SBD with self aligned guard ring[8].

3.2 C-V performance

The small signal junction capacitor C_j of Schottky diode is given below,

$$C_j = A\sqrt{\frac{q\varepsilon_s N_d}{2(\phi_B - \phi_n - V)}} \quad (5)$$

where N_d is the doping concentration of the n-well, ϕ_n is the potential difference between the fermi level and the conduction band edge which equals to $(E_C - E_f)/q$.

Figure 5 shows the measured reverse bias C-V curve for SBDs.

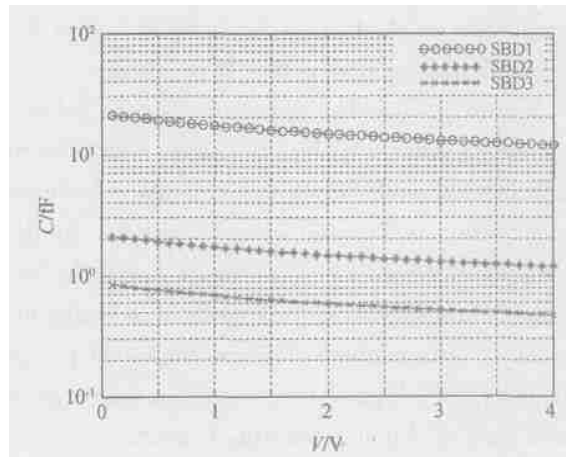

Fig. 5 Measured C-V curve $f = 2.4$GHz

3.3 S parameter measurement and SBD high frequency modeling

In order to measure the high frequency S parameter of the designed devices, each SBD was laid with three probe pads. The size of middle signal pad is 85μm ×85μm and top/bottom ground size is 85μm × 135μm. Using the GSG probe and network analysis instrument, we can get the S parameter of the designed SBD. But the directly measured results of S parameter include the parasitic capacitance of pads, metal line and overlays. For the designed device is very small, these parasitic parameters could not be ne-

glected and must be subtracted from the directly measured *S* parameter by GSG probe. In our works, we fabricated two dummy GSG pads with no tested device. The dummy pads size is the same as that including SBD. One dummy GSG pads' signal is connected with GND called short pad. The other dummy GSG pads' signal is open which is called open pad. The *S* parameter of dummy pads should be measured. Then we can get the parasitic capacitance and resistance of the pad and metal line. And subtracting these parasitic parameter we can get the *S* parameter of SBDs with no parasitic capacitance and resistance. This method is called de-embedding technology[9].

Using the measured *S* parameter, the SPICE model can be abstracted for high frequency simulation. Figure 6 shows the simulation model of the realized SBD. L_1 and L_2 exhibit the input and output serial inductance. C_i and C_o exhibit the anode input and cathode node output capacitance respectively. C_1 exhibits the parasitic capacitance between the interdigitating fingers of Schottky diode's two ports. R_1 and R_2 model for the resistance under the n-well which connects the place under NWLL to ground. The pn diode reflects the parasite n-well-p-sub diode. In our design, the parameter of the pn diode can be gotten from the charted 0.35μm analog CMOS process SPICE model.

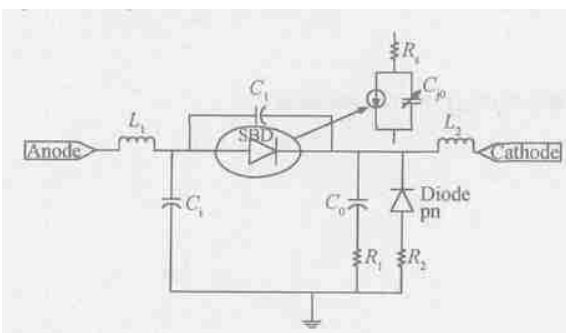

Fig. 6　Simulation model of the realized SBD

Figure 7 shows the measured and simulation *S* parameter of SBD1 (after de-embedding). Table 2 shows the parameter of SBD1 by the simulation model. The frequency is swept from 50MHz to 40GHz. And the model can match the measured results up to 30GHz. Figure 8 shows the photo of realized SBD under probe measurement.

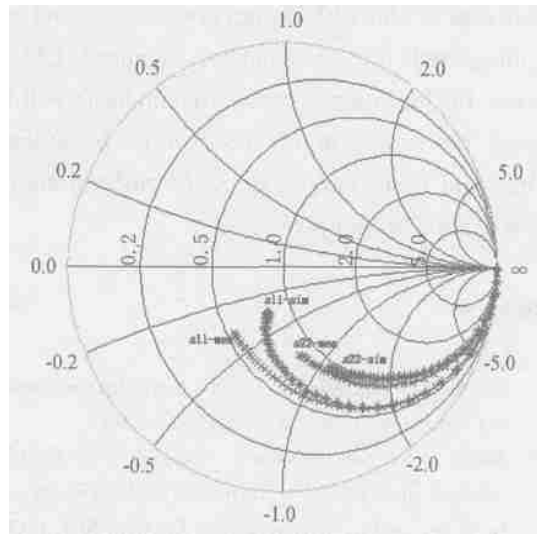

Fig. 7　Measurement and simulation *S* parameter of SBD1 from 50MHz to 40GHz after de-embedding

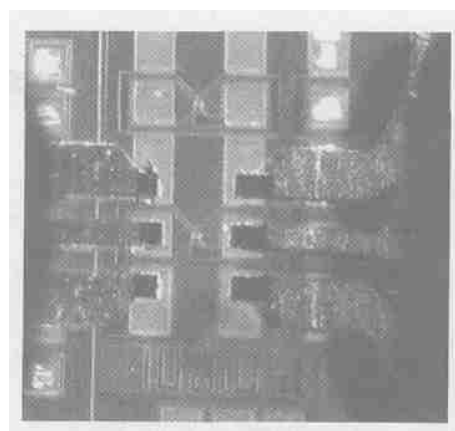

Fig. 8　Photo of the realized SBD under GSG probe measurement

Table 2　Component value of SBD1

L_1	0.005nH	L_2	0.005nH
C_i	0.01pf	C_o	0.05pf
R_1	200Ω	R_2	200Ω
C_1	0.14pf	I_s	2×10^{-8}A
R_s	10Ω	C_{j0}	0.022pf
B_v	4.5V	Nbv	23

4　Conclusion

Fabrication of Schottky barrier diode in standard CMOS process through MPW are performed. The barrier height of the Al-nSi contacts is about 0.44eV. The measured *I-V*, *C-V*, and *S* parameter of the re-

alized SBDs are shown in this paper. The advantages of this SBD design are low cost and can be integrated into commercial standard CMOS process. In the future work, more emphasis will be focused on extension of the reverse breakdown voltage and frequency range of the SBDs designed on standard CMOS process.

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标准 CMOS 工艺集成肖特基二极管设计与实现*

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摘要: 提出了一种在标准 CMOS 工艺上集成肖特基二极管的方法,并通过 MPW 在 charted 0.35μm 工艺中实现. 为了减小串连电阻,肖特基的版图采用了交织方法. 对所设计的肖特基二极管进行了实测得到 *I-V*, *C-V* 和 *S* 参数,并计算得出所测试肖特基二极管的饱和电流、势垒电压及反向击穿电压. 最后给出了可用于 SPICE 仿真的模型.

关键词: CMOS; 肖特基二极管; 集成

EEACC: 2560H; 2570D

中图分类号: TN311^{+}.7 **文献标识码**: A **文章编号**: 0253-4177(2005)02-0238-05

*国家高技术研究发展计划资助项目(批准号:2003AA1Z1280)

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2004-05-24 收到,2004-08-02 定稿