Analysis on Characteristic of Static Induction Transistor Using Mirror Method

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Abstract: A cylindrical gates model of the static induction transistor is proposed and mirror method is used to calculate the distribution of electric potential. The results show that: the potential barrier is directly determined by channel over pinched-off factor; gate efficiency η decreases as the gate dimension α_2 and shifted gate voltage are minished, and what differs from the first-order theory is that η will tend to zero at the shifted gate voltage tends to zero when $V_D = 0$; at low current, the voltage amplification factor μ increases as the drain current rising. When the drain current reaches certain degree, the voltage amplification factor keeps almost constant. In the end, an analytical description of SIT's characteristic suited to both triode-like and mixed I-V characteristics are obtained. The predicted I-V curves are consistent perfectly with the reported experimental ones.

Key words: static induction transistor; mirror method; I-V characteristic

PACC: 0239P

CLC number: TN32 **Document code:** A **Article ID:** 0253-4177(2005)02-0258-08

1 Introduction

Since static induction transistor (SIT) was reported in 1972[1], many works have been done for its structure optimization[2~7], but the theoretical studies on its working mechanism have always been lagged behind practical researches.

SIT is a kind of structurally sensitive device. Its electric parameters and I-V characteristics depend strongly on its structural parameters (such as channel length, channel thickness, etc.), material parameters (such as channel doping concentration), and biasing voltage (V_D and V_G). Generally, SIT's I-V characteristics exhibit triode-like, pentode-like, and mixed between triode- and pentode-like ones. In the past thirty years, some analyses have been done for the basic theoretical model of SIT[8~10]. Bulucea and Rusu followed Shockley's JFET analytical model and proposed a first-order theory of the SIT[8]. Strollo and Spirito developed a self-consistent model using the voltage-doping transformation (VDT) approach[9]. All these results fit well to the triode-like I-V characteristic, but ill-suited to the mixed one.

Our purpose of this work is to (1) propose a cylindrical gates model, work out the distribution of electric field using mirror method, and give a fundamental insight into the mechanisms involved in SIT operation under low biasing voltages; (2) provide a general I-V equation, which is suitable for both of triode-like and mixed I-V characteristics under unipolar SIT operation.

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Received 26 June 2004, revised manuscript received 3 September 2004

2 Model structure

SIT has many types of structure. In this paper we will focus on buried-gate one.

For simplicity, we hypothesize that the gates are cylindrical. The sketched structure of SIT is shown in Fig. 1 (right part). The channel depletion region around the gate and surface charges on the electrodes are also depicted in Fig. 1.

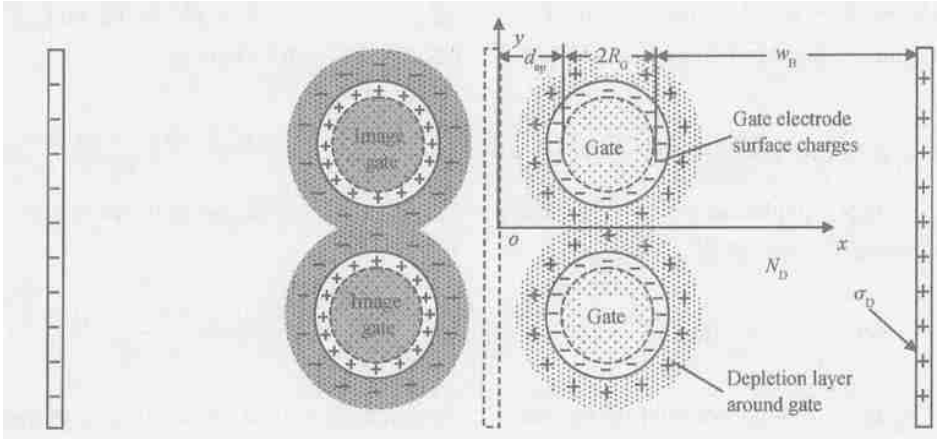

Fig. 1　Analyzing model of SIT

The drain electrode far from the gates is heavily dopped, and the drain surface charge can be regarded as uniform distribution. Also, the study is focused on the channel, we can group the net charges in the long base area with two heads: one is under the depletion layer around the gates; the other is attributed to drain surface charge. Being very close to the gates, the source surface charge can be equivalent to a group of image gates whose polarity is opposite to and whose volume is equal to the gates and their surrounding depletions by using mirror method. Considering charge conversation law, the image drain surface charge should also be calculated. On all these accounts, the analytical model used in this paper is shown in Fig. 1. The main structural dimension and material parameters are given in Table 1.

Table 1　Structural and material parameters of device

Parameter definition	Notation	Value
Channel doping concentration	N_D	$10^{14}cm^{-3}$
Gate doping concentration	N_A	$10^{19}cm^{-3}$
Source doping concentration	n_s	$10^{19}cm^{-3}$
Center distance between two adjacent gates	d	20μm
Width of the long base	w_B	200μm
Radius of the cylindrical gate	R_G	6μm
Thickness of the secondary epitaxial layer	d_{ep}	6μm

3 Potential distribution

Under different biasing voltages, the device can be split into three (the channel is not pinched off) or four subregions (the channel is pinched off) —— gate zone, electrical neutral zone, depletion zone, and depletion-overlapped zone. Considering the symmetry and using superposition principle of the electric field, we can obtain

(1) In gate zone, $(d'_{ep} - x)^2 + (d/2 - y)^2 \leq R_G^2$, the gates can be regarded as an equipotential bulk:

$$\phi(x, y) = V_G - \phi_{BO} \qquad (1)$$

where $\phi_{BO} = V_T \ln \frac{N_A N_D}{n_i^2}$ is gate-channel build-in voltage, V_G is gate voltage.

(2) In electrical neutral zone, $(d'_{ep} - x)^2 + (d/2 - y)^2 \geq R_C^2$, all charges of electrode and depletion region are contributed to the electric field.

$$\phi_1(x,y) = \frac{\sigma_D}{\varepsilon}x + \frac{\lambda'_G}{4\pi\varepsilon}\sum_{n=1/2}\ln\left[\frac{(d'_{ep}-x)^2+(nd-y)^2}{(d'_{ep}+x)^2+(nd-y)^2}\times\frac{(d'_{ep}-x)^2+(nd+y)^2}{(d'_{ep}+x)^2+(nd+y)^2}\right] \quad (2)$$

where σ_D is surface charge density of drain electrode, $\lambda'_G = \lambda_G - \lambda_C$ is general linear density (along z axis) of the gate-channel depletion charge, λ_G is linear density (along z axis) of the gate surface charge, $\lambda_C = qN_D\pi(R_C^2 - R_G^2)$ is linear density (along z axis) of channel depletion charge, $d'_{ep} = d_{ep} + R_G$.

(3) In depletion zone, only part of depletion zone charge affects the electric field. This involves two cases: depletion overlapped and nonoverlapped. For nonoverlapped region, i.e. that of $R_G^2 \leq (d'_{ep}-x)^2 + (d/2-y)^2 \leq R_C^2$ and $(d'_{ep}-x)^2 + (d/2+y)^2 \geq R_C^2$, having:

$$\phi_2(x,y) = \phi_1(x,y) + \frac{qN_D}{4\varepsilon}R_C^2\left[\ln\frac{(d'_{ep}-x)^2+(d/2-y)^2}{R_C^2} + 1 - \frac{(d'_{ep}-x)^2+(d/2-y)^2}{R_C^2}\right] \quad (3)$$

(4) For overlapped depletion region, i.e. that $R_G^2 \leq (d'_{ep}-x)^2 + (d/2-y)^2 \leq R_C^2$ and $(d'_{ep}-x)^2 + (d/2+y)^2 \leq R_C^2$ are met, we have:

$$\phi_3(x,y) = \phi_2(x,y) + \frac{qN_D}{4\varepsilon}R_C^2\left[\ln\frac{(d'_{ep}-x)^2+(d/2+y)^2}{R_C^2} + 1 - \frac{(d'_{ep}-x)^2+(d/2+y)^2}{R_C^2}\right] \quad (4)$$

where λ'_G, σ_D, and R_C can be determined by boundry conditions, i.e.

$$\begin{aligned} &\frac{d\phi(0,0)}{dx} = 0, \\ &\phi(w,0) = V_D, \\ &\phi(d_{ep}, d/2) = V_G - \phi_{BO} \end{aligned} \quad (5)$$

where $w = w_B + 2R_G + d_{ep}$.

4 Barrier height ϕ_{min}

Figure 2 shows a 2D plot of the potential distribution in the device for $V_D = 20$V and $V_G = -3$V. In order to manifest the potential distribution along y-axis, we start from $x = 7\mu$m. It is very clear that a channel barrier occurs along the channel axis and its position x_{min} can be obtained by

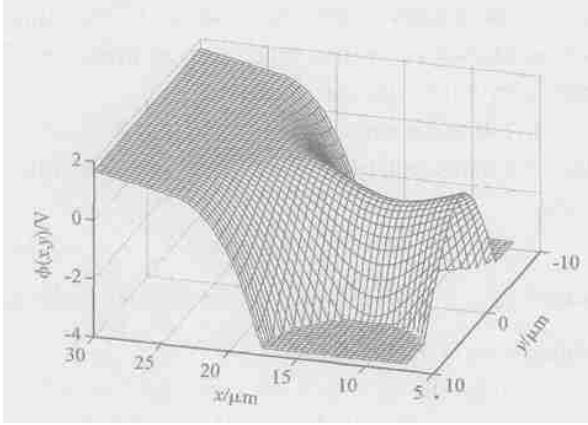

Fig. 2 Two-dimension distribution of the potential obtained from our model for $V_D = 20$V and $V_G = -3$V

$$\frac{d\phi(x,0)}{dx} = 0 \quad (6)$$

When the channel exists in neutral region, equation (6) has no solution. This indicates that the barrier control mechanism occurs only when the channel is pinched-off. Also, the barrier position is the function of biasing voltages. When $V_D = 0$, it is at the center of channel. If V_D is not equal to zero, it will fluctuate from the channel center. We obtain

$$x_{min} = (\alpha_1 - \delta)d \quad (7)$$

where

$$\delta = \frac{B_1 - \sqrt{B_1^2 - 4(A_6 + 4A_3 - 4A_4)(A_3 - A_4)}}{2(A_6 + 4A_3 - 4A_4)} \quad (8)$$

It is a fluctuation from the channel center due to the static induction effect. $B_1 = A_5 + \frac{qN_D d^2}{\varepsilon V_D}(\beta^2 + 2\beta)(A_1 + \alpha_3 A_3)$ is a parameter related to the device structure and biasing voltages, $\alpha_1 = \frac{d'_{ep}}{d}$, $A_1 = \sum_{n=1/2}\left(\ln\frac{(\alpha_3-\alpha_1)^2+n^2}{(\alpha_3+\alpha_1)^2+n^2}\right)$, $A_3 = \sum_{n=1/2}\frac{4\alpha_1}{\alpha_1^2+n^2}$, $A_4 = \sum_{n=1/2}\frac{4\alpha_1}{4\alpha_1^2+n^2}$, $A_5 = \sum_{n=1/2}\left(\frac{2}{n^2} - \frac{2\alpha_1}{4\alpha_1^2+n^2}\right) +$

$\sum_{n=1/2}\left(\frac{4\alpha_1}{4\alpha_1^2+n^2}\right)^2$, $A_6=\sum_{n=1/2}\frac{8\alpha_1}{(4\alpha_1^2+n^2)^2}$ are parameters related to device structure. $\beta\equiv\frac{R_C-d/2}{d/2}$ is channel over pinched-off factor.

Substitute Eq. (7) into Eq. (4), we can obtain the barrier height,

$$\phi_{min}=\frac{V_D\left(\sum_{n=1/2}\ln\frac{\delta^2+n^2}{(2\alpha_1-\delta)^2+n^2}+A_3(\alpha_1-\delta)\right)}{A_1+\alpha_3A_3}+\frac{qN_D}{2\varepsilon}R_C^2\left(\ln\frac{4\delta^2+1}{(1+\beta)^2}+1-\frac{4\delta^2+1}{(1+\beta)^2}\right)\tag{9}$$

where $\alpha_3=w/d$ is a parameter related to device structure.

Figure 3 gives the relationship of barrier height and channel over pinched-off factor under zero voltage of drain. It shows that the potential barrier is directly determined by channel over pinched-off factor. Meanwhile it is necessary of channel deep pinched-off for the forming of barrier high enough to control the drain current.

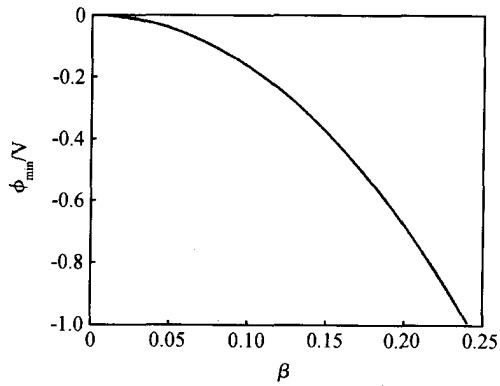

Fig. 3　Relationship of potential barrier height ϕ_{min} and channel over pinch-off factor under zero drain voltage

5　Gate efficiency η and voltage amplification factor μ

Noting that $\frac{\partial\phi_{min}}{\partial\delta}=-d\frac{\partial\phi(x_{min},0)}{\partial x}=0$, the gate efficiency η and voltage amplification factor μ can be obtained:

$$\eta=\frac{\partial\phi_{min}}{\partial V_G}=\frac{(\beta+1)\ln((1+\beta)^2/(4\delta^2+1))}{[1-\ln(2\alpha_2)]\beta-\ln(2\alpha_2)}\tag{10}$$

$$\mu=\left(\frac{1}{\eta}\times\frac{\partial\phi_{min}}{\partial V_D}\right)^{-1}=\left(\sum_{n=1/2}\ln\frac{\delta^2+n^2}{(2\alpha_1-\delta)^2+n^2}+A_3(\alpha_1-\delta)+\frac{(1+\beta)(A_2-(\alpha_1-\alpha_2)A_3)}{[1-\ln(2\alpha_2)]\beta-\ln(2\alpha_2)}\ln\left(\frac{(1+\beta)^2}{1+4\delta^2}\right)\right)^{-1}\times(A_1+\alpha_3A_3)\frac{(1+\beta)\ln((1+\beta)^2/(1+4\delta^2))}{[1-\ln(2\alpha_2)]\beta-\ln(2\alpha_2)}\tag{11}$$

Equations (10) and (11) are the function of biasing voltages and rely on gate dimension α_2 directly. $\alpha_2=\frac{R_G}{d}$, $A_2=\sum_{n=1}\ln\frac{(2\alpha_1-\alpha_2)^2+n^2}{\alpha_2^2+n^2}+\ln\frac{2\alpha_1-\alpha_2}{\alpha_2}$ are the parameters related to the device structure.

Figure 4 gives the dependences of gate efficiency η on shifted gate voltage (V_G-V_P) under different drain voltages and gate dimensions. Here V_P is pinched-off gate voltage for $V_D=0$:

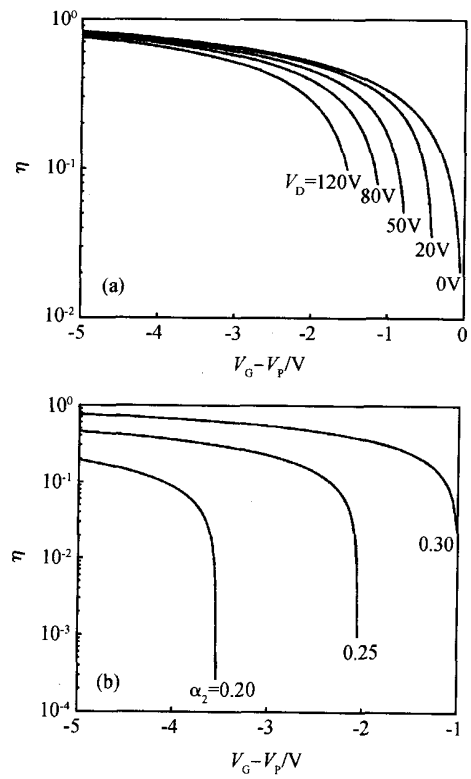

Fig. 4　Dependences of the gate efficiency η on the shifted gate voltage under different drain voltages V_D and different gate dimension α_2　(a) Under different drain voltages for the same α_2; (b) Under different gate dimension for the same V_D

$$V_P = \frac{qN_D d^2}{16\varepsilon} \times (1 - 4\alpha_2^2 + 2\ln(2\alpha_2)) + \phi_{BO} \quad (12)$$

Figure 5 shows that η will decrease when the gate dimension α_2 and shifted gate voltage become less. This result is similar to that of the first-order theory[8]. What differs from the first-order theory is that η will tend to be zero when the shifted gate voltage tends to zero under zero drain voltage. This indicates once more that it is essential of the channel over pinched-off for the barrier control mechanism.

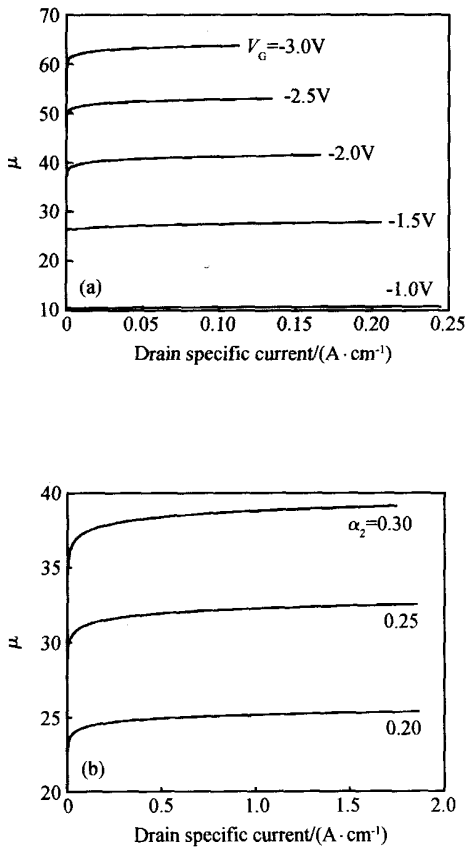

Fig. 5 Dependences of the voltage amplification factor μ on the drain specific current under different V_G and α_2 (a) Under different gate voltages for the same α_2; (b) Under different gate dimension for some β

Figure 5 also gives the dependences of voltage amplification factor μ on specific current of drain under different gate voltage and gate dimensions. At low drain current, the voltage amplification factor μ increases as the drain current rising. When the drain current reaches certain ralue, the voltage amplification factor keeps almost constant. This agrees with the experimental results obtained from buried gate SIT[1].

6 I-V characteristic

The current density along channel axis can be obtained by the following current continuity equation:

$$j_n = q\mu_n n(x) E(x) + D_n \frac{dn(x)}{dx}$$
$$= qD_n\left(\frac{E(x)}{V_T} n(x) + \frac{dn(x)}{dx}\right) \quad (13)$$

The electric field strength along channel axis is given in Fig. 6. Around the center of the channel, the field is nearly linear variation. Considering $E(x_{min},0) = 0$, letting:

$$E(x,0) \approx -V_T\beta_1(x - x_{min}) \quad (14)$$

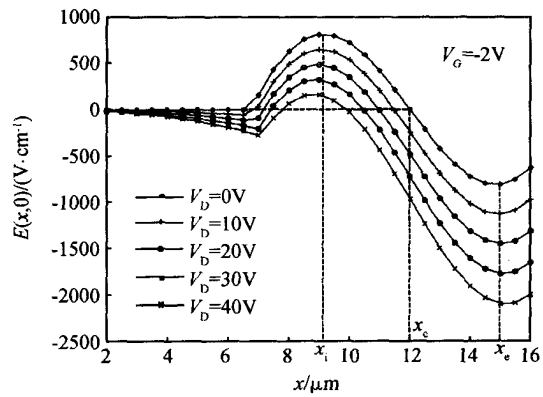

Fig. 6 Electric field strength along channel axis

From Eqs. (13) and (14), we can obtain:

$$n(x) = \left\{\sqrt{\frac{\pi}{2\beta_1}} \times \frac{j_n}{qD_n} Q\left(\sqrt{\beta_1/2}(x - x_{min})\right) + n_0\right\} \times e^{\beta_1(x - x_{min})^2/2} \quad (15)$$

where n_0 is electron concentration at the barrier ($E = 0$). It is determined by the boundary condition. Using Boltzmann approximation, we have:

$$n_0 = n(x_{min}) = n_s e^{\phi_{min}/V_T} \quad (16)$$

Q is error function, $\beta_1 = \dfrac{(A_3 - A_4) V_D}{(A_1 + \alpha_3 A_3) d^2 V_T(\alpha_1 - \delta)}$ is a new introduced parameter.

At the end of the channel (that is $x = x_e$, see

Fig. 6) ,drift field is so high that the carriers are hard to accumulate , so the carrier concentration gradient inclines to zero. Then we can obtain :

$$j_n = -qD_n\left(\sqrt{\frac{\pi}{2\beta_1}}\,Q\left(\sqrt{\beta_1/2}\,(x_e - x_{min})\right) + \frac{e^{-\beta_1(x_e-x_{min})^2/2}}{\beta_1(x_e - x_{min})}\right)^{-1} n_s e^{\phi_{min}/V_T} \quad (17)$$

Following the analysis reported in Ref. [10] ,the effective half channel thickness a_{eff} can be written as

$$a_{eff} \equiv \frac{I_n}{2 j_n w_t} = \int_0^{y_2} \exp\left(\frac{\phi(x_{min}, y) - \phi_{min}}{V_T}\right) dy \quad (18)$$

where I_n is the drain current , w_t is the total width of channel , y_2 is half minimum of cross section of channel. Then

$$2a_{eff} = \sqrt{\frac{\pi}{B_5}}\,dQ\left(\frac{\sqrt{B_3}\,y_1}{d}\right) + \sqrt{\frac{\pi}{B_4}}\,d \times \left(Q\left(\sqrt{B_4}\left(\frac{y_2}{d} + \frac{B_5}{B_4}\right)\right) - Q\left(\sqrt{B_4}\left(\frac{y_1}{d} + \frac{B_5}{B_4}\right)\right)\right) \quad (19)$$

where $y_1 = \sqrt{R_C^2 - (d'_{ep} - x_{min})^2} - \frac{d}{2}$, $y_2 = \frac{d}{2} - \sqrt{R_G^2 - (d'_{ep} - x_{min})^2}$, $B_2 = \frac{A_5 V_D/V_T}{2(A_1 + \alpha_3 A_3)}$, $B_3 = B_2 + \frac{2qN_D}{\varepsilon V_T}(R_C^2 + \frac{d^2}{4})$, $B_4 = B_2 + \frac{qN_D}{\varepsilon V_T}(R_C^2 + \frac{d^2}{4})$, $B_5 = \frac{qN_D}{\varepsilon V_T}(R_C^2 - \frac{d^2}{4})$ are parameters related to the device structure and biasing voltages.

Using above equations , the I-V characteristics under different gate voltages are obtained and shown in Fig. 7 : (a) is a typical group of mixed I-V characteristic curves and (b) is a group of triode-like ones.

The error function has the properties of $Q(x) \xrightarrow{x \geq 3} 1$ and $Q(x) \xrightarrow{x \to \infty} 0$. If the reverse gate voltage is high , the channel is deep pinched off , $\frac{\sqrt{B_3}\,y_1}{d} \geq 3$ and $\sqrt{\frac{\beta_1}{2}}(x_e - x_{min}) \geq 3$ are met , Equations (17) and (19) can be simplified to

$$j_n \approx -qD_n\sqrt{\frac{2\beta_1}{\pi}}\,n_s e^{\phi_{min}/V_T} \quad (20)$$

$$2a_{eff} = \sqrt{\frac{\pi}{B_3}}\,d \approx \left(\frac{2qN_D}{\pi\varepsilon V_T}(R_C^2 + \frac{d^2}{4})\right)^{-1/2} d \quad (21)$$

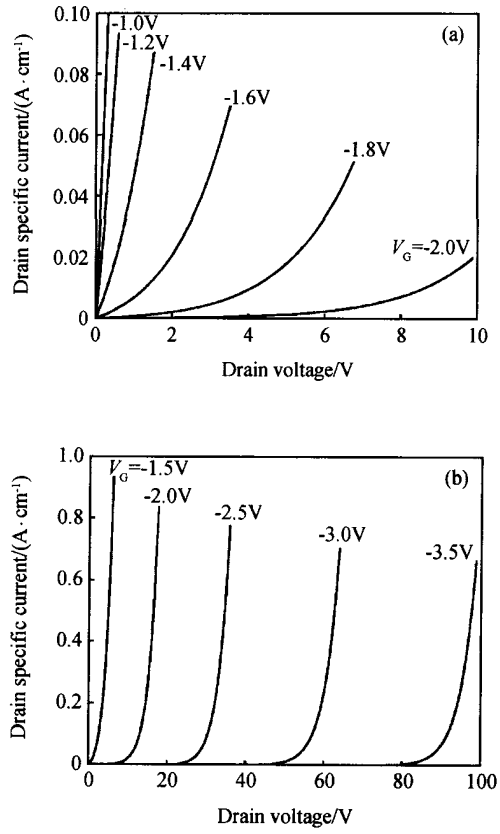

Fig. 7　Calculated I-V characteristic of SIT　(a) Mixed characteristics under lower gate voltage ; (b) Triode-like characteristics under higher gate voltages

Then

$$I_n \approx -2w_t qD_n\sqrt{1 - \frac{d^2/2}{R_C^2 + d^2/4}}\,n_s e^{\phi_{min}/V_T} \equiv -I_0 e^{\phi_{min}/V_T} \quad (22)$$

where the pre-exponential factor $I_0 = 2w_t qD_n \times \sqrt{1 - \frac{d^2/2}{R_C^2 + d^2/4}}\,n_s$ (the so called saturation current) is almost constant with V_D.

If channel pinched off degree is low , $Q\left(\sqrt{\beta_1/2}\,(x_e - x_{min})\right) \ll \frac{e^{-\beta_1(x_e-x_{min})^2/2}}{\beta_1(x_e - x_{min})} \approx -\frac{1}{E_{max}}$ and $\sqrt{B_4}\,\frac{y_1}{d} \to 0$, Euqations (17) , (19) and drain current can be simplified to

$$j_n \approx q\mu_n E_{max} n_s e^{\phi_{min}/V_T} \quad (23)$$

$$2a_{eff} \doteq \sqrt{\frac{\pi}{B_4}}\,d \approx \sqrt{\frac{\pi}{B_2}}\,d \quad (24)$$

$$I_n \approx -w_t q\mu_n n_s e^{\phi_{min}/V_T}\sqrt{\frac{\pi A_5 V_T \beta V_D}{3(A_1 + \alpha_3 A_3)}} \quad (25)$$

From Eqs. (20), (22), (23), and (25), we can see that, when the pinched-off degree of channel is deep, the current flowing through the channel is mainly by diffusion, the so called saturation current is almost constant with V_D, the device exhibits exponential I-V characteristics; when the pinched-off degree of channel is low, the current flowing through the channel is mainly by drifting, the so called saturation current is almost 1/2 power with V_D, the device exhibits mixed I-V characteristics.

7 Conclusion

Basing on cylindrical gates model, the distribution of channel potential has been calculated directly by mirror method. Two opposite action fields in the channel are obtained and the saddle resembled potential distribution is gotten. In addition, we have proposed the concept of channel over pinch-off factor β and pointed out definitely that it is essential that the channel over pinched-off for the barrier control mechanism. Moreover, the forming of potential barrier relies on channel over pinched-off; and the controlling of barrier height lies in channel over pinched-off factor.

Meanwhile, the gate efficiency and voltage amplification factor are given. Both of them are gate dimension a_2 related parameters. The more a_2 is, the more η and μ are.

Though this model is under the assumption that the channel overlapped depletion zone is much less than the total depletion zone, it still has great help to understand the mechanism of SIT. It works well for the analysis of the SIT which has mixed I-V characteristics. And using this model, we have presented a group of I-V characteristic curves, which fits quite well to the experimental result published up to now[1~3]. This confirms further that our model is correct and available.

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镜像法分析静电感应晶体管特性

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摘要：针对埋栅型静电感应晶体管(SIT)提出一种柱栅模型.用镜像法计算了器件内电势分布,并在此基础上计算了沟道势垒、栅效率、电压放大因子等.结果表明:沟道势垒直接取决于沟道过夹断因子;栅效率随栅尺寸和位移栅压的减小而减小,并随位移栅压一起趋向于 0;在小电流情况下电压放大因子随电流的增大而增大,到一定数值后,电压放大因子趋于常数.最后给出了 SIT *I*-*V* 特性解析表达式,它既适用于类三极管特性(加大栅压下)也适用于混合特性(较小栅压下),且由此得到的 *I*-*V* 特性曲线和实验符合较好.

关键词：静电感应晶体管；镜像法；*I*-*V* 特性

PACC：0239P

中图分类号：TN32　　**文献标识码**：A　　**文章编号**：0253-4177(2005)02-0258-08

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2004-06-26 收到,2004-09-03 定稿