Fabrication of Ultrathin SiO_2 Gate Dielectric by Direct Nitrogen Implantation into Silicon Substrate *

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Abstract: Nitrogen implantation in silicon substrate at fixed energy of 35keV and split dose of 10^{14}～$5\times10^{14}cm^{-2}$ is performed before gate oxidation. The experiment results indicate that with the increasing of implantation dose of nitrogen, oxidation rate of gate decreases. The retardation in oxide growth is weakened due to thermal annealing after nitrogen implantation. After nitrogen is implanted at the dose of $2\times10^{14}cm^{-2}$, initial O_2 injection method which is composed of an O_2 injection/ N_2 annealing/ main oxidation, is applied for preparation of 3.4nm gate oxide. Compared with the control process, which is composed of N_2 annealing/ main oxidation, initial O_2 injection process suppresses leakage current of the gate oxide. But Q_{bd} and HF C-V characteristics are almost identical for the samples fabricated by two different oxidation processes.

Key words: ultrathin gate dielectric; nitrogen implantation; breakdown

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1 Introduction

As channel length of MOS transistors is reduced to 0.1μm, thickness of gate oxide has to be decreased to overcome short channel effect. But oxide quality has to be maintained in addition to ultrathin thickness. Nitrogen incorporated oxide seems to satisfy this requirement. Nitrogen has a useful feature in growing ultrathin gate oxide such as reduced oxidation rate and prevention of boron penetration[1,2]. Furthermore, nitrogen has an advantage of preventing degradation of transistor characteristics due to hot carriers created during the device operation. The general methods to incorporate nitrogen into oxide are oxidation in N_2O or NO ambient[3,4]. But they have difficulties in incorporating a large amount of nitrogen into oxide in ultrathin gate oxide regime. In such processes furnace oxidation time should be lengthened to gain higher nitrogen concentration, which results in a thicker oxide. Meanwhile, the techniques are performed in high temperature, which may limit the process window and complicate gate oxide process. Nitrogen implantation into polysilicon gate followed by thermal annealing is another attempt to form nitrided oxide[5～7]. But most of the nitrogen incorporated by this mean exists in bulk oxide and has no efficiency on improvement of Si/ SiO_2 interface quality.

In this work, nitrogen was implanted in the substrate before gate oxidation to fabricate ultrathin gate oxide, which eliminates these above problems. Nitrogen implantation in the silicon substrate was performed at the fixed energy of 35keV and with the split dose of 10^{14}～$5\times10^{14}cm^{-2}$, and the nitrogen

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profile and the effect of thermal annealing on it were examined by secondary ion mass spectroscopy (SIMS). The effects of profile and dose of nitrogen on gate oxide thickness were studied. Initial O_2 injection method composed of O_2 injection/ N_2 annealing/ main oxidation was applied for gate oxidation. The reliability of 3.4nm gate oxide prepared by this method was investigated by *I-V*, *C-V*, Q_{bd}, and SILC characteristics of MOS capacitors.

2 Experiment

All experiments were performed on n-type (100) silicon substrates with a relative resistivity of 2～4Ω·cm. And oxide thicknesses were measured by ellipsometry in the experiments.

Figure 1 shows key process and split conditions to form thin oxides on nitrogen-implanted silicon. The wafers were SPM cleaned, and a 40nm dry O_2 screen oxide was grown on the substrates prior to N_2^+ implantation. Some samples underwent high temperature annealing before removal of the screen oxide. After screen oxide was stripped and SPM cleaning was performed, thin oxides were prepared in O_2/ N_2 ambient at 950 ℃. Control wafers that were not implanted by nitrogen were also fabricated.

Figure 2 is process flow for preparation of gate oxides of MOS capacitor samples. Nitrogen implantation has been performed at 35keV and with the dose of $2\times10^{14}cm^{-2}$ through a 40nm dry O_2 screen oxide. The initial O_2 injection method was used to grow gate oxide after the removal of screen oxide. First, oxidation at 650 ℃ for very short time was done to form an extremely thin oxide layer that provides a Si/ SiO_2 interface. Then the annealing process was performed from 650 ℃ to 850 ℃ in N_2 ambient for 20min to pile up the nitrogen at the Si/ SiO_2 interface from substrate. Finally, gate oxides were grown at 850 ℃ in O_2/ N_2 ambient. Control samples were grown by conventional method for comparison. The difference between the initial O_2 injection method and the conventional method was with and without O_2 injection at the initial gate oxidation stage. After gate oxidation,

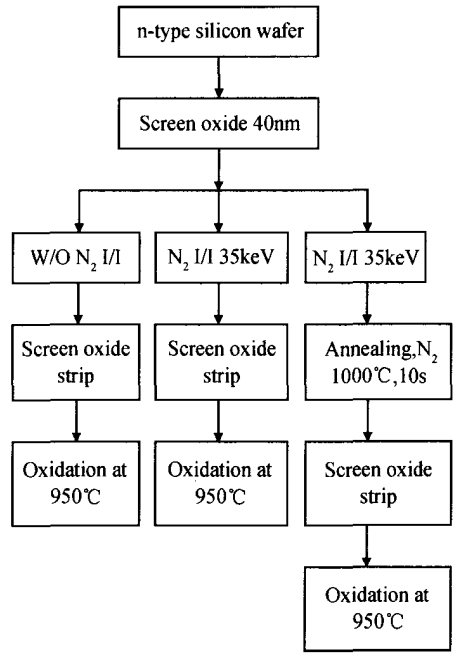

Fig. 1 Key process and split conditions to form thin oxides on nitrogen implanted silicon

250nm polysilicon was deposited and doped with BCl_3.

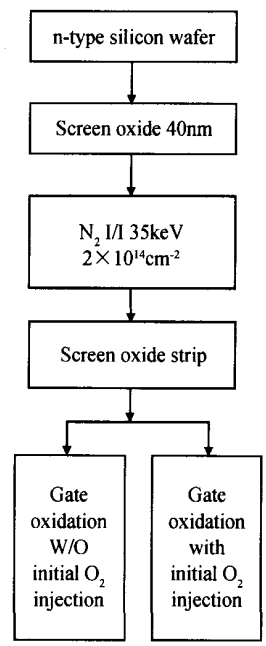

Fig. 2 Process flow for preparation of gate oxides used in MOS capacitors

3 Results and discussion

3.1 Oxidation retardation effect

Table 1 summarizes the oxide thickness for samples fabricated by process showed in Fig. 1. For samples without thermal annealing after N_2^+ implantation, oxidation retardation effect was observed at a N_2^+ dose as low as $10^{14}cm^{-2}$, and it was

Table 1 Oxide thickness and growth rate reduction for various N_2^+ I/I doses after oxidation at 950 ℃ for 10min

N_2^+ I/I dose / $10^{14}cm^{-2}$	Gate oxide thickness / nm	Growth rate reduction / %
0	5.5	Reference point
1	4.9	11
2	4.4	20
5	3.5	36
5 *	5.5	0

* The sample is annealed in N_2 ambient at 1000 ℃ for 10s before screen oxide removal.

enhanced with increase of N_2^+ dose. With a N_2^+ dose of 10^{14}～$5\times10^{14}cm^{-2}$, the growth rate is reduced by as much as 11 %～36 %. But retardation effect did not appear if thermal annealing in N_2 ambient at 1000 ℃ for 10s was performed after N_2^+ implantation. It seems that the retardation in oxide growth was more pronounced for the samples without thermal annealing, which coincides with the result of Ref. [8]. We attempt to explain it by nitrogen concentration profile which was obtained by SIMS analysis and showed in Fig. 3. It could be seen that nitrogen was piled up at the Si/SiO_2 interface after that thermal annealing. Defects at Si/SiO_2 interface which could trap nitrogen atoms during the thermal annealing may be the reason for the piling up. It was supposed that the nitrogen-rich layer formed by the piling up of nitrogen after thermal annealing was extremely thin and just existed in transition layer at Si/SiO_2 interface, so some nitrogen was lost during the removal of screen oxide. Then thermal annealing before screen oxide removal made nitrogen concentration lower than that of implanted, and the oxidation retardation effect arisen from nitrogen was weakened. It needs more experiments to confirm the hypothesis. The optimized thermal annealing process that can eliminate some structural damage induced by N_2 implantation should be proposed to satisfy for the requirement of oxidation retardation.

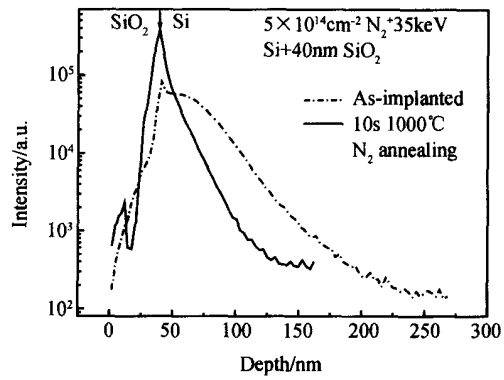

Fig. 3 Nitrogen SIMS profile in the Si/SiO_2 double layer

3.2 3.4nm gate oxide properties

Figure 4 plots the current voltage characteristics to compare the two gate oxides prepared by initial O_2 injection method and by conventional method showed in Fig. 2. It could be seen that sample with initial O_2 injection has lower leakage current than that without it. Stress induced leakage current (SILC) is an increase in oxide leakage current at low field after a high field electrical stress. After samples were stressed at the oxide field of 10MV/cm for certain time, and SILC was monitored at the oxide field of 5MV/cm under positive gate bias. The results are shown in Fig. 5. SILC appears to be lowered by the application of initial O_2 injection method. Nitrogen at Si/SiO_2 interface can replace strained Si—O bonds, Si—H, and Si—OH weak bonds at the interface by Si—N bonds, which thus improves the interface quality and decreases the amount of defects and traps induced by electrical stress. Initial O_2 injection accumulates nitrogen from the silicon substrate to the Si/SiO_2 interface before the main oxidation, resulting in higher nitrogen peak concentration at the interface.

The high frequency C-V characteristics and Q_{bd} measured at constant current stress and positive gate

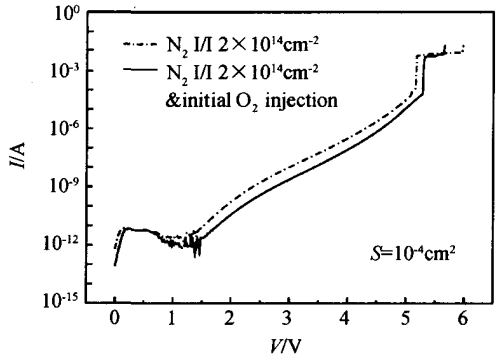

Fig. 4　Leakage current of gate oxide versus gate voltage　T_{ox} (with initial O_2 injection) = 3.4nm, T_{ox} (without initial O_2 injection) = 3.3nm

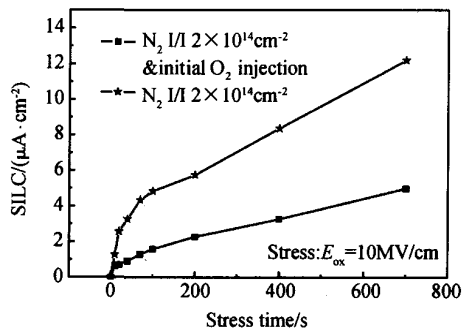

Fig. 5　SILC versus stressing time　T_{ox} (with initial O_2 injection) = 3.4nm, T_{ox} (without initial O_2 injection) = 3.3nm

bias are presented in Figs. 6 and 7 respectively. There is no obvious difference for 3.4nm gate oxide prepared by the initial O_2 injection method and by the control method.

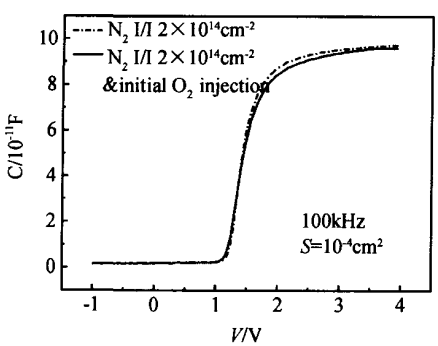

Fig. 6　HF *C-V* characteristics of with initial O_2 injection (a) and without initial O_2 injection (b) p^+ gate MOS capacitor　T_{ox} (with initial O_2 injection) = 3.4nm, T_{ox} (without initial O_2 injection) = 3.3nm

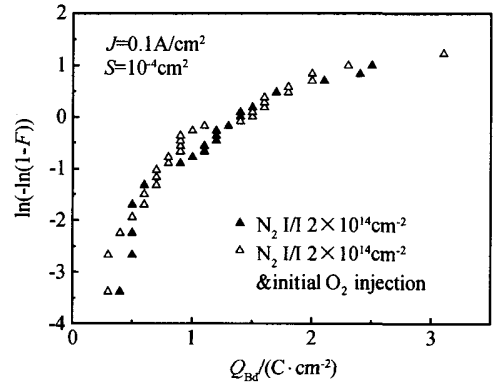

Fig. 7　Q_{bd} distributions of gate oxides prepared by initial O_2 injection method and conventional method　T_{ox} (with initial O_2 injection) = 3.4nm, T_{ox} (without initial O_2 injection) = 3.3nm　p^+ gate MOS capacitors with active areas of $10^{-4}cm^{-2}$ were used.

4　Conclusion

By implanting nitrogen in the substrate before growing thin gate oxides, we found that oxidation retardation effect resulted from nitrogen existence at Si/SiO_2 interface is enhanced with the increase of nitrogen dose and is weakened by thermal annealing in N_2 ambient at 1000 ℃for 10s.

3.4nm gate oxide was fabricated on the nitrogen implanted silicon substrate with initial O_2 injection before main gate oxidation. The experimental results show that initial O_2 injection method improves *I-V* and SILC characteristics of the gate oxide because it could pile up more nitrogen at Si/ SiO_2 interface.

References

[1] Liu C T, Lloyd E J, Ma Yi, et al. High performance 0.2μm CMOS with 2.5nm gate oxide grown on nitrogen implanted Si substrates. IEDM, 1996: 499

[2] Chen Y Y, Liu I M, Gardner M, et al. Performance and reliability assessment of dual-gate CMOS devices with gate oxide grown on nitrogen implanted Si substrate. IEDM, 1997: 639

[3] Lai P T, Xu J P, Cheng Y C. Interface properties of NO-annealed N_2O-grown oxynitride. IEEE Trans Electron Devices, 1999, 46 (12): 2311

[4] Aoyama T. Ohkubo S, Tashiro H, et al. Boron diffusion in nitrided-oxide gate dielectrics leading to high suppression of boron

penetration in p-MOSFETs. Jpn J Appl Phys, 1998, 37(3B): 1244

[5] Krisch K S, Green M L, Baumann F H, et al. Thickness dependence of boron penetration through O_2- and N_2O-grown gate oxides and its impact on threshold voltage variation. IEEE Trans Electron Devices, 1996, 43(6): 982

[6] Herden M, Bauer A J, Ryssel H. Suppression of boron penetration through thin gate oxides by nitrogen implantation into the gate electrode of pMOS devices. Microelectronics Reliability, 2000, 40(4/5): 633

[7] Wang Yanfeng, Liu Zhongli. Characteristics of thin gate oxide nitrided by implantation. Chinese Journal of Semiconductors, 2001, 22(7): 881(in Chinese) [王延峰, 刘忠立. 离子注入氮化薄 SiO_2 栅介质的特性. 半导体学报, 2001, 22(7): 881]

[8] Soleimani H R, Doyle B S, Philipossian A. Formation of ultrathin nitrided SiO_2 oxides by direct nitrogen implantation into silicon. J Electrochem Soc, 1995, 142(8): L132

硅衬底注氮方法制备超薄 SiO_2 栅介质*

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摘要: 利用栅氧化前在硅衬底内注氮可抑制氧化速率的方法,制得 3.4nm 厚的 SiO_2 栅介质,并将其应用于 MOS 电容样品的制备. 研究了 N^+ 注入后在 Si/SiO_2 中的分布及热退火对该分布的影响;考察了不同注氮剂量对栅氧化速率的影响. 对 MOS 电容样品的 *I-V* 特性,恒流应力下的 Q_{bd},SILC 及 *C-V* 特性进行了测试,分析了不同氧化工艺条件下栅介质的性能. 实验结果表明:注氮后的热退火过程会使氮在 Si/SiO_2 界面堆积;硅衬底内注入的氮的剂量越大,对氧化速率的抑制作用越明显;高温栅氧化前进行低温预氧化的注氮样品较不进行该工艺步骤的注氮样品具有更低的低场漏电流和更小的 SILC 电流密度,但二者恒流应力下的 Q_{bd}值及高频 *C-V* 特性相近.

关键词: 超薄栅介质; 氮离子注入; 击穿特性

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