A Systematical Approach for Noise in CMOS LNA

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Abstract : A systematic approach is used to analyze the noise in CMOS low noise amplifier (LNA) ,including channel noise and induced gate noise in MOS devices. A new analytical formula for noise figure is proposed. Based on this formula ,the impacts of distributed gate resistance and intrinsic channel resistance on noise performance are discussed. Two kinds of noise optimization approaches are performed and applied to the design of a 5. 2GHz CMOS LNA.

Key words : amplifier noise ; channel noise ; channel resistance ; induced gate noise ; low noise amplifier ; noise optimization

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1 Introduction

The progress in CMOS process makes it possible to integrate more functions on one chip ,including radio frequency front-end and digital signal processing back-end. WLAN (wireless local area network) transceiver is one of these digital communication systems , which connects laptops and other mobile terminals to ethernet backbone through AP (access point) . As MAC (media access control) part of WLAN transceiver is implemented in CMOS technology ,it is appealing to implement the RF front-end circuit in the same technology. It is promising to integrate the whole system on a single chip.

As the first critical component of the receiver , low noise amplifier (LNA) should sufficiently amplify the weak RF signal coming from antenna and duplexer with as less distortion and noise as possible. From the Friis noise equation[1] ,the noise figure of the receiving system is dominated by the noise contribution of the first stage or two.

The source inductive degeneration configuration is widely used for LNA due to its superior noise performance[2] . This LNA architecture has been analyzed[3] especially on noise performance. There are three main noise sources , which should be taken into consideration to fully appreciate the noise performance. One is the noise associated with the distributed gate resistance and other losses in series with the gate ; the others are induced gate noise and channel noise in submicron MOS devices due to hot electron effects. The analysis in Ref. [3] dealt with the contribution of each noise source separately ,thus the interactions among these components were neglected. The correlation between induced gate noise and channel noise was not treated rigidly in mathematics. The induced gate noise was simply split into two components ,one of which is fully correlated with the channel noise and the other is uncorrelated with the channel noise[3] . Although this technique simplified the analysis ,it was just a conjecture without proof. Only the amplitude of the correlation coefficient , which is a complex number ,was considered. As frequency approaching cut-off frequency f_T , the gate impedance of the MOS device exhibits a significant phase shift from its purely capacitive value at lower frequencies. In the RF applications ,the channel of MOSFET must

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be viewed as a bias dependent RC distributed transmission line[4]. To model the finite time needed to build up the channel charge, one way is to insert a noiseless equivalent resistors R_{ch} in series with the gate capacitors C_{gs} and C_{gd}, respectively[5]. The existence of R_{ch} was verified through simulation and measurement[6]. Meanwhile R_{ch} complicates the analysis of noise figure, and its effect on noise performance was dropped out[3]. This was noted in Ref. [7], but the analysis there is a simple extension of the results in Ref. [3] and is not accurate and rigor in mathematics.

To fully appreciate the noise performance of CMOS LNA, a comprehensive analysis is presented in this paper. The noise performance of source inductive degeneration CMOS LNA is analyzed and a new analytical formula for noise figure is derived. Two approaches of noise optimization are performed with respect to fixed transconductance gain G_m and fixed power dissipation P_D, respectively, and they are applied in the design of a 5.2GHz CMOS LNA.

2 CMOS LNA noise analysis

The CMOS LNA analyzed here is the source inductive degeneration architecture (Fig. 1) for its superior noise performance and prevalence.

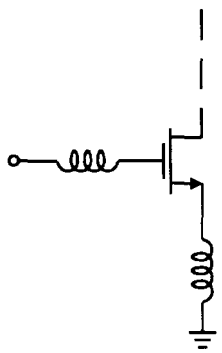

Fig. 1 Source inductive degeneration LNA architecture

To perform a comprehensive noise analysis of the LNA with a systematic approach, a generic small-signal model of source inductive degeneration LNA is used. The small-signal model is shown in Fig. 2. The parasitic components between gate and drain are not shown in Fig. 2, as there are methods (such as cascode configuration) to improve reverse-isolation. Z_g denotes the impedance in series with the gate. Z_{gs} is the impedance between the gate and the source including parasitic C_{gs} and channel resistance R_{ch}. Z_s and Z_L are the source degeneration and load impedances of the LNA, respectively. g_m is the transconductance of the MOS device.

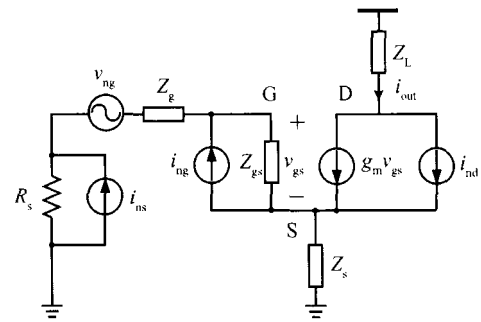

Fig. 2 Generic small-signal model for LNA noise analysis

i_{ns} is the noise current source associated with source resistance R_s. Three main noise sources are fully considered here. v_{ng} is the noise voltage source associated with gate impedance Z_g which includes distributed gate resistance and other parasitic losses. In RF CMOS circuits, transistors are commonly implemented with multi-finger gate layout. The PSD (power spectral density) of v_{ng} is given by

$$\overline{v_{ng}^2} = 4kT\frac{R_g}{3}\Delta f \qquad (1)$$

where the factor of 1/3 is due to the distributed effect of the gate resistance, assuming the fingers are only contacted at one end[8]. If both ends are contacted, the factor is reduced to 1/12. i_{nd} is channel noise source, which is the dominant noise source in MOS device. i_{nd} is white noise, the PSD of which is given by

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \qquad (2)$$

where γ is a bias-dependent factor, and g_{d0} is the zero-bias drain conductance of the MOS device. i_{ng} is induced gate noise source, the PSD of which is given by[9]

$$\overline{i_{ng}^2} = 4kT\delta\frac{\omega^2 C_{gs}^2}{5g_{d0}}\Delta f \tag{3}$$

where δ is the coefficient of gate noise. This equation is valid when the device is operated in saturation. i_{ng} is induced by the fluctuations in the channel charge due to capacitive coupling when MOS device is biased so that the channel is inverted. Thus i_{ng} and i_{nd} are partially correlated, and the correlation coefficient is given by[9]

$$c = \frac{\overline{i_{ng}\, i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}\,\overline{i_{nd}^2}}} \tag{4}$$

where asterisk (*) indicates the conjugate of complex number. It is worth noting that the choice of directions of correlated noise sources has effect on the phase of the correlation coefficient c. The value of c for long-channel devices is 0.395j.

Applying the noisy two-port network based analysis outlined in Ref. [10], the input impedance and noise factor F of the source degeneration LNA are given by

$$Z_{in} = Z_g + Z_{gs} + Z_s + g_m Z_{gs} Z_s \tag{5}$$

$$F = 1 + \frac{\overline{v_{ng}^2}}{R_s^2\,\overline{i_{ns}^2}} + |A|^2\frac{\overline{i_{ng}^2}}{\overline{i_{ns}^2}} + |B|^2\frac{\overline{i_{nd}^2}}{\overline{i_{ns}^2}} + 2\frac{\mathrm{Re}(AB^*\,\overline{i_{ng}\, i_{nd}^*})}{\overline{i_{ns}^2}} \tag{6}$$

$$A = 1 + \frac{Z_g + Z_s}{R_s}$$

$$B = \frac{1}{g_m Z_{gs}}\left(1 + \frac{Z_g + Z_{gs} + Z_s}{R_s}\right)$$

where it is assumed that v_{ng} is uncorrelated with i_{nd} and i_{ng}. It is worth noting that the load impedance Z_L does not appear in the noise factor expression, because the reverse path between gate and drain has been disregarded.

For the source inductive degeneration LNA considered here, the explicit expressions for Z_g, Z_{gs}, and Z_s are

$$\begin{cases} Z_g = j\omega L_g + R_g \\ Z_{gs} = R_{ch} + \dfrac{1}{j\omega C_{gs}} \\ Z_s = j\omega L_s \end{cases} \tag{7}$$

where R_g includes the distributed gate resistance and loss of inductor L_g. R_{ch} is the noiseless equivalent channel resistance to model the deviation of gate impedance of MOS device from its purely capacitive value at lower frequencies as operating frequency approaching ω_T. The expression of R_{ch} is

$$R_{ch} = \frac{1}{5g_{d0}} \tag{8}$$

assuming that operating frequency ω_0 satisfies

$$\omega_0 \ll \frac{5\omega_T}{\alpha} \tag{9}$$

with the definition that

$$\alpha = \frac{g_m}{g_{d0}} \tag{10}$$

Note that α is always less than one.

From Eq. (5), the impedance matching input and the corresponding resonant frequency ω_0 are determined by

$$\begin{aligned} R_s &= R_g + R_{ch} + g_m\frac{L_s}{C_{gs}} \\ \omega_0 &= \frac{1}{\sqrt{C_{gs}\left[L_g + L_s\left(1 + \dfrac{\alpha}{5}\right)\right]}} \end{aligned} \tag{11}$$

The impact of neglecting R_{ch} on input impedance matching and intended operating frequency can be appreciated from Eq. (11).

Substituting Eqs. (1) ~ (4) and (7) into Eq. (6), the noise factor F of source inductive degeneration LNA can be explicitly given by

$$F = 1 + F_1 + F_2 + F_3 + F_4$$

$$F_1 = \frac{R_g}{3R_s}$$

$$F_2 = \left(\frac{\omega_0}{\omega_T}\right)^2\frac{\delta g_{d0}\alpha^2}{5R_s}[(R_s + R_g)^2 + \omega_0^2(L_g + L_s)^2]$$

$$F_3 = \frac{\gamma g_{d0}\left(\dfrac{\omega_0}{\omega_T}\right)^2}{1 + \left(\dfrac{\omega_0}{\omega_T}\right)^2\times\dfrac{\alpha^2}{25}}\times\frac{(R_s + R_g + R_{ch})^2 + \omega_0^2 L_s^2\dfrac{\alpha^2}{25}}{R_s}$$

$$F_4 = \left\{\frac{\left(\dfrac{\omega_0}{\omega_T}\right)^2 g_m^2}{1 + \left(\dfrac{\omega_0}{\omega_T}\right)^2\times\dfrac{\alpha^2}{25}}[(R_s + R_g)^2 + \omega_0^2(L_g + L_s)^2] - \frac{L_g + L_s}{L_g + L_s\left(1 + \dfrac{\alpha}{5}\right)}\right\}\times\frac{2|c|}{g_m R_s}\sqrt{\frac{\delta}{5}} \tag{12}$$

F_1 is due to the distributed gate resistance only where the noise contribution of loss in L_g has been disregarded. F_2 and F_3 are attributed to induced

gate noise and channel noise, respectively. F_4 is due to the correlation between induced gate noise and channel noise. During the derivation, some assumptions have been made

$$\omega_T \approx \frac{g_m}{C_{gs}} \qquad (13)$$
$$c = |c| \mathrm{j}$$

From the explicit noise factor expression, it is clear that gate resistance R_g increases noise factor through F_2, F_3, and F_4 in addition to its direct contribution to F. This has been ignored in the previous work[3,7], where the noise sources are treated individually for simplicity. Multi-finger gate layout and salicide CMOS process can alleviate this plague without power penalty. Another conclusion is that L_g should be implemented with bond wire and external high-Q inductor instead of on-chip spiral inductor if lower NF is desirable, because the loss of on-chip spiral inductor is larger. Even if on-chip spiral inductor is used for higher integration, the AC coupling capacitor at the RF input should be implemented with external component. R_{ch} also increases the noise factor only through F_3. It is clear that improvement of ω_T of MOS devices will improve the noise performance. The negative term in the braces of F_4 is due to the impact of inductance (L_g and L_s) on the correlation between induced gate noise and channel noise. This can not be overlooked in this complicated case for accurate estimation of F, which has not been predicted in the previous literatures[3,7].

3 Optimization of CMOS LNA noise performance

To simplify the expression for F and gain more insight on noise optimization, R_g in F is omitted except for F_1 and a new variable Q is defined as

$$Q = \frac{\omega_0 (L_g + L_s)}{R_s + R_g} \approx \frac{\omega_0 (L_g + L_s)}{R_s} \approx \frac{1}{\omega_0 C_{gs} R_s} \qquad (14)$$

After tedious algebraic manipulations, noise factor F can be denoted as

$$F \approx 1 + \frac{R_g}{3R_s} + \frac{\omega_0}{\omega_T}\left\{ Q\beta + \frac{1}{Q}\left(\beta + \frac{\gamma}{\alpha} \right) + \frac{2\gamma}{5} \times \frac{\omega_0}{\omega_T} \right\} - \frac{2|c|}{g_m R_s} \sqrt{\frac{\beta\delta}{5}} \qquad (15)$$
$$\beta = \frac{\delta\alpha}{5} + \left(\frac{\omega_0}{\omega_T} \right)^2 \times \frac{\alpha\gamma}{25} + 2|c| \sqrt{\frac{\beta\delta}{5}}$$

Based on the new expression for F, noise performance of CMOS LNA can be optimized. The optimization presented here is different from the conventional procedure detailed in Ref. [11], which based on the parameters of a fixed device the source impedance is transformed to a noise optimum impedance by an impedance matching network. Thus the input power matching and noise matching may not occur at the same time. For CMOS LNA design, the size and bias of device are under the control of designers. Noise performance can be optimized by seeking optimum device size or bias to minimize noise factor for a design parameter, such as power or gain, under the condition of perfect input power matching.

A simple second-order model of MOS transistor is used to optimize the noise performance, which accounts for high-field effects in short-channel devices[12].

$$I_d = W C_{ox} v_{sat} \frac{V_{od}^2}{V_{od} + L\varepsilon_{sat}} \qquad (16)$$

where V_{od} is the overdrive voltage, C_{ox} is the gate oxide capacitance per unit area, v_{sat} is the saturation velocity, ε_{sat} is the velocity saturation field strength, and W and L are channel width and length, respectively. The definition of V_{od} is

$$V_{od} = V_{gs} - V_T \qquad (17)$$

where V_T is the threshold voltage of the transistor. Thus the device transconductance g_m is given by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{3 v_{sat} \rho \alpha}{\omega_0 L R_s Q} \qquad (18)$$

with the definition that

$$\rho = \frac{V_{od}}{L\varepsilon_{sat}} \qquad (19)$$

Substituting Eq. (18) into (15), noise factor F can be rewritten as

$$F \approx 1 + \frac{R_g}{3R_s} + \frac{\omega_0}{\omega_T}\left\{ Q\left(\beta - \frac{2|c|L\omega_T}{3v_{sat}\rho\alpha} \sqrt{\frac{\gamma\delta}{5}} \right) + \frac{1}{Q}\left(\beta + \frac{\gamma}{\alpha} \right) + \frac{2\gamma}{5} \times \frac{\omega_0}{\omega_T} \right\} \tag{20}$$

To optimize the noise performance of the LNA, it is useful to formulize the quantities α, ω_T, and Q.

$$\alpha = \frac{2 + \rho}{2(1 + \rho)^2} \tag{21}$$

$$\omega_T \approx \frac{g_m}{C_{gs}} = \frac{3v_{sat}}{2L} \times \frac{\rho(2 + \rho)}{(1 + \rho)^2} \tag{22}$$

$$Q \approx \frac{3}{2\omega_0 WL C_{ox} R_s} \tag{23}$$

It is clear that all quantities in Eq. (20) except for Q depend on bias voltage. Q depends on device width. The input circuit of the LNA takes the form of a series-resonant network and the output current is proportional to the voltage on Z_{gs}. At the resonant frequency ω_0, the input power matching is achieved and the transconductance gain G_m of the LNA is

$$\begin{aligned} G_m &= g_m Q_{in}(1 + j\omega_0 R_{ch} C_{gs}) \\ &= g_m \frac{1 + j\omega_0 R_{ch} C_{gs}}{\omega_0 C_{gs}\left(R_s + R_g + R_{ch} + g_m \frac{L_s}{C_{gs}} \right)} \\ &= \frac{\omega_T}{2\omega_0 R_s}\left(1 + j\frac{\omega_0}{\omega_T} \times \frac{\alpha}{5} \right) \end{aligned} \tag{24}$$

where Q_{in} is the effective quality factor of the LNA input circuit. Here the influence of channel resistance R_{ch} on the transconductance gain G_m has been considered, which was ignored in Ref. [7]. It is clear that to fix the value of transconductance gain G_m, ρ(or V_{od}) should be assigned a constant value. Once ρ is determined, G_m is determined and noise factor F can be minimized for fixed G_m by choosing the appropriate device width. The optimum noise factor for fixed G_m optimization is

$$F_{\min, G_m} \approx 1 + \frac{R_g}{3R_s} + \frac{\omega_0}{\omega_T} \times \left\{ 2\sqrt{\left(\beta - \frac{2|c|L\omega_T}{3v_{sat}\rho\alpha} \sqrt{\frac{\gamma\delta}{5}} \right)\left(\beta + \frac{\gamma}{\alpha} \right)} + \frac{2\gamma}{5} \times \frac{\omega_0}{\omega_T} \right\} \tag{25}$$

The corresponding Q_{opt} for $F_{\min, G_m}$ is determined by

$$Q_{opt} = \frac{\beta + \frac{\gamma}{\alpha}}{\sqrt{\left(\beta - \frac{2|c|L\omega_T}{3v_{sat}\rho\alpha} \sqrt{\frac{\gamma\delta}{5}} \right)\left(\beta + \frac{\gamma}{\alpha} \right)}} \tag{26}$$

Further, the device width corresponding to $F_{\min, G_m}$ can be obtained through Eqs. (23) and (26).

From the expression of I_d, the power dissipation of the LNA is formulated as

$$\begin{aligned} P_D &= V_{dd} I_d = \frac{P_0}{Q} \times \frac{\rho^2}{\rho + 1} \\ P_0 &= \frac{3V_{dd} v_{sat} \varepsilon_{sat}}{2\omega_0 R_s} \end{aligned} \tag{27}$$

where V_{dd} is the power supply voltage for the LNA. It is worth noting that P_0 is a constant determined by intended design specs (V_{dd}, ω_0, and R_s) and physical technological parameters (v_{sat} and ε_{sat}). The corresponding power dissipation for $F_{\min, G_m}$ can be determined from Eqs. (26) and (27).

An alternative of fixed G_m noise performance optimization fixes the power dissipation P_D and adjusts bias (ρ or V_{od}) to find the minimum noise factor. It is instructive to recast the noise factor in P_D and ρ.

$$F \approx 1 + \frac{R_g}{3R_s} + \frac{\omega_0}{\omega_T}\left[\frac{P_0}{P_D} \times \frac{\rho^2}{\rho + 1}\left(\beta - \frac{2|c|L\omega_T}{3v_{sat}\rho\alpha} \sqrt{\frac{\gamma\delta}{5}} \right) + \frac{P_D}{P_0} \times \frac{\rho + 1}{\rho^2}\left(\beta + \frac{\gamma}{\alpha} \right) + \frac{2\gamma}{5} \times \frac{\omega_0}{\omega_T} \right] \tag{28}$$

The noise factor F is minimized for a fixed P_D when

$$\frac{\partial F}{\partial \rho} = 0 \tag{29}$$

The solution to this equation is too complex to be given in a closed form for fixed P_D noise optimization. But in a specific design, the optimum bias point can be determined numerically.

4 Results

The noise performance of a CMOS LNA working at 5.2 GHz frequency band is investigated applying the work presented in the previous sections. The technology used is TSMC 0.25μm 3.3V mixed-signal CMOS process. The physical technological parameters of this process are that L = 0.35μm, V_T = 0.55V, C_{ox} = 4.86 × 10^{-3} F/m^2, v_{sat} =

1.05×10^5 m/s, and $\mu_{eff}=0.03\text{m}^2/(\text{V}\cdot\text{s})$. Power supply $V_{dd}=3.3$V and source resistance $R_s=50\Omega$. Parameters c, γ, and δ are bias dependent, while $\delta/\gamma=2$[13,14]. Here the assumption that $c=0.395$j and $\gamma=1.3$ is reasonable. As R_g can be reduced by multi-finger gate layout and salicide process, its effect has not been included in the results below.

For fixed G_m optimization, the curve of optimum NF versus ρ is shown in Fig. 3. In the design process of LNA, bias voltage (ρ or V_{od}) of the device can be determined from the noise requirement. The corresponding device width is found from Eq. (26). As usually power is another important concern, to appreciate the tradeoffs among NF, ρ, and P_D, the corresponding P_D is also shown in the same figure. It makes sense that the optimum NF decreases with the increasing ρ at the cost of more power dissipation. In practical design, only the portion where $\rho<0.3$ is useful.

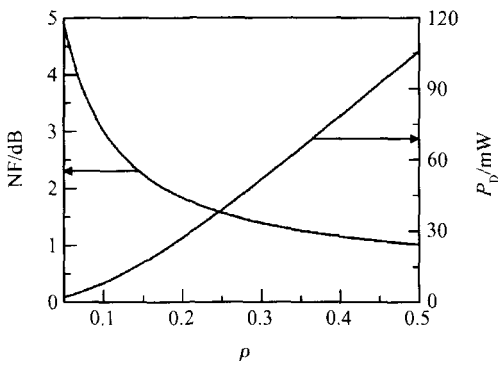

Fig. 3 Optimum NF for fixed G_m optimization and corresponding P_D versus ρ

Fixed P_D optimization is more useful in practical LNA design. The contours of constant noise figure relating ρ and P_D are useful to reveal the design tradeoffs among gate overdrive, power dissipation and noise figure, which are shown in Fig. 4. In the practical design process of LNA, the bias voltage and device width can be determined from the requirements of both noise and power graphically.

5 Conclusion

The noise performance of LNA is crucial for the sensitivity of receiver. All kinds of noise

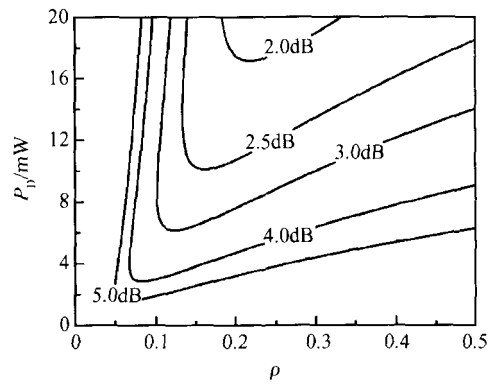

Fig. 4 Contours of constant NF relating ρ and P_D for fixed P_D optimization

sources and components complicate the analysis of noise performance. A systematic approach based on noisy two-port network theory to analyze the noise performance of CMOS LNA is presented in this paper. A new analytical noise figure formula is proposed. Channel noise and induced gate noise in MOS devices are rigidly treated in mathematics.

Investigating the new noise figure formula reveals that distributed gate resistance and other losses in series with the gate have both direct and indirect contributions to the noise figure, which was not obtained in the previous work[3,7]. The impact of channel resistance R_{ch} is evaluated fully for frequency approaching ω_t. Both the input impedance matching and the intended operating frequency are affected by this resistance. This resistance also increases the noise contribution of channel noise to noise figure. The correlation between induced gate noise and channel noise in MOS devices is manipulated rigidly to result in a negative term in the noise figure. This negative term is due to the impact of inductors on the correlation between induced gate noise and channel noise.

For a second-order model of MOS transistor that accounts for high-field effects in short-channel devices, noise optimization of CMOS LNA is performed. The optimization is to minimize the noise figure by seeking the appropriate bias voltage or device width for a design parameter, such as power or transconductance gain, under the condition of

perfect input impedance matching. The results of fixed G_m optimization and fixed P_D optimization are applied to the design of a 5.2GHz CMOS LNA using the TSMC 0.25μm 3.3V mixed-signal CMOS process.

The comprehensive analysis and optimization of CMOS LNA noise performance presented in this paper will benefit the design of high performance LNA, as the design tradeoffs among noise figure, power dissipation and overdrive voltage are revealed quantificationally and visually.

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CMOS 低噪声放大器中噪声的系统研究方法

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摘要: 采用系统研究方法来分析包括 MOS 器件的沟道噪声和感应栅噪声在内的 CMOS 低噪声放大器中的噪声, 并提出了一个新的噪声系数解析式. 基于此解析式, 讨论了分布栅电阻和内部沟道电阻对噪声性能的影响. 对噪声性能进行了两种不同的优化, 并应用于 5.2GHz CMOS 低噪声放大器的设计.

关键词: 放大器噪声; 沟道噪声; 沟道电阻; 感应栅噪声; 低噪声放大器; 噪声优化

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