A Systematical Approach for Noise in CMOS LNA

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Abstract: A systematic approach is used to analyze the noise in CMOS low noise amplifier (LNA), including channel noise and induced gate noise in MOS devices. A new analytical formula for noise figure is proposed. Based on this formula, the impacts of distributed gate resistance and intrinsic channel resistance on noise performance are discussed. Two kinds of noise optimization approaches are performed and applied to the design of a 5.2 GHz CMOS LNA.

Key words: amplifier noise; channel noise; channel resistance; induced gate noise; low noise amplifier; noise optimization

Introduction

The progress in CMOS process makes it possible to integrate more functions on one chip, including radio frequency front-end and digital signal processing back-end. WLAN (wireless local area network) transceiver is one of these digital communication systems, which connects laptops and other mobile terminals to ethernet backbone through AP (access point). As MAC (media access control) part of WLAN transceiver is implemented in CMOS technology, it is appealing to implement the RF front-end circuit in the same technology. It is promising to integrate the whole system on a single chip.

As the first critical component of the receiver, low noise amplifier (LNA) should sufficiently amplify the weak RF signal coming from antenna and duplexer with as less distortion and noise as possible. From the Friis noise equation, the noise figure of the receiving system is dominated by the noise contribution of the first stage or two.

The source inductive degeneration configuration is widely used for LNA due to its superior noise performance. This LNA architecture has been analyzed especially on noise performance. There are three main noise sources, which should be taken into consideration to fully appreciate the noise performance. One is the noise associated with the distributed gate resistance and other losses in series with the gate; the others are induced gate noise and channel noise in submicron MOS devices due to hot electron effects. The analysis in Ref. [3] dealt with the contribution of each noise source separately, thus the interactions among these components were neglected. The correlation between induced gate noise and channel noise was not treated rigidly in mathematics. The induced gate noise was simply split into two components, one of which is fully correlated with the channel noise and the other is uncorrelated with the channel noise. Although this technique simplified the analysis, it was just a conjecture without proof. Only the amplitude of the correlation coefficient, which is a complex number, was considered. As frequency approaching cut-off frequency, the gate impedance of the MOS device exhibits a significant phase shift from its purely capacitive value at lower frequencies. In the RF applications, the channel of MOSFET must...
be viewed as a bias dependent RC distributed transmission line\(^1\). To model the finite time needed to build up the channel charge, one way is to insert a noiseless equivalent resistors \(R_h\) in series with the gate capacitors \(C_g\) and \(C_{gs}\), respectively\(^1\).

The existence of \(R_h\) was verified through simulation and measurement\(^6\). Meanwhile \(R_h\) complicates the analysis of noise figure, and its effect on noise performance was dropped out\(^1\). This was noted in Ref. \([7]\), but the analysis there is a simple extension of the results in Ref. \([3]\) and is not accurate and rigor in mathematics.

To fully appreciate the noise performance of CMOS LNA, a comprehensive analysis is presented in this paper. The noise performance of source inductive degeneration CMOS LNA is analyzed and a new analytical formula for noise figure is derived. Two approaches of noise optimization are performed with respect to fixed transconductance gain \(G_m\) and fixed power dissipation \(P_0\), respectively, and they are applied in the design of a 5.2 GHz CMOS LNA.

2 CMOS LNA noise analysis

The CMOS LNA analyzed here is the source inductive degeneration architecture (Fig. 1) for its superior noise performance and prevalence.

![Fig. 1 Source inductive degeneration LNA architecture](image)

To perform a comprehensive noise analysis of the LNA with a systematic approach, a generic small-signal model of source inductive degeneration LNA is used. The small-signal model is shown in Fig. 2. The parasitic components between gate and drain are not shown in Fig. 2, as there are methods (such as cascode configuration) to improve reverse-isolation. \(Z_0\) denotes the impedance in series with the gate. \(Z_{gs}\) is the impedance between the gate and the source including parasitic \(C_{gs}\) and channel resistance \(R_h\). \(Z_0\) and \(Z_{gs}\) are the source degeneration and load impedances of the LNA, respectively. \(g_m\) is the transconductance of the MOS device.

![Fig. 2 Generic small-signal model for LNA noise analysis](image)

\[ \frac{1}{v_{pg}} = 4kT \frac{R_g \Delta f}{3} \]  
\[ \frac{1}{i_{ds}} = 4kT \gamma g_{m0} \Delta f \]
where $\delta$ is the coefficient of gate noise. This equation is valid when the device is operated in saturation. $i_{ng}$ is induced by the fluctuations in the channel charge due to capacitive coupling when MOS device is biased so that the channel is inverted. Thus $i_{ng}$ and $i_{ad}$ are partially correlated, and the correlation coefficient is given by $c$ for long-channel devices is 0. 395).

Applying the noisy two-port network based analysis outlined in Ref. [10], the input impedance and noise factor $F$ of the source degeneration LNA are given by

$$Z_a = Z_0 + Z_{gs} + Z + g_m Z_s Z_i$$

$$F = 1 + \frac{\sigma_{vng}}{R_s} Z_{in} + |A| \left( \frac{\sigma_{i_{ng}}}{2} \right)^2 + 2 \text{Re}(AB^* i_{ng} i_{ad}^*)$$

$$A = 1 + \frac{Z_a + Z}{R_s}$$

$$B = 1 + \frac{Z_a + Z}{R_s}$$

where it is assumed that $\sigma_{vng}$ is uncorrelated with $i_{ad}$ and $i_{ng}$. It is worth noting that the load impedance $Z_s$ does not appear in the noise factor expression, because the reverse path between gate and drain has been disregarded.

For the source inductive degeneration LNA considered here, the explicit expressions for $Z_a$, $Z_{gs}$, and $Z$ are

$$Z_a = j\omega L_s + R_s$$

$$Z_{gs} = R_{ch} + \frac{1}{j\omega C_{gs}}$$

$$Z = j\omega L_s$$

where $R_s$ includes the distributed gate resistance and loss of inductor $L_s$. $R_{ch}$ is the noiseless equivalent channel resistance to model the deviation of gate impedance of MOS device from its purely capacitive value at lower frequencies as operating frequency approaching $\omega_r$. The expression of $R_{ch}$ is

$$R_{ch} = \frac{1}{5 g_{m}}$$

assuming that operating frequency $\omega$ satisfies

$$\omega \ll \frac{\omega_r}{\alpha}$$

with the definition that

$$\alpha = \frac{g_m}{g_{m}}$$

Note that $\alpha$ is always less than one.

From Eq. (5), the impedance matching input and the corresponding resonant frequency $\omega_b$ is determined by

$$\omega_b = \frac{1}{\sqrt{\frac{L_s + L_g}{1 + \frac{\alpha}{5}}}}$$

The impact of neglecting $R_{ch}$ on input impedance matching and intended operating frequency can be appreciated from Eq. (11).

Substituting Eqs. (1) and (7) into Eq. (6), the noise factor $F$ of source inductive degeneration LNA can be explicitly given by

$$F = 1 + F_1 + F_2 + F_3 + F_4$$

$$F_1 = \frac{R_s}{3 R_s}$$

$$F_2 = \left( \frac{\omega}{\omega_f} \right)^2 \frac{\delta_{vgs} A^2}{5 R_s} \left( \frac{R_s + R_g}{\omega_c} \right)^2 \left( \frac{L_s + L_g}{\omega_c} \right)^2$$

$$F_3 = \frac{\sqrt{\frac{\omega}{\omega_f} \frac{L_s + L_g}{\omega_c} \frac{R_s + R_g + R_{ch}}{\omega_c}}}{1 + \frac{\omega}{\omega_f} \frac{\omega_c}{25} \left( \frac{L_s + L_g}{\omega_c} \right)^2 \frac{R_s}{25}}$$

$$F_4 = \left( \frac{\omega}{\omega_f} \right)^2 \frac{\delta_{vgs} A^2}{5 R_s} \left( \frac{R_s + R_g}{\omega_c} \right)^2 \left( \frac{L_s + L_g}{\omega_c} \right)^2$$

$F_1$ is due to the distributed gate resistance only where the noise contribution of loss in $L_s$ has been disregarded. $F_2$ and $F_3$ are attributed to induced
gate noise and channel noise, respectively. $F_i$ is due to the correlation between induced gate noise and channel noise. During the derivation, some assumptions have been made

$$\gamma = \frac{\gamma m}{C_{gs}} $$

(13)

From the explicit noise factor expression, it is clear that gate resistance $R_g$ increases noise factor through $F_3$, $F_4$, and $F_5$ in addition to its direct contribution to $F$. This has been ignored in the previous work$^{[3,7]}$, where the noise sources are treated individually for simplicity. Multi-finger gate layout and salicide CMOS process can alleviate this plague without penalty. Another conclusion is that $L_g$ should be implemented with bond wire and external high-$Q$ inductor instead of on-chip spiral inductor if lower NF is desirable because the loss of on-chip spiral inductor is larger. Even if on-chip spiral inductor is used for higher integration, the AC coupling capacitor at the RF input should be implemented with external components. $R_{sh}$ also increases the noise factor only through $F_3$. It is clear that improvement of $\omega_T$ of MOS devices will improve the noise performance. The negative term in the braces of $F_i$ is due to the impact of inductance ($L_g$ and $L_s$) on the correlation between induced gate noise and channel noise. This can not be overlooked in this complicated case for accurate estimation of $F$, which has not been predicted in the previous literature.$^{[3,7]}$.

3 □ Optimization of CMOS LNA noise performance

□ □ To simplify the expression for $F$ and gain more insight on noise optimization, $R_g$ in $F$ is omitted except for $F_1$ and a new variable $Q$ is defined as

$$Q = \frac{\omega_1 (L_s + L_g)}{R_1 + R_s}$$

(14)

After tedious algebraic manipulations, noise factor $F$ can be denoted as

$$F \approx 1 + \frac{R_g}{3R_s} \left( 1 + \frac{1}{\gamma_3} \right) \left( 1 + \frac{1}{\gamma_4} \right) \left( 1 + \frac{1}{\gamma_5} \right) +$$

$$\frac{\omega_1}{5} \left( \frac{\omega_1}{\omega_T} \right)^2 \left( 1 + \frac{1}{\gamma_3} \right) \left( 1 + \frac{1}{\gamma_4} \right) \left( 1 + \frac{1}{\gamma_5} \right)$$

(15)

□ □ Based on the new expression for $F$, noise performance of CMOS LNA can be optimized. The optimization presented here is different from the conventional procedure detailed in Ref. [11], which based on the parameters of a fixed device the source impedance is transformed to a noise optimum impedance by an impedance matching network. Thus the input power matching and noise matching may not occur at the same time. For CMOS LNA design, the size and bias of device are under the control of designers. Noise performance can be optimized by seeking optimal device size or bias to minimize noise factor for a design parameter, such as power or gain, under the condition of perfect input power matching.

A simple second-order model of MOS transistor is used to optimize the noise performance, which accounts for high-field effects in short-channel devices$^{[12]}$.

$$I_d = W C_{ox} \frac{V_{od}}{V_{od} + \varepsilon_{sat}}$$

(16)

where $V_{od}$ is the overdrive voltage, $C_{ox}$ is the gate oxide capacitance per unit area, $V_{sat}$ is the saturation velocity, $\varepsilon_{sat}$ is the velocity saturation field strength, and $W$ and $L$ are channel width and length, respectively. The definition of $V_{od}$ is

$$V_{od} = V_{gs} - V_T$$

(17)

where $V_T$ is the threshold voltage of the transistor. Thus the device transconductance $g_m$ is given by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{3}{\omega_0 L R_s} \frac{\partial \alpha}{\partial V_{gs}}$$

(18)

with the definition that

$$\rho = \frac{V_{od}}{\varepsilon_{sat}} $$

(19)

□ □ Substituting Eq. (18) into (15), noise factor $F$ can be rewritten as
\[ F \approx 1 + \frac{R_c}{3 R_i} + \frac{\omega_i}{\omega_t} \left( \frac{1}{\beta} + \frac{2 \gamma}{5} \frac{\omega_t}{\omega_i} \right) \]

\[ \frac{1}{Q} \left( \beta + \frac{V}{\alpha} \right) + \frac{2 \gamma}{5} \frac{\omega_t}{\omega_i} \]

(20)

To optimize the noise performance of the LNA, it is useful to formulize the quantities \( \alpha, \omega_t \), and \( Q \).

\[ \alpha = \frac{2 + \rho}{2(1 + \rho)^2} \]

(21)

\[ \omega_t \approx \frac{g_m}{C_{gs}} = \frac{3 V_{dd}}{2 L} \times \frac{\beta + \rho}{(1 + \rho)^2} \]

(22)

\[ Q = \frac{3}{2 \omega_w W L C_{eq} R_i} \]

(23)

It is clear that all quantities in Eq. (20) except for \( Q \) depend on bias voltage. \( Q \) depends on device width. The input circuit of the LNA takes the form of a series-resonant network and the output current is proportional to the voltage on \( Z_{gs} \). At the resonant frequency \( \omega_t \), the input power matching is achieved and the transconductance gain \( G_m \) of the LNA is

\[ G_m = g_m Q_m (1 + j \omega_t R_c C_{gs}) \]

\[ = g_m \frac{1 + j \omega_t R_c C_{gs}}{\omega_t C_{gs}} = \frac{\omega_t}{2 \omega_w R_s} \left[ 1 + j \frac{\omega_t}{\omega_r} \frac{\alpha}{5} \right] \]

(24)

where \( Q_m \) is the effective quality factor of the LNA input circuit. Here the influence of channel resistance \( R_c \) on the transconductance gain \( G_m \) has been considered, which was ignored in Ref. [7]. It is clear that to fix the value of transconductance gain \( G_m \) \( \rho \) (or \( V_{dd} \)) should be assigned a constant value. Once \( \rho \) is determined, \( G_m \) is determined and noise factor \( F \) can be minimized for fixed \( G_m \) by choosing the appropriate device width. The optimum noise factor for fixed \( G_m \) optimization is

\[ F_{\text{opt}, G_m} \approx 1 + \frac{R_c}{3 R_i} + \frac{\omega_t}{\omega_i} \times \left[ \frac{1}{\beta} + \frac{2 \gamma}{5} \frac{\omega_t}{\omega_i} \right] \]

\[ \left[ \frac{2}{N} \left( \beta + \frac{V}{\alpha} \right) + \frac{2 \gamma}{5} \frac{\omega_t}{\omega_i} \right] \]

(25)

The corresponding \( Q_{\text{opt}} \) for \( F_{\text{opt}, G_m} \) is determined by

\[ Q_{\text{opt}} = \frac{\beta + \frac{V}{\alpha}}{2 \omega_t \omega_i} \]

(26)

Further, the device width corresponding to \( F_{\text{opt}, G_m} \) can be obtained through Eqs. (23) and (26).

From the expression of \( I_s \), the power dissipation of the LNA is formulated as

\[ P = V_{dd} I_s = \frac{P_0}{Q} \times \frac{\rho^2}{\rho + 1} \]

(27)

where \( V_{dd} \) is the power supply voltage for the LNA. It is worth noting that \( P_0 \) is a constant determined by intended design specs (\( V_{dd}, \omega_t \), and \( R_s \)) and physical technological parameters (\( v_{dd} \) and \( \varepsilon_{ox} \)). The corresponding power dissipation for \( F_{\text{opt}, G_m} \) can be determined from Eqs. (26) and (27).

An alternative of fixed \( G_m \) noise performance optimization fixes the power dissipation \( P_0 \) and adjusts bias \( \rho \) or \( V_{dd} \) to find the minimum noise factor. It is instructive to recast the noise factor in \( P_0 \) and \( \rho \).

\[ F \approx 1 + \frac{R_c}{3 R_i} + \frac{\omega_t}{\omega_i} \left[ \frac{P_0}{\rho} \times \frac{\rho^2}{\rho + 1} \right] \left[ \beta + \frac{2 \gamma}{5} \frac{\omega_t}{\omega_i} \right] \]

(28)

\[ \frac{P_0}{\beta} \times \frac{\rho + 1}{\rho} \left[ \beta + \frac{V}{\alpha} \right] + \frac{2 \gamma}{5} \frac{\omega_t}{\omega_i} \]

\[ \frac{\beta + \frac{V}{\alpha}}{2 \omega_t \omega_i} \]

(29)

The solution to this equation is too complex to be given in a closed form for fixed \( P_0 \) noise optimization. But in a specific design, the optimum bias point can be determined numerically.

4 Results

The noise performance of a CMOS LNA working at 5.2 GHz frequency band is investigated applying the work presented in the previous sections. The technology used is TSMC 0.25 \( \mu \)m 3.3 V mixed-signal CMOS process. The physical technological parameters of this process are that \( L = 0.3 \mu m, V_T = 0.55 V, C_{gs} = 4.86 \times 10^{-2} F/m^2, v_{dd} = \)
1.05 × 10^5 m/s, and μ_{eff} = 0.03 m^2 / (V·s). Power supply V_{dd} = 3.3 V and source resistance R_s = 50Ω. Parameters c, δ, and Y are bias dependent, while δ/γ = 2^{13,14}. Here the assumption that c = 0.395 and Y = 1.3 is reasonable. As R_s can be reduced by multi-finger gate layout and salicide process, its effect has not been included in the results below.

For fixed G_m optimization, the curve of optimum NF versus ρ is shown in Fig. 3. In the design process of LNA, bias voltage (Φ or V_{dd}) of the device can be determined from the noise requirement. The corresponding device width is found from Eq. (26). As usually power is another important concern, to appreciate the tradeoff among NF, ρ, and P_0, the corresponding P_0 is also shown in the same figure. It makes sense that the optimum NF decreases with the increasing ρ at the cost of more power dissipation. In practical design, only the portion where ρ < 0.3 is useful.

![Fig. 3](Image)

**Fig. 3** Optimum NF for fixed G_m optimization and corresponding P_0 versus ρ

Fixed P_0 optimization is more useful in practical LNA design. The contours of constant noise figure relating ρ and P_0 are useful to reveal the design tradeoffs among gate overdrive, power dissipation and noise figure, which are shown in Fig. 4. In the practical design process of LNA, the bias voltage and device width can be determined from the requirements of both noise and power graphically.

5 Conclusion

The noise performance of LNA is crucial for the sensitivity of receiver. All kinds of noise sources and components complicate the analysis of noise performance. A systematic approach based on noisy two-port network theory to analyze the noise performance of CMOS LNA is presented in this paper. A new analytical noise figure formula is proposed. Channel noise and induced gate noise in MOS devices are rigidly treated in mathematics.

Investigating the new noise figure formula reveals that distributed gate resistance and other losses in series with the gate have both direct and indirect contributions to the noise figure, which was not obtained in the previous work^{13,17}. The impact of channel resistance R_c is evaluated fully for frequency approaching Ω. Both the input impedance matching and the intended operating frequency are affected by this resistance. This resistance also increases the noise contribution of channel noise to noise figure. The correlation between induced gate noise and channel noise in MOS devices is manipulated rigidly to result in a negative term in the noise figure. This negative term is due to the impact of inductors on the correlation between induced gate noise and channel noise.

For a second-order model of MOS transistor that accounts for high-field effects in short-channel devices, noise optimization of CMOS LNA is performed. The optimization is to minimize the noise figure by seeking the appropriate bias voltage or device width for a design parameter, such as power or transconductance gain, under the condition of
perfect input impedance matching. The results of fixed $G_0$ optimization and fixed $P_0$ optimization are applied to the design of a 5.2 GHz CMOS LNA using the TSMC 0.23 $\mu$m 3.3V mixed-signal CMOS process.

The comprehensive analysis and optimization of CMOS LNA noise performance presented in this paper will benefit the design of high performance LNA, as the design tradeoffs among noise figure, power dissipation and overdrive voltage are revealed quantificationally and visually.

References
