Lattice-Matched InP-Based HEMTs with f_T of 120 GHz *

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Abstract: Lattice-matched InP-based InAlAs/InGaAs HEMTs with 120 GHz cutoff frequency are reported. These devices demonstrate excellent DC characteristics: the extrinsic transconductance of 600 mS/mm, the threshold voltage of -1.2 V, and the maximum current density of 500 mA/mm.

Key words: cutoff frequency; high electron mobility transistors; InAlAs/InGaAs; InP
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1 Introduction

High electron mobility transistors (HEMTs) have been demonstrated excellent high-frequency and low-noise performance because of the superior transport properties. The applications of HEMTs can meet the demand of two important aspects: high-speed optical-fiber communication systems and high-frequency wireless systems, such as millimeter-wave (30 ~ 300 GHz) communication systems[1].

InP-based HEMTs have superior electronic transport properties to GaAs-based structures due to the large band separation, low effective mass, high low-field electron mobility, high electron saturation velocity, and high sheet carrier densities in the InGaAs channel[2]. They are promising devices to achieve ultrahigh-speed operation because of the superior electronic transport properties mentioned above, which are achieved by the InAlAs/InGaAs/InP material system. In recent years, InP-based HEMTs have been leading the highest current-gain cutoff frequency (f_T) in solid-state devices. Several groups have fabricated InP-based HEMTs with f_T over 350 GHz[3~6]. The highest f_T ever reported was 472 GHz for lattice-matched HEMTs and 562 GHz for pseudomorphic HEMTs[7]. However, the research on InP-based HEMTs in our country is behind others and the report about this aspect is relatively lack. In this article, we report the lattice-matched InP-based InAlAs/InGaAs HEMTs with f_T of 120 GHz, including the device structure, fabrication process, DC and RF performances.

2 Material structure

The lattice-matched HEMT epitaxial layers were grown on 50mm semi-insulating (100) InP substrate by molecular beam epitaxy (MBE). The layers shown in Fig. 1, consists of a 300nm $In_{0.52}Al_{0.48}As$ buffer layer, 15nm $In_{0.53}Ga_{0.48}As$ channel layer, 3nm $In_{0.52}Al_{0.48}As$ spacer layer, Si planar doped (5×10^{12} cm^{-2}) layer, 10nm $In_{0.52}Al_{0.48}As$

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barrier layer, 6nm InP etching-stopper layer, and 25nm Si-doped ($1 \times 10^{19}\ cm^{-3}$) n^+-$In_{0.53}Ga_{0.47}As$ cap layer. All the layers are lattice-matched to the InP substrate. Hall measurements show a two-dimensional electron gas (2DEG) sheet density of $3.32 \times 10^{12}\ cm^{-2}$ and a mobility of $9290 cm^2/(V \cdot s)$ at room temperature. In our experiments, we use two kinds of substrate provided by MBE technology, Singapore and Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences.

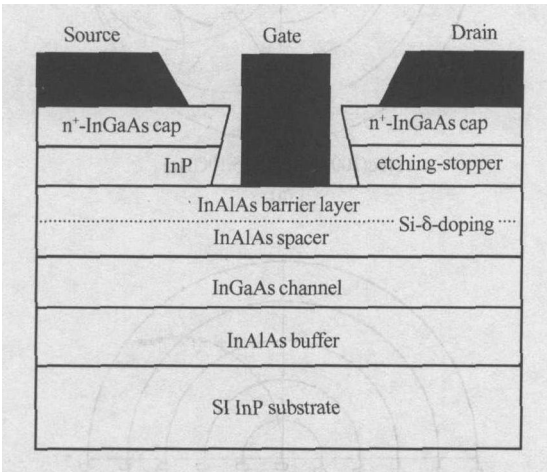

Fig. 1　Schematic cross-section of InP HEMT

3　Fabrication process

Source and drain electrodes were made first. The source and drain patterns were generated with electronic beam (EB) direct writing. The Ohmic contact was formed with AuGeNi/Au metallization and alloyed after lift-off at a wafer temperature of 285 ℃ for 10min in nitrogen. The temperature must be well controlled because fine Ohmic contact would be hard to form in lower temperature and degradation of the eptiaxial structure would occur to worsen the DC and RF performance of HEMTs in higher temperature above 300 ℃. Then the devices were isolated with mesa isolation by wet chemical etching using $H_3PO_4/H_2O_2/H_2O$ solution. Next the Ti/Au connecting wire and testing pad metal were evaporated by electronic beam evaporation system.

The gate formation process was similar to that of our previous works[8] and only the gate-metal thickness was adjusted. We used a novel PMMA/PMGI/PMMA trilayer resistance structure, getting the gate pattern by a single alignment, EB exposure and a series of development steps. The gate recess etching was then performed with $H_2SO_4/H_2O_2/H_2O$ solution while temperature control and ultrasonic were complemented. Finally, the Ti/Pt/Au gate metal was evaporated and lifted off. Figure 2 is the photograph of the device we obtained, with 0.4μm of gate length, 2×50μm of gate width and 2.0μm of source to drain distance.

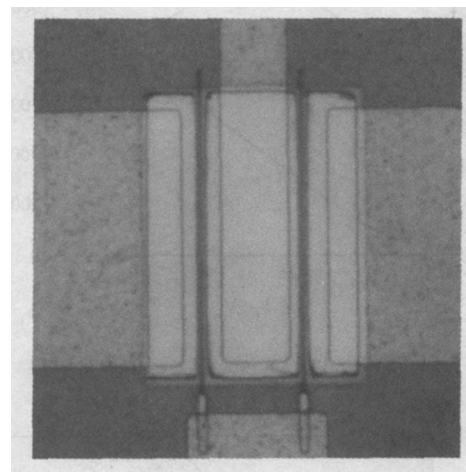

Fig. 2　Partial photograph of InP HEMT

4　Device performance

The DC and RF characteristics were measured at room temperature. Figure 3 shows the typical *I-V* characteristics of the HEMTs measured by HP4155. The gate-source voltage V_{GS} is decreased from 0 to -1.2V in -0.2V steps and the device is well pinched off at $V_{GS} = -1.2$V. The maximum DC transconductance g_m is 602mS/mm, shown in Fig. 4. The gate to drain breakdown voltage is about -1V, measured under the gate current of 1 mA/mm, shown in Fig. 5. The on-state drain to source breakdown voltage, i.e. $V_{GS} = 0$V, is 3.1V.

S-parameters, shown in Fig. 6, were measured in a frequency range from 0.1 to 15.1GHz in 0.1GHz steps by HP8510C network analyzer and

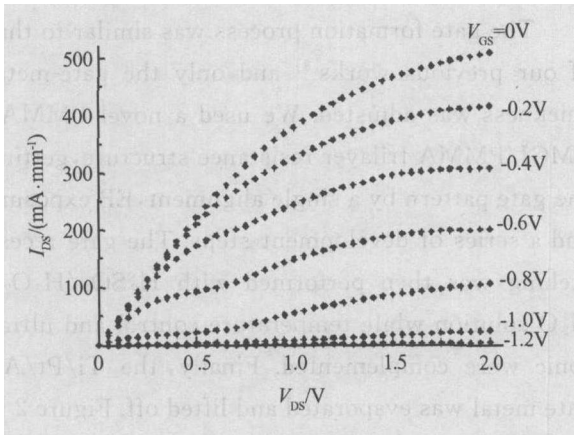

Fig. 3 *I-V* characteristics of InP HEMT

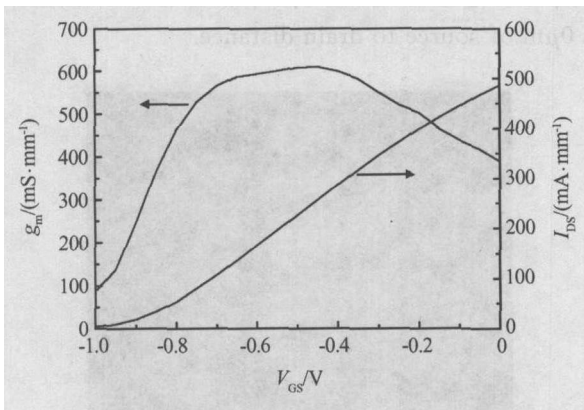

Fig. 4 I_{DS} and g_m versus V_{GS} of InP HEMT

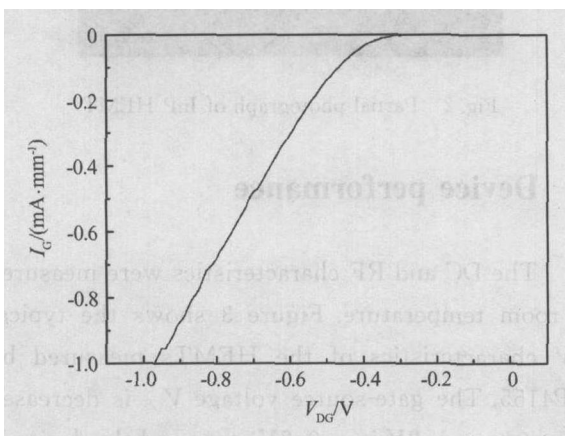

Fig. 5 Breakdown characteristics of gate-drain

cascade on wafer probes. Figure 7 shows the frequency dependence of current gain ($|h_{21}|^2$) and maximum available/stable power gain (MAG/MSG) of HEMT. The drain-source voltage V_{DS} is 0.8V, and gate-source voltage V_{GS} is -0.6V. The parasitic capacitance caused by the probing pads is subtracted from the measured *S*-parameters. f_T of 120GHz is obtained by the extrapolation of $|h_{21}|^2$ in a frequency range from 0.1 to 15.1GHz, where the slope of least-squares fitting of $|h_{21}|^2$ is -20dB/decade, as expected. The f_{max} is only 40GHz, where the slope is -40dB/decade due to the singularity.

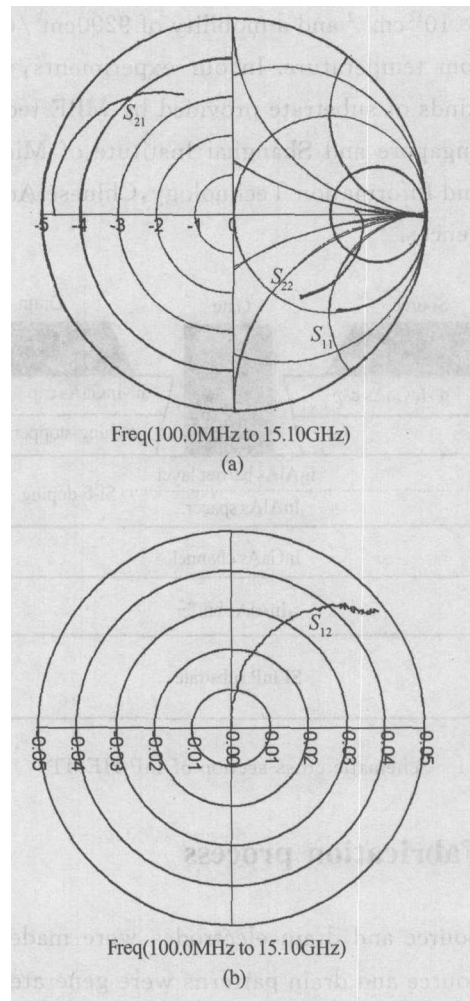

Fig. 6 *S*-parameters of InP HEMT (a) S_{11}, S_{21}, and S_{22}; (b) S_{12}

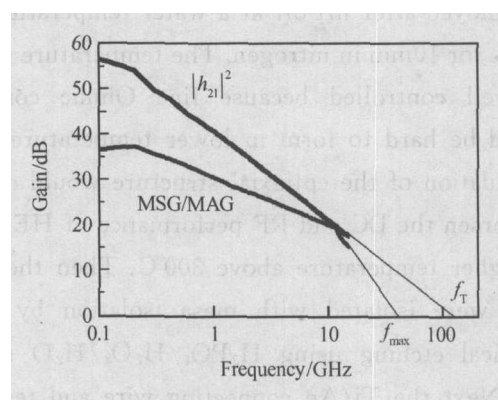

Fig. 7 Current gain and maximum available/stable power gain

5 Summary

The lattice-matched InP-based InAlAs/InGaAs HEMTs with 120 GHz cutoff frequency are fabricated and characterized. f_{max} is much lower than f_T mainly because of the parasitic parameters. In order to get higher f_T, f_{max}, and more reliable devices in future, much attentation should be paid to solve the problems in fabrication process we found.

References

[1] Streit D, Lai R, Oki A, et al. InP HEMT and HBT technology and applications. Electron Devices for Microwave and Optoelectronic Applications, 2002: 14

[2] Chen Y W, Hsu W C, Hsu R T, et al. Characteristics of InAlAs/InGaAs HEMTs with various InGaAs channels. Solid-State Electron, 2004, 48(1): 119

[3] Suemitsu T, Ishii T, Yokoyama H, et al. 30-nm InAlAs/InGaAs HEMTs lattice-matched to InP substrate. IEDM, San Francisco, California, 1998: 223

[4] Endoh A, Yamashita Y, Higashiwaki M, et al. High f_T 50-nm-gate lattice-matched InAlAs/InGaAs HEMTs. International Conference on Indium Phosphide and Related Materials, williamsburg, VA, USA, 2000: 87

[5] Yamashita Y, Endoh A, Shinohara K, et al. Ultra-short 25-nm-gate lattice-matched InAlAs/InGaAs HEMTs within the range of 400 GHz cutoff frequency. IEEE Electron Device Lett, 2001, 22(8): 367

[6] Suemitsu T, Yokoyama H, Ishii T, et al. 30-nm two-step recess gate InP-based InAlAs/InGaAs HEMTs. IEEE Trans Electron Devices, 2002, 49(10): 169

[7] Yamashita Y, Endoh A, Shinohara K, et al. Pseudomorphic InAlAs/InGaAs HEMTs with an ultrahigh f_T of 562 GHz. IEEE Electron Device Lett, 2002, 23(10): 573

[8] Shi Huafen, Zhang Haiying, Liu Xunchun, et al. A novel high-yield InP-based T-shaped nanometer-gate fabrication technique. Chinese Journal of Semiconductors, 2003, 24(4): 411 (in Chinese) [石华芬, 张海英, 刘训春, 等. 一种新的高成品率 InP 基 T 型纳米栅制作方法. 半导体学报, 2003, 24(4): 411]

截止频率为 120 GHz 的晶格匹配 InP 基 HEMT*

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摘要: 报道了具有良好直流特性的晶格匹配 InP 基 HEMT, 器件的跨导为 600 mS/mm, 阈值电压为 -1.2 V, 最大电流密度为 500 mA/mm, 截止频率为 120 GHz.

关键词: 截止频率; 高电子迁移率场效应晶体管; InAlAs/InGaAs; InP

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