A 4.8GHz CMOS Fully Integrated LC Balanced Oscillator with Symmetrical Noise Filter Technique and Large Tuning Range

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Abstract: This paper presents a fully integrated 4.8GHz VCO with an invention——symmetrical noise filter technique. This VCO, with relatively low phase noise and large tuning range of 716MHz, is fabricated with the 0.25μm SMIC CMOS process. The oscillator consumes 6mA from 2.5V supply. Another conventional VCO is also designed and simulated without symmetrical noise filter on the same process, which also consumes 6mA current and is with the same tuning. Simulation result describes that the first VCO's phase noise is 6dBc/Hz better than the latter's at the same offset frequency from 4.8GHz. Measured phase noise at 1MHz away from the carrier in this 4.8GHz VCO with symmetrical noise filter is -123.66dBc/Hz. This design is suitable for the usage in a phase-locked loop and other consumer electronics. It is amenable for future technologies and allows easy porting to different CMOS manufacturing process.

Key words: VCO; symmetrical noise filter; radio frequency; inductor; switch capacitor
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1 Introduction

Advances in radio frequency (RF) communication systems have brought on a large increase in the demand for communication devices such as mobile/cellular telephones, radios, portable digital telecommunications, WLAN phones, and data devices[1]. To transform RF signal to intermediate frequency (IF), a local oscillator (LO) is needed. IF output desires that precise down-conversion does not interfere with the adjacent channels. So it requires that LO has low phase noise. Integrated voltage controlled oscillators are commonly used in RF system and used to up- and down-convert signals.

Due to the ever-increasing demand for bandwidth, very stringent requirements are placed on the spectral purity and tuning range of local oscillators. Recently, there has been some work on improving phase noise and tuning range[2] in VCO. It results in a large number of implementations. Despite these endeavors, design and optimization of integrated LC VCO still pose many challenges to circuit designers as large tuning range and low voltage are required. It is especially important when gigahertz tuning range is needed, as any parasitic capacitor will decrease the resonating frequency and the tuning range.

In this paper, a 4.8GHz VCO based on new symmetrical noise filter technology is described. To realize low phase noise, a high quality on-chip inductor is custom-made by ADS MOM, and symmetrical noise filter technique can further reduce the noise coming from tail current source and power line, especially the $1/f$ noise. Switch capacitor array can realize large tuning range of the VCO frequency. The principle of this VCO and the process

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of phase noise are described in detail. This chip is fabricated in normal 0.25μm one-poly five-metal RF CMOS technology. The measured results show that the phase noise is -123.66dBc/Hz at 1MHz when the VCO frequency is 4.728GHz, and the tuning range is more than 700MHz.

2 Phase noise

Rael *et al*.[3] concluded three physical mechanisms are responsible for flicker noise up-conversion into phase noise, which include flicker noise in bias current's up-conversion effect and flicker noise in differential pair's modulation effect. Hegazi *et al*.[2] analysed how current-source noise creates phase noise in the oscillator. The switching nMOS differential pair, which is acting as a single-balanced mixer for noise in the current source, commutates and up-converts low frequency noise into two correlated amplitude modulation (AM) sidebands around the fundamental. AM leads to phase modulation (PM) and phase noise in VCO because of the non-linearity of varactor. Noise around the second harmonic down-converts into the frequency close to the oscillation frequency and also produces phase noise. In Ref. [3], the phase noise of VCO can be expressed as

$$L\{\Delta\omega\} = 10\lg\left[\frac{8FkTR}{V_0^2}\times\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \qquad (1)$$

where

$$F = 1 + \frac{4\gamma RI_T}{\pi V_0} + \frac{4}{9}\gamma g_{m,tail}R \qquad (2)$$

where I_T is the bias current, γ is the channel noise coefficient of the MOSFET, and g_m is the transconductance of the current source MOSFET, R is the equal impedance of the LC tank, V_0 is the amplitude of the oscillator.

A proper designed noise filter reduces the noise factor (F) of the differential LC oscillator to its fundamental minimum of $1+\gamma/2$. Once the constant of proportionality F is minimum, given a resonator Q and current limited operation, for minimum phase noise the oscillator amplitude V_0 must be as large as possible.

In the conventional design[4], complementary cross-coupled transistors are around a LC tank. The negative conductance generated by cross-coupled nMOS and pMOS transistors, is designed to compensate for the loss associated with the LC tank. The advantage of using both pMOS and nMOS cross-coupled transistors is less current consumption and lower phase noise by sizing the pMOS and nMOS transistors properly.

Thus, Hegazi *et al*.[2] presented an evolution of the conventional VCO topology, among it noise filter technique is adopted, where an on-chip LC filter is inserted between the tail current source and nMOS switch pair. It uses a narrow band circuit to suppress the noise in the current source. But the low frequency noise from tail current source is not removed although on-chip capacitor C_1 exists. Andreani[5] gives improvement on Hegazi's structure by adding an off-chip large capacitor C_p paralleling with C_1, so low frequency noise can be filtered more. Though the noise of tail current source can be suppressed by giving a high impedance in the narrow band of frequencies at point B of Fig. 1, high and low frequency noise from power line also have the same up-conversion effect and modulation effect in the pMOS switch pair as the tail current source does, so point A in Fig. 1 also should be high impedance to achieve better noise performance.

Therefore, new structures should be adopted to make a good improvement in phase noise under condition of large tuning range.

3 Design

Figure 2 shows a simplified block diagram of the VCO with symmetrical noise filter technique and large tuning range. The LC tank resonator circuit is to select an operating frequency, and a switch capacitor array connected to the LC resonator circuit is to change the frequency range of VCO. Complementary cross-coupled transistors M1 ~M4 are to generate the negative conductance to

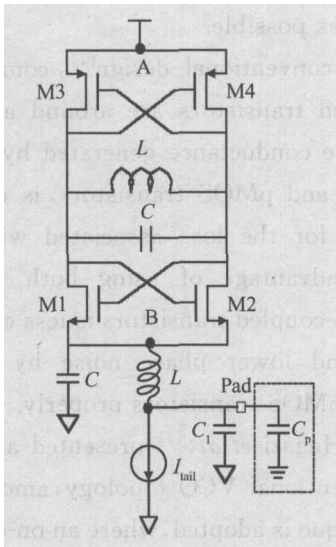

Fig. 1 VCO with noise filter

compensate for the loss associated with the LC tank as the conventional VCO does. The most discrepancy is symmetrical noise filter circuit, which is comprised two LC resonators, L_1 and C_{p_1}, L_2 and C_{p_2}. It resonates at the second harmonic of the oscillation frequency. C_1 and C_2 are two big capacitors, so ports A, B are AC grounds. Therefore it appears a high impendence to the second harmonic in the two port of the main LC tank, C and D. As shown in Fig. 2, both L_1-C_{p_1} and L_2-C_{p_2} are chosen to resonate at 2ω in parallel with whatever capacitor is present at the common source of the two differential pair.

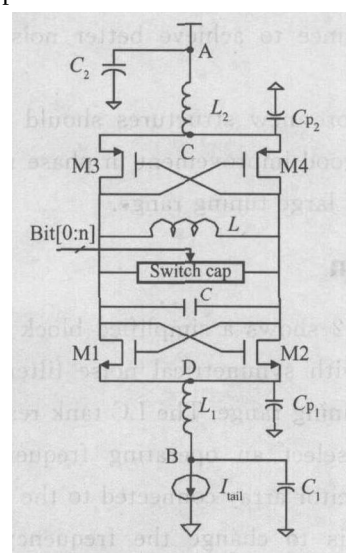

Fig. 2 VCO with symmetrical noise filter

The impedance at resonating frequency is limited only by the quality factor of the inductors. C_{p_1} or C_{p_2} comprises all the capacitors appeared at C or D. Since the VCO has a large tuning range, the second harmonic also has a varied frequency. To get better impedance at noise filter port, C and D, proper Q of the inductors, L_1 and L_2, should be designed to resonate.

The inductor is a key device to realize low phase noise. It is designed using a fast simulator that models self-inductance, parasitic capacitor, and all losses, including dissipation due to displacement

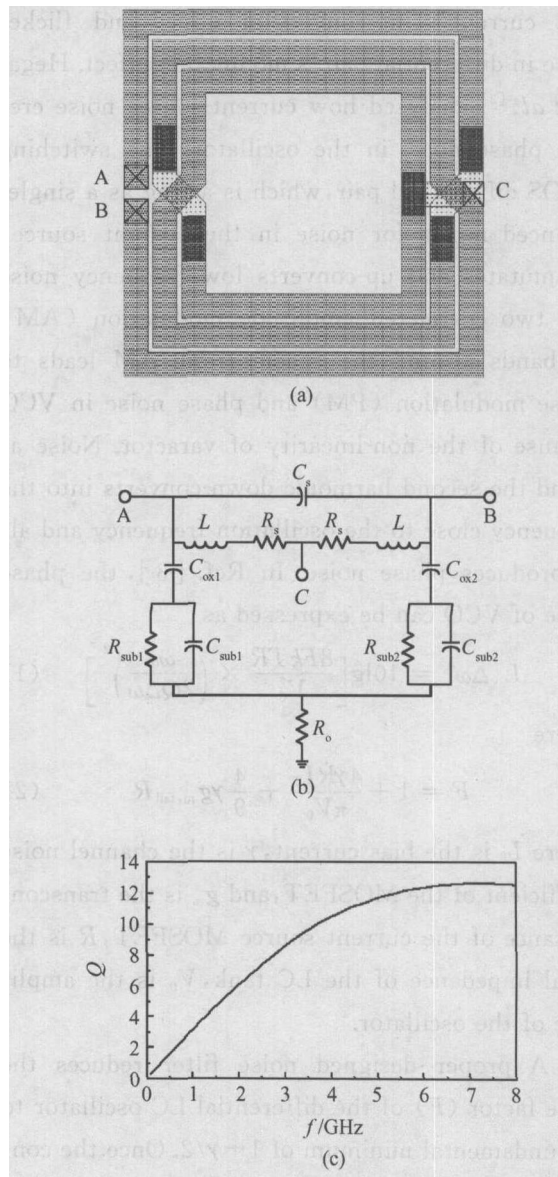

Fig. 3 (a) Differential inductor; (b) Model of inductor; (c) Quality of the inductor

and eddy currents in the substrate. The differential inductor is about 1. 2nH and has a relatively high quality factor; simulation result shows that the Q value at 4. 8GHz is about 11. 2, so it is the proper selection for resonator. Figure 3(a) is a differential inductor, which is designed by ASITIC and simulated by ADS MOM; Figure 3(b) shows the SPECTRE model; Figure 3(c) is the quality curve of the inductor.

Figure 4 is a cell of switch capacitor. Compared to conventional cell, the resistors R_1 and R_2 are added to the gate of the switch nMOS transistor. It reduces the noise coming from the control line because it can block AC signal coming from the control line. There exists a common mode ground point A between M1 and M2. To isolate the signal from A to ground, a resistor R_3 is inserted between them.

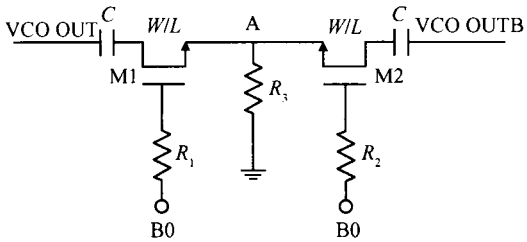

Fig. 4　Switch capacitor cell

The quality of the switch is directly related to the tank quality. To improve the phase noise of the VCO, the Q of the switch needs to be improved. It can be shown as below[6]

$$Q = \frac{1}{\omega_0 R_{on} C_{mm}} \tag{3}$$

where R_{on} is the channel resistor of M1 and M2, C_{mm} is the metal to metal capacitor, among this

$$R_{on} = [\mu C_{ox} \frac{W}{L} (V_{GS} - V_t)]^{-1} \tag{4}$$

where μC_{ox} is a process constant, W/L is device size, $V_{GS} - V_t$ is the overdrive voltage. As Eq. (4) shown, to minimize the channel resistor of a switch in the ON state, it uses the maximum V_{GS} (usually VDD). With an array of switch capacitor, this VCO can adjust frequency from 4. 8 to 5. 7GHz and the tuning range is 900MHz from the simulation.

4 Simulation

The symmetrical noise filter technique is simulated and a very significant reduction of phase noise is achieved. The following section is the simulation result.

As Fig. 5 shown, phase noise at 1MHz away from the carrier in this 4. 8GHz oscillator with symmetrical noise filter is - 130. 5dBc/ Hz, while the phase noise of the other one without symmetrical noise filter is - 124. 5dBc/ Hz at the same offset frequency. Phase noise of VCO with symmetrical noise filter is 6dB better than that of the conventional one.

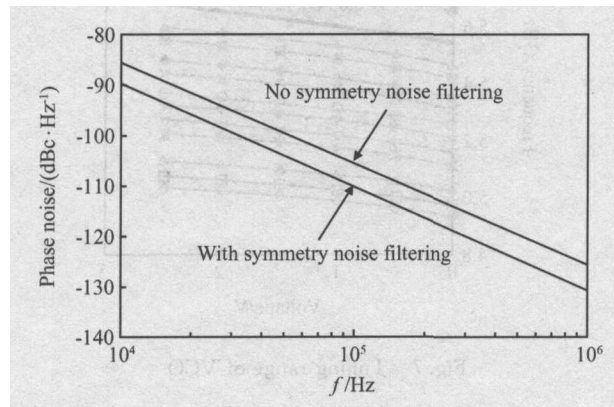

Fig. 5　Phase noise of VCO with or without symmetrical noise filter by simulation

Simulating the output amplitude versus bias current can optimize the bias current of the VCO. Figure 6 is the simulation result of amplitude under the condition of differential core current, the minimum phase noise times current consumption is achieved at the corner between the current-limited and voltage-limited regions, the corresponding current is about 6mA, which meets the specification.

To realize large tuning range, switch capacitor technique is applied, Figure 7 is the simulation result of tuning curve. Through linearization, it can be seen that the gain of the VCO is about 55MHz/ V, and the tuning range is 4. 93～5. 85GHz, nearly 920MHz range, which is 18. 3%. Large tuning

range can be achieved by switch capacitor technique.

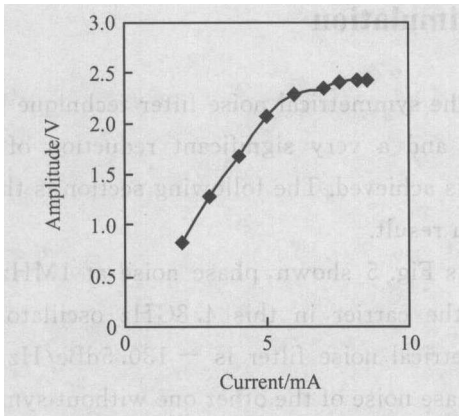

Fig. 6 VCO output amplitude versus current

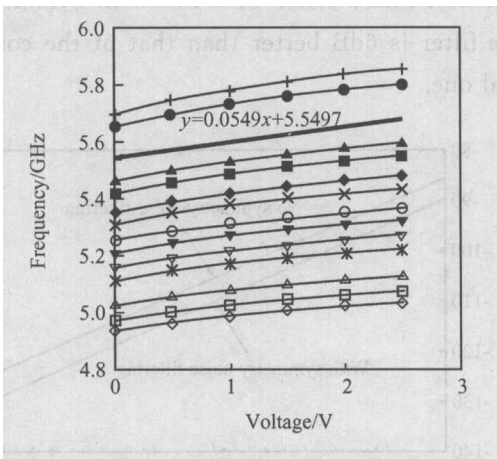

Fig. 7 Tuning range of VCO

5 Experimental result

Table 1 summarizes the performance of the VCO, which was implemented in a five-metal 0.25μm RF CMOS technology with MIM capacitor. Figure 8 shows the layout of the VCO module and it is a part of a RF transceiver. Limited by the test range of the spectrum analyzer the output of the VCO is divided by four. Figure 9 is the frequency spectrum of VCO output, and the real frequency range of this VCO is 4.012 to 4.728GHz. There is about 900MHz difference between the simulation result and the test result, the reason is that the simulation result is without taking care of the parasitic capacitance among the metal to substrate, metal to active region, and metal to metal, and model is also not so accurate when the working frequency is near the f_T of the device.

Table 1 VCO performance

Supply voltage	2.5V
Current (VCO core)	6mA
Frequency range	4.012～4.728GHz
Tuning range	17.8%
Output power (50Ω load)	0.151dBm
Phase noise	-123.66dBc/Hz at 1MHz

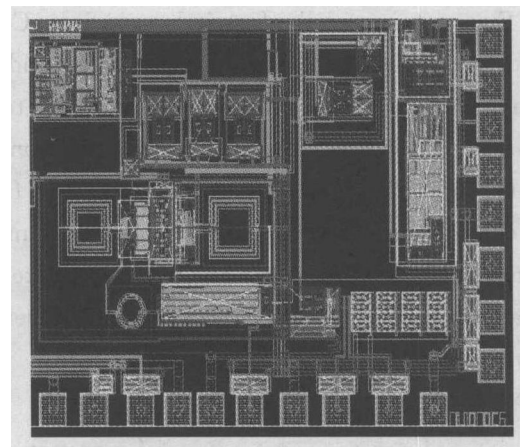

Fig. 8 VCO layout

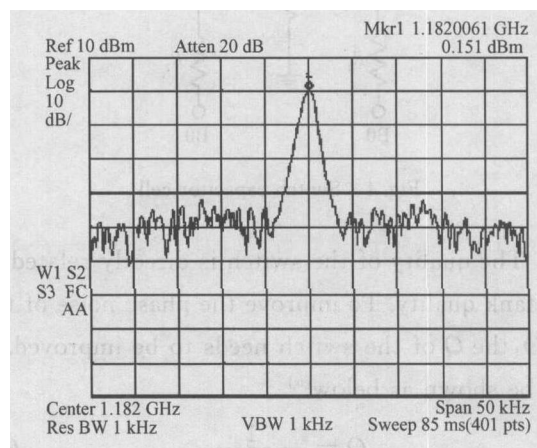

Fig. 9 VCO output spectrum (divided by four)

The phase noise, measured on 4404E spectrum analyzer, is -123.66dBc/Hz at 1MHz offset for the 1.104GHz signal, which is 4.416GHz signal divided by four. At 100kHz offset, the phase noise is about -97dBc/Hz. The phase noise measured is about 7dB worse than the simulation result, the reason of which is that this VCO is tested on the PLL of a RF transceiver and many building blocks, especially the sigma-delta modulator, contribute noise

to the output spectrum though VCO dominates the noise in the far offset region, while the simulation result is gotten without the other blocks. The phase noise versus offset frequency is shown in Fig. 10.

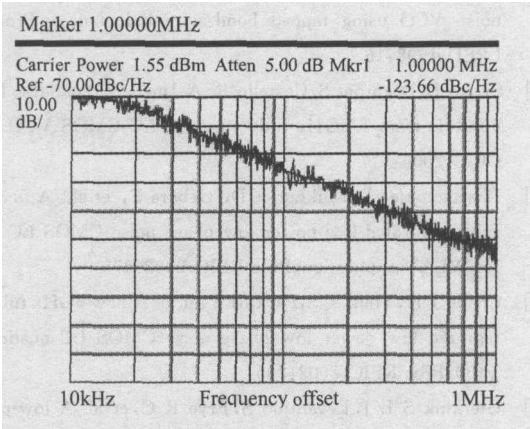

Fig. 10 Phase noise versus offset frequency

In order to compare the performance with other recently proposed VCOs in terms of center frequency, phase noise, power consumption, and tuning range[7], the power-frequency-tuning-normalized (PTFN) figure is defined as

$$\mathrm{PFTN} = 10\lg\left[\frac{kT}{P_{\mathrm{sup}}}\left(\frac{f_{\mathrm{tune}}}{f_{\mathrm{off}}}\right)^{2}\right] - S\Phi(f_{\mathrm{off}}) \quad (5)$$

where P_{sup} is the total DC power consumption in the VCO, $f_{\mathrm{tune}} = f_{\max} - f_{\min}$, f_{off} is the offset frequency from the carrier, and $S\Phi(f_{\mathrm{off}})$ is the phase noise. A large PFTN corresponds to a better oscillator. Table 2 shows performance of various LC VCOs and their PFTN.

Table 2 Comparison of various LC VCOs

VCO	Tech /μm	Power / mW	Freq / GHz	PFTN / (dBc · Hz^{-1})
Ref. [10]	0.35	12	1.45	- 9.5117
Ref. [11]	0.18	7	2.4	- 6.9770
Ref. [12]	0.35	28	12.5	- 29.2876
Ref. [13]	0.35	12.6	2.37	- 4.0084
Ref. [14]	0.35	12	1.3	- 9.1710
Ref. [15]	0.25	20	1.99	- 2.4499
Ref. [16]	0.5	3	1.4	- 9.2985
Ref. [17]	0.35	4	2.45	0.4283
Ref. [18]	0.24	5	5.8	- 13.6603
Ref. [19]	0.18	2.88	6	- 1.8403
Ref. [20]	0.25	21.88	5	- 3.7064
This work	0.25	15	4.728	- 3.0717

This work has the fourth largest PFTN among the fifteen oscillators. It achieves a good phase noise performance and large tuning range.

6 Conclusion

In this paper, a 4.8GHz fully integrated CMOS LC VCO, capable of providing a large tuning range (716MHz) and low phase noise (- 123.66Bc/Hz at 1MHz), has been presented. With symmetrical noise filter technique, the noise factor of LC oscillator can be lowered to its fundamental minimum. The noise at $2\omega_0$ in the current source and power line can be suppressed. The chip has been fabricated in 0.25μm RF CMOS process. The circuit consumes less than 6mA in the tuning range with the power supply voltage of 2.5V. The die area of the VCO core is about 0.7mm × 0.5mm.

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一种 LC 全集成、具有对称噪声滤波及宽调节范围的 4.8GHz CMOS 平衡振荡器*

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摘要: 将对称噪声滤波技术应用到 4.8GHz LC 全集成 VCO 设计中. 该 VCO 具有很低的相位噪声以及 716MHz 的调节范围, 在 SMIC 0.25μm 单层多晶、五层金属、n 阱 RF CMOS 工艺上实现, 在 2.5V 电源电压下工作电流仅为 6mA, 与常规 VCO 比较, 在相同条件下, 噪声性能改善了 6dBc/Hz. 芯片测试结果表明, 在偏离 4.8GHz 载波 1MHz 的地方相位噪声为 -123.66dBc/Hz, 该设计在锁相环及其他消费类电子产品中有广泛应用.

关键词: VCO; 对称噪声滤波; 射频集成电路; 片上电感; 开关电容

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