A New Low Voltage RF CMOS Mixer Design *

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Abstract: A new architecture of CMOS low voltage downconversion mixer is presented. With 1.452 GHz LO input and 1.45 GHz RF input, simulation results show that the conversion gain is 15dB, IIP3 is -4.5dBm, NF is 17dB, the maximum transient power dissipation is 9.3mW, and DC power dissipation is 9.2mW. The mixer's noise and linearity analyses are also presented.

Key words: downconversion mixer; CMOS process; noise and linearity analysis
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1 Introduction

In recent years, low voltage has become a target in most digital and analog integrated circuit applications. The most commonly used CMOS mixer topology is Gilbert mixer[1]. It has stacked structure, which limits its use in low supply voltage applications. Recently, a lot of efforts have been spent on the development of low-voltage CMOS RF mixers. In Refs. [2,3], the presented mixer avoids the stacking of transistors; tradeoff is that it suffers from a lower conversion gain for a given power. In Ref. [4], MOS transistor is used as a four-terminal device, RF and LO signals are applied to the gate and the back gate while the mixing product is extracted from the drain; this kind of mixer can be working on a low supply voltage, but it is difficult to predict the mixer performance due to the lack of adequate model for the transistor in such working mode. In Ref. [5], LC tanks are used in the mixer to achieve low voltage operation, but in CMOS technology, Q-value of the spiral inductor is relatively low, and the inductor occupies a lot of chips space.

In this paper, a high gain downconversion CMOS mixer with low supply voltage is presented; the topology of the mixer has never been reported previously. This new mixer does not need inductors, so it is relatively easy to fabricate.

2 Architecture of proposed mixer

Figure 1 shows the basic operating principle of the mixer. In this mixer core, transistor M1 is working in the triode region, transistor M2 is working in the saturation region, the current flow through M1 and M2 is equal, so that

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$$\frac{1}{2}\mu_n C_{on}\left(\frac{W}{L}\right)_2 (V_{B2} + v_{RF} - V_{Tn})^2 = \mu_p C_{xo}\left(\frac{W}{L}\right)_1 (\mathrm{VDD} - V_{B1} - v_{LO} - |V_{Tp}|)(\mathrm{VDD} - v) \quad (1)$$

Equation (1) can be changed into

$$v = \mathrm{VDD} - \frac{\frac{1}{2}\mu_n\left(\frac{W}{L}\right)_2 (V_{B2} + v_{RF} - V_{Tn})^2}{\mu_p\left(\frac{W}{L}\right)_1 (\mathrm{VDD} - V_{B1} - |V_{Tp}|)} \times \frac{1}{1 - \frac{v_{LO}}{\mathrm{VDD} - |V_{Tp}| - V_{B1}}} \quad (2)$$

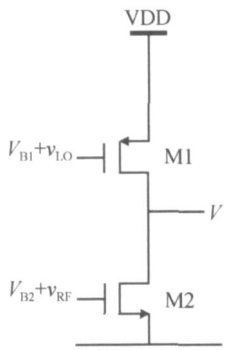

Fig. 1 Basic operating principle of the proposed mixer

V_{Tn} and V_{Tp} are the threshold voltage of M2 and M1, μ_n and μ_p are the mobilities of charge carriers of NMOS and PMOS transistors, W, L, and C_{ox} represent the transistor's width, length, and gate capacitance per unit area, respectively, V_{B1} and V_{B2} are DC bias voltages. The bias voltage and the aspect ratio of transistors are selected to guarantee

$$\frac{v_{LO}}{\mathrm{VDD} - |V_{Tp}| - V_{B1}} \ll 1 \quad (3)$$

Thus

$$\frac{1}{1 - \frac{v_{LO}}{\mathrm{VDD} - |V_{Tp}| - V_{B1}}} \approx 1 + \frac{v_{LO}}{\mathrm{VDD} - |V_{Tp}| - V_{B1}}$$

Then equation (2) can be approximated to

$$v \approx \mathrm{VDD} - \frac{\frac{1}{2}\mu_n\left(\frac{W}{L}\right)_2 (V_{B2} + v_{RF} - V_{Tn})^2}{\mu_p\left(\frac{W}{L}\right)_1 (\mathrm{VDD} - V_{B1} - |V_{Tp}|)} - \frac{\frac{1}{2}\mu_n\left(\frac{W}{L}\right)_2 (V_{B2} - V_{Tn})^2 v_{LO}}{\mu_p\left(\frac{W}{L}\right)_1 (\mathrm{VDD} - V_{B1} - |V_{Tp}|)} - \frac{\mu_n\left(\frac{W}{L}\right)_2 (V_{B2} - V_{Tn}) v_{RF} v_{LO}}{\mu_p\left(\frac{W}{L}\right)_1 (\mathrm{VDD} - V_{B1} - |V_{Tp}|)^2} \quad (4)$$

The last term in Eq. (4) is proportional to $v_{RF} v_{LO}$; this term can be used to achieve mixing.

Figure 2 is the complete schematic diagram of the proposed mixer, it has four sections: section 1 is composed of M1, M2, MM1, and MM2; section 2 is composed of M3, M4, MM3, and MM4; section 3 is composed of M5, M6, MM5, and MM6; and section 4 is composed of M7, M8, MM7, and MM8. The functions of the four sections are equal; each section consists of a mixer core (for example M1 and M2) and an output transconductance stage (for example MM1 and MM2, which are used to convert the output voltage of the mixer core into current). Transistors ML1 and ML2 have equal sizes. They are used to add the output transconductance stages' output current and convert the added current into voltage. V_{out} is the output voltage of the mixer. The balanced structure is chosen to reduce the feed through of LO and RF signals.

The commonly used active mixer, such as Gilbert mixer, is to achieve mixing through current, and it has a transconductance stage, which converts the RF input voltage into current, the LO signal switches the currents on and off, the output currents contains the mixing terms and are converted into voltage by using transistors or resistances as load. This kind of mixer has a procedure of converting voltage into current and then converting the current back into voltage, so the structure are complex and usually has stacked transistors. In this paper, first the RF input voltage is converted into current whose value is proportional to RF input voltage, then this current flows through LO controlled load, the resistance of this load has a term which is proportional to the LO voltage, so the output voltage has the mixing term. This kind of mixing procedure is rather simple; the mixer core only has two transistors, thus can be working in low supply voltage. The supply voltage can be adjusted lower depending on the system requirements.

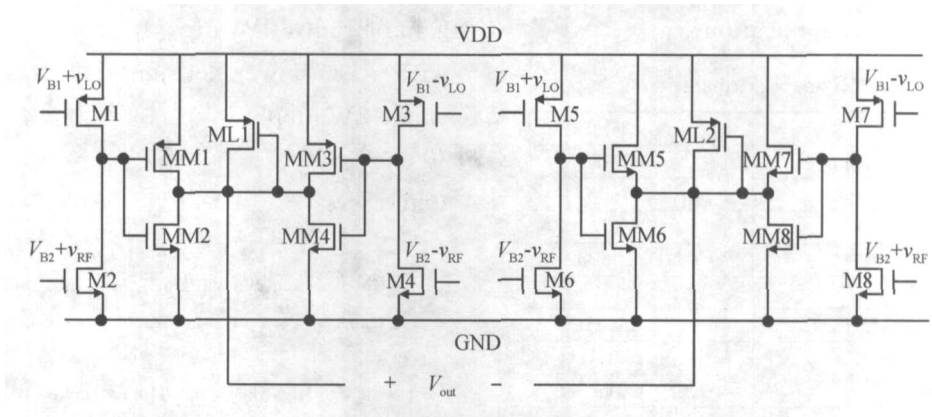

Fig. 2 Complete schematic diagram of the mixer

3 Mixer noise and linearity analysis

The design of the mixer requires a compromise ,and the performance parameters of the mixer should be carefully specified for different applications. In this paper ,the mixer is designed with high gain and low operating voltage , moderate NF (noise figure) ,and IIP3 (input referred third-order intercept point) .

The noise contribution of each transistor of the proposed mixer can be simulated and calculated by Cadence SpectreRF. This mixer is a low IF downconversion mixer ,and the thermal noise is the primary noise source.

$I_d^2(f)$ represents the thermal noise current in the drain due to the channel resistance. If the transistor operates in the triode region ,

$$I_d^2(f) = \frac{4kT}{r_{ds}} \tag{5}$$

Where r_{ds} is the channel resistance[6] .

For the long-channel transistor working in the saturation region[6] ,

$$I_d^2(f) = 4kT\gamma g_m \tag{6}$$

The coefficient γ is derived to be equal to 2/3 for long-channel transistors and may be needed to be replaced by a larger value for submicron MOSFETs.

Transistors M1 ,M3 ,M5 ,and M7 are working in the triode region ; their noise can be reduced by increasing their lengths. Simulation results show that transistors M2 ,M4 ,M6 ,and M8 contribute to most of the noise. As they are working in saturation region ,the transconductance of them should be large enough to minimize their equivalent noise voltage at the circuit input. After adjusting the parameter value of the mixer , simulation shows that it has a NF of 17dB.

Linearity is an important consideration in mixer design ,from Eqs. (1～4) ,it can be seen that to achieve high linearity , the condition of Eq. (4) must be satisfied. The linearity of the mixer is also determined by the linearity of mixer core and output transconductance stage. The linearity of the mixer core is determined by the lower MOS transistor in the mixer core , which is the RF input transconductance stage. Transconductance linearity can be improved by increasing the gate overdrive voltage ,but increasing the gate overdrive will increase power consumption. To increase the linearity of the output transconductance stage ,the aspect ratio of the two transistors of the transconductance stage is carefully chosen to cancel the nonlinear terms.

4 Simulation results

The mixer circuit is simulated using Cadence SpectreRF based on Dongbu 0. 25μm CMOS process. The simulation result of this mixer is summarized in Table 1. It is a low supply voltage high gain mixer , with moderate IIP3 and NF. The frequency of RF signal is 1. 452 GHz ; LO signal frequency is 1. 45 GHz ; this is because the mixer is de-

signed for L-band DAB applications.

Table 1 Mixer performance

Supply voltage	2V
DC power dissipation	9.2mW
Maximum transient power dissipation	9.3mW
Conversion gain	15dB
IIP3	-4.5dBm
NF	17dB
LO frequency	1.45GHz
RF frequency	1.452GHz
LO amplitude	0dBm
Technology	Dongbu 0.25μm

5 Conclusion

In this paper, a new CMOS RF downconversion mixer is presented. The mixer first converts the RF input voltage signal into current, then this current flows through a transistor working in the triode region whose resistance is modulated by the LO signal. This kind of mixer can work in a relatively low supply voltage.

This mixer achieved a simulated conversion gain of 15dB, IIP3 of -4.5dBm, and NF of 17dB, with a DC power consumption of 9.2mW from a single 2V supply.

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一种新的射频 CMOS 混频器结构*

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摘要: 提出了一种低电压高增益 CMOS 下变频混频器的新结构. 这个结构避免了堆叠晶体管, 因此可以在低电压下工作. 在 LO 信号的频率为 1.452GHz, RF 信号频率为 1.45GHz 的情况下, 仿真结果表明: 混频器的增益为 15dB, IIP3 为 -4.5dBm, NF 为 17dB, 最大瞬态功耗为 9.3mW, 直流功耗为 9.2mW. 并对该混频器的噪声特性和线性度进行了分析.

关键词: 下变频混频器; CMOS 工艺; 噪声和线性度分析
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