Design and Realization of a Monolithic GaAs 3Bit Phase Digitizing DAC

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Abstract : Design ,realization ,and test of a monolithic GaAs 3bit phase digitizing DAC for 3bit digital radio-frequency memory are detailedly described. The 0. 5μm fully ion-implanted GaAs MESFET is used to fabricate the circuit in Nanjing Electronic Devices Institute 's (NEDI 's) 75mm standard process line. The high-speed DAC is designed with on-wafer 50Ω I/O impedance matching. Test results show that its work bandwidth is more than 1. 5GHz ,and phase accuracy is better than 4 %. Its code conversion rate can be higher than 12Gbps.

Key words : phase digitizing DAC; high-speed; GaAs; DRFM
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1 Introduction

Digital radio-frequency memory (DRFM) is based on high-speed sampling and digital storage. It can save and reconstruct the radio and microwave signal ,so it has been widely used for radar and electronic countermeasure[1~3] . The most important parameter is instantaneous bandwidth (IBW) , which is determined by the bandwidth of high-speed ADC and DAC. But unfortunately ,high resolution ,high-speed ,wide bandwidth ADC and DAC are very difficult to be realized ,so ,DRFM is usually implemented using phase digitizing ADC and phase digitizing DAC which can be fabricated easily because of their smaller scale than the traditional ADC and DAC[2] . In this paper ,a monolithic 3bit high-speed ,wide bandwidth phase digitizing DAC using 0. 5μm fully ion implanted GaAs MESFET process is designed and realized for high speed 3bit DRFM system.

2 Circuit design

Phase digitizing DAC can reconstruct two orthogonal signals from Johnson codes. According to 3bit phase digitizing DAC ,the quantization interval is 45 °,and the voltage level is 5 steps after D/A conversion[2] . In order to obtain good phase accuracy and perfect frequency spectrum of output signals ,an approximate 3 ∶7 weighted summer will be an appropriate choice. So ,in theoretical the biggest magnitude of harmonic is - 16. 9dBc ,for 7th harmonics ,which is perfect for the further signal processing. The DAC 's block diagram is shown in Fig. 1.

The critical component of the phase digitizing DAC is the current source switch sequence , the same as the magnitude DAC. And each constant-current source will directly determine the perform-

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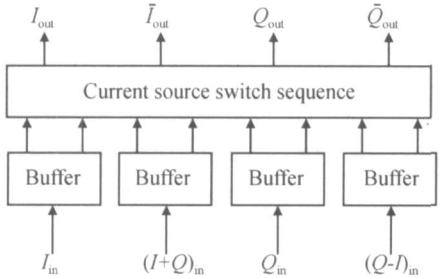

Fig. 1 3Bit phase digitizing DAC block diagram

ance of the whole DAC. Usually, the current source steering and weighted current source are used as current sequence[4~6]. For 3bit phase digitizing DAC, the circuit will need 8 current switches, which consists of only 2 types, so the weighted constant current source sequence is a most appropriate choice according to the scale of GaAs circuits. In order not to increase the scale of DAC, and to get good constant current property, the cascode constant-current is used, which has low offset, high gain and high output impedance. And this cascode arrangement desensitizes the current source FET from the variable source voltage of the differential switches. A single constant-current switch is shown in Fig. 2. Finally, the circuit is designed with on-wafer 50Ω I/O impedance matching for high-speed test and practical use.

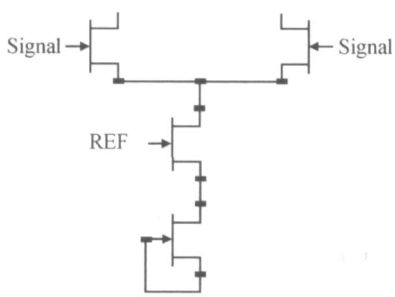

Fig. 2 Cascode source switch

Because DAC is sensitive to the device mismatching, the current switches should be placed carefully in order to assure chip layout to be symmetric both in geometry and in electricity[4]. Also, the current switches should output current symmetrically and the power dissipation should be uniform in total chip. During circuit layout, another point, to which should be paid more attention, is the side-gating effect[7]. At last, the DAC layout is illustrated in Fig. 3, and the current magnitude relative ratio of current switches is also shown.

$(Q-I)_{in}$ buffer		Q_{in} buffer	
$7I_{out}$	$3I_{out}$	$7Q_{out}$	$3Q_{out}$
$3I_{out}$	$7I_{out}$	$3Q_{out}$	$7Q_{out}$
I_{in} buffer		$(I+Q)_{in}$ buffer	

Fig. 3 3bit phase digitizing DAC switch sequence layout arrangement

3 Circuit realization

The DAC is fabricated using a fully 0.5μm ion-implanted MESFET technology in Nanjing Electronic Devices Institute (NEDI) 75mm standard process line. The active layer is formed by the Si ion-implantation at the energy of 60keV with a dose of $4.3\times10^{12}\ cm^{-2}$. The n^+ region is also formed by Si ion-implantation with two steps of implantation, 120keV and 60keV with the same dose $3\times10^{13}\ cm^{-2}$. Ohmic contacts are formed by alloying the standard AuGeNi metallization. The 0.5μm TiPtAu gates are recessed for a normal pinch-off of -1.3V. Two levels of metallization, separated by silicon nitride dielectric, are used for interconnections. The traditional photolithography and lift-off techniques are used. The typical transconductance is g_m = 180mS/mm. Figure 4 shows the photograph of the fabricated 3bit phase digitizing DAC chip.

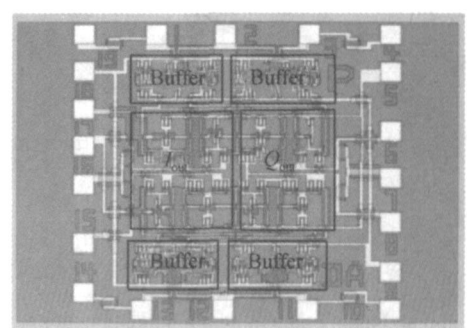

Fig. 4 Photo of GaAs 3bit phase digitizing DAC

4 Circuit test

The circuit should be mounted on a specific

high-frequency test board and bonded with golden wire in order to test its performance. According to the principle of 3bit phase digitizing DAC, four signals should be applied to the circuit[2]. Each signal consists of four continuous 1 states and four continuous 0 states, but there is 1/8 period delay between every two adjacent signals. The output two signals, I_{out} and Q_{out}, are sent to high-speed oscilloscope through DC block. In order to get accurate results, the phase differences of the test lines are first determined by net analyzer. The results are shown in Fig. 5. Therefore, the test results from oscilloscope should eliminate the phase errors from the test lines. Figure 6 shows the uncorrected results with 1.5 GHz input signals. The corrected results are shown in Fig. 7. Because each period of input signal has 8 phase states, the result corresponds to 12 Gbps code conversion rate. The output signals have 100 mV_{pp} at 50Ω load impedance.

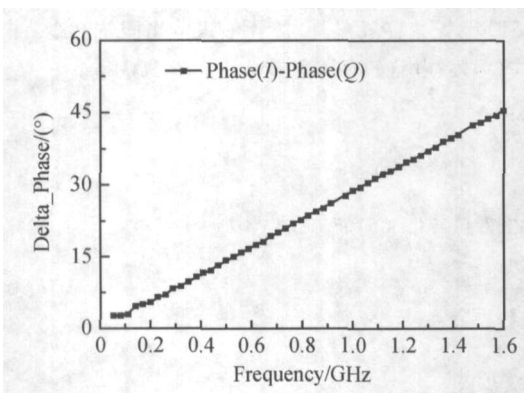

Fig. 5　Phase difference between two test line for output signals

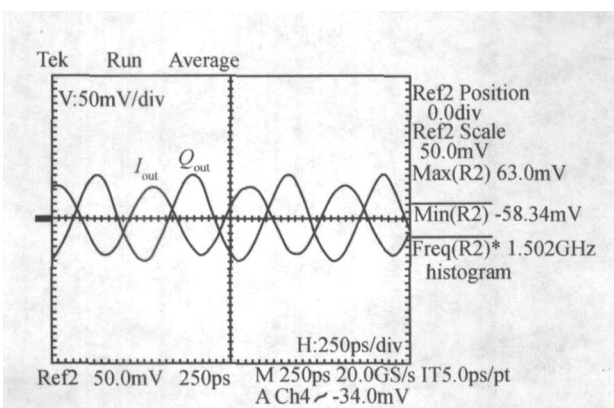

Fig. 6　Output signals at 1.5 GHz input signals

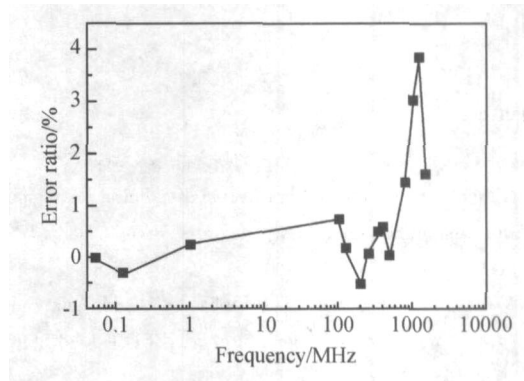

Fig. 7　Phase accuracy in work bandwidth

The above result is directly tested by oscilloscope whose input impedance is 50Ω. If using the oscilloscope as load of DAC, the amplitude of output signal will be doubled. The most important performance of phase digitizing DAC is its phase accuracy of two output orthogonal signals, which can be charactered by the deviation of phase difference of output signals from 90°, like Eq. (1)

$$\text{Phase accuracy}(f) = 100\% \times (\text{Phase}(I_{out}(f)) - \text{Phase}(Q_{out}(f)) - 90°)/360° \quad (1)$$

Figure 7 shows the DAC's phase accuracy at some typical frequency points. Obviously, the phase accuracy is below 4% at all work bandwidth, and is below 2% at most frequency points.

All the above test results indicate that this 3bit phase digitizing DAC has good phase accuracy and more than 1.5 GHz work bandwidth. Its code conversion rate can be higher than 12 Gbps.

5　Conclusion

Design, fabrication, and test of a monolithic GaAs 3bit phase digitizing DAC for 3bit phase DRFM system are detailedly discussed. 0.5μm fully ion-implanted GaAs MESFET process is used to fabricate the circuit in NEDI's 75mm standard process line. This high-speed phase digitizing DAC is designed with on-wafer 50Ω I/O impedance matching and the test results show that its working bandwidth is more than 1.5 GHz, and code conversion rate can be higher than 12 Gbps. Its phase accuracy is better than 4% in the full work band-

width.

References

[1] Gilbert B K. Design and fabrication of a digital RF memory using custom designed GaAs integrated circuits. GaAs IC Symposium, 1985: 173

[2] Vu T T, Hattis J M. A GaAs phase digitizing and summing system for microwave signal storage. IEEE J Solid-State Circuits, 1989, 24(1): 104

[3] Herskovitz D. A sampling of digital RF memories. Journal of Electronic Defense, 1998, March: 51

[4] Wikner J J, Tan N. CMOS data converters for communications. USA: Kluwer, 2000

[5] Seki S, Saito T, Fujishiro H I, et al. An 8bit 1GHz digital to analog converter using 0.5μm gate inveted HEMTs. Proc Int Electron Devices Meeting, 1988: 770

[6] Feng S, Sauereer J, Seitzer D. Mismatch of current sources and accuracy of D/A converters in 0.5μm GaAs/GaAlAs HEMT technology. IEEE International Symposium on Circuits and Systems, 1992, 1: 224

[7] Liu Yi, Dutton R W, Deal M D. Sidegating effect of GaAs MESFET's and leakage current in a semi-insulating GaAs substrate. IEEE Electron Device Lett, 1990, 11(11): 505

单片 GaAs 3bit 相位 DAC 的设计与实现

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摘要: 详细论述了用于数字射频存储器系统的单片超高速 GaAs 3bit 相位 DAC 的设计、制造及测试. 在南京电子器件研究所标准 75mm GaAs 工艺线采用 0.5μm 全离子注入 MESFET 工艺完成流片. 芯片输入输出阻抗实现在片 50Ω 匹配. 测试结果表明, 其工作带宽大于 1.5GHz, 相位精度小于 4%, 电路的码流翻转速率大于 12Gbps.

关键词: 相位数字化 DAC; 超高速; GaAs; DRFM

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