An Asynchronous Implementation of Add-Compare-Select Processor for Communication Systems *

Zhao Bing , Qiu Yulin , L ü Tieliang , and Hei Yong

(*Institute of Microelectronics , Chinese Academy of Sciences , Beijing* 100029 , *China*)

Abstract : A novel asynchronous ACS(add-compare-select) processor for Viterbi decoder is described. It is controlled by local handshake signals instead of the globe clock. The circuits of asynchronous adder unit ,asynchronous comparator unit ,and asynchronous selector unit are proposed. A full-custom design of asynchronous 4-bit ACS processor is fabricated in CSMC-HJ 0. 6μm CMOS 2P2M mixed-mode process. At a supply voltage of 5V ,when it operates at 20MHz ,the power consumption is 75. 5mW. The processor has no dynamic power consumption when it awaits an opportunity in sleep mode. The results of performance test of asynchronous 4-bit ACS processor show that the average case response time 19. 18ns is only 82 % of the worst-case response time 23. 37ns. Compared with the synchronous 4-bit ACS processor in power consumption and performance by simulation ,it reveals that the asynchronous ACS processor has some advantages than the synchronous one.

Key words : asynchronous circuits ; Viterbi decoder ; ACS ; response time
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1 Introduction

The advantages claimed for asynchronous circuits are that such circuits are capable of operating at the maximum speed determined by the intrinsic hardware (they can be designed for average-case rather than worst-case performance) ,they have no problems with clock skew and they may have a substantial low-power advantage over synchronous circuits[1]. Asynchronous circuits are one possible solution to clock distribution problems in VLSI circuits[2].

As a method of decoding convolution codes , the Viterbi algorithm is widely applied to digital communications and data compression[3]. Although the Viterbi algorithm is computationally efficient , its high-speed implementation is limited by the critical path that exists in the ACS processor.

Aria *et al*.[4] have brought forward an asynchronous ACS for communication systems. In their design ,there are two signal lines that need to be represented as a three-state code. The signals coding is complex. The adder and comparator use Manchester architecture. C program is used to simulate the delay through the ACS processor. It assumed that the delay through all of the gates is the same. There are no final experimental results in

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Zhao Bing male ,was born in 1977 ,PhD candidate. His current research interests are in the high performance and low power asynchronous circuits design.

Qiu Yulin male ,professor ,advisor of PhD candidates. His research interests are in the design of high performance and low power integrated circuits.

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their paper.

In this paper, effort is mainly paid to investigate the power saving and high performance potential of asynchronous circuits in CMOS VLSI design. Using the simple signal-coding mode, an asynchronous ACS processor for communication systems is designed. It is controlled by local handshake signals instead of the globe clock. The simulation and experimental results of the asynchronous ACS processor are presented. The asynchronous ACS processor has some advantages in performance and power consumption compared with the synchronous one.

2 Viterbi decoder and ACS

Viterbi decoder is a kind of maximum likelihood decoder used for the decoding of convolution codes[5]. Its main operations are calculations of BM (branch metric), PM (path metric) and trace-back. BM calculation is the operation of addition and subtraction in little bit (< 5bit) and the amount of BM calculation is less than those of PM and trace-back. PM calculation includes large numbers of ACS (add-compare-select) operations. Trace-back is a series of memory reading and writing operation.

Convolution codes have three main parameters (k, n, L). It means that blocks of input data are k bits, blocks of output data are n bits, and outputs are correlative not only with the current block of input data but also with the L - 1 blocks of previous inputs. In Viterbi decoder, one block of input data will operate $2n$ addition and subtraction for BM, $2L$ - 1 ACS operations for PM. The numbers of trace-back operation depend on the size of memory and the trace-back depth. When trace-back depth is $5L$ and using the least amount of memory, each block of input data needs $5L$ read operations.

In Viterbi decoder, the ACS module deals with the concurrent addition of operands to evaluate different path metrics, and selection of one of the metrics in accordance with the relative magnitudes of these metrics[6]. In practical application, k is commonly 1, n is 2 or 3, and L is between 5 and 9. It indicates that the ACS operations are the most frequent operations and one of the performance bottlenecks of Viterbi decoder.

3 Asynchronous logic and asynchronous data-path

3.1 Asynchronous logic

The characteristic of asynchronous logic systems controls the sequence of logic circuits by local handshake signals instead of the globe clock in synchronous circuits.

3.2 Asynchronous data-path

Asynchronous systems use asynchronous data-path. The beginning of the data-path is controlled by a determinate signal and the end of the data-path is controlled by another determinate signal.

The main influences on performance of integrated circuits are cell circuits and connection of them. The high performance of asynchronous circuits is realized by the average performance of data-path from another point of view.

The base cells of data-path are realized by domino complex gates. The connection of each series uses the one-hot decoding. The base data-path uses the handshake module connection to form the subsystem.

4 Function and structure of asynchronous ACS

4.1 Asynchronous adder

When an asynchronous adder completes the addition operation, a done signal will be produced. It is the base characteristic of asynchronous adder. Garside[7] has brought forward a new design of asynchronous adder's functions and circuits. It provides a moulding board for asynchronous adder. The asynchronous adder also has the structure of

RCA ,CLA ,and so on. 2bit CLA has less quantity of transistors ,lower power consumption ,less average delay and less worst-case delay than RCA[8]. The asynchronous 2bit adder unit is showed in Fig. 1. The adder in this paper has higher speed than synchronous one , however , the area is smaller. The output signals are simple compared with Aria Eshraghi 's asynchronous adder.

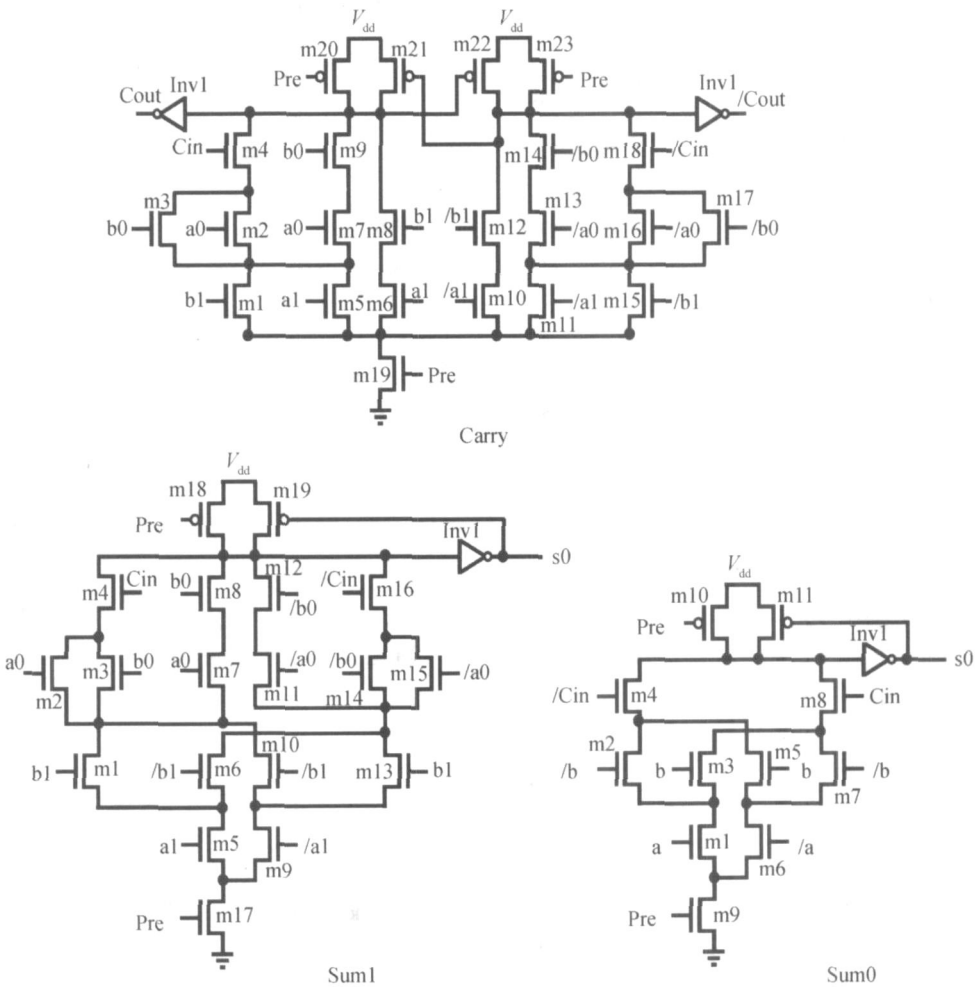

Fig. 1 Asynchronous 2bit adder unit

4.2 Asynchronous comparator

The comparator depends more on data correlation than adder. The usual comparator structure is based on subtraction operation or concatenation of 1bit compare cells. In his paper , the asynchronous comparator is based on concatenation of 1bit compare cells. The comparator uses the 2 'complement. Types of the 1bit compare cell are signed comparator unit and unsigned comparator unit , shown in Figs. 2 and 3. The comparator has a done signal generator that produces a done signal after comparison results are ready. It has fewer transistors than Aria Eshraghi 's asynchronous comparator in Manchester architecture.

4.3 Asynchronous selector

The asynchronous selector is based on concatenation of 1bit selector units as shown in Fig. 4. It is actually an asynchronous multiplexer. This MUX is controlled by handshake signal. It works after input data and control signal are ready. The selector has a done signal generator that produces a done signal after output data are ready.

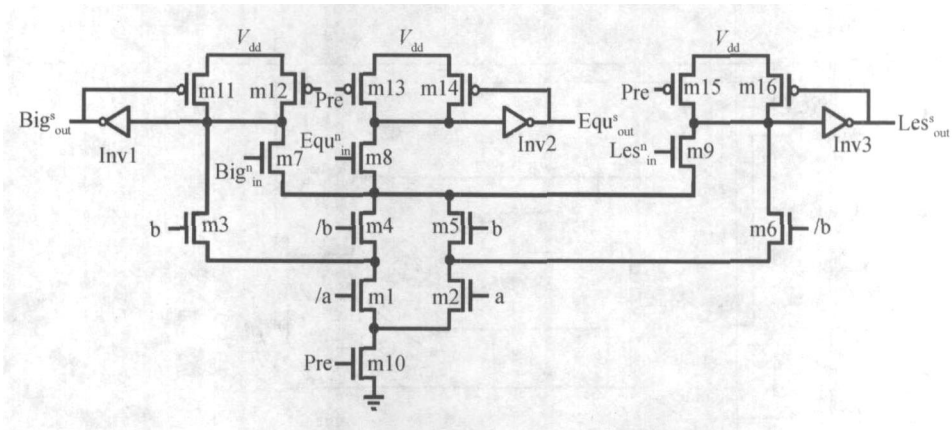

Fig. 2　Asynchronous 1bit signed comparator unit

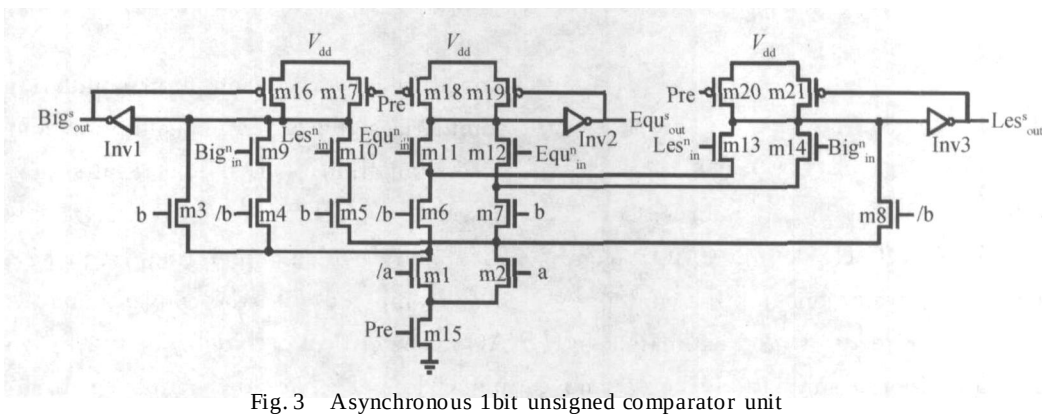

Fig. 3　Asynchronous 1bit unsigned comparator unit

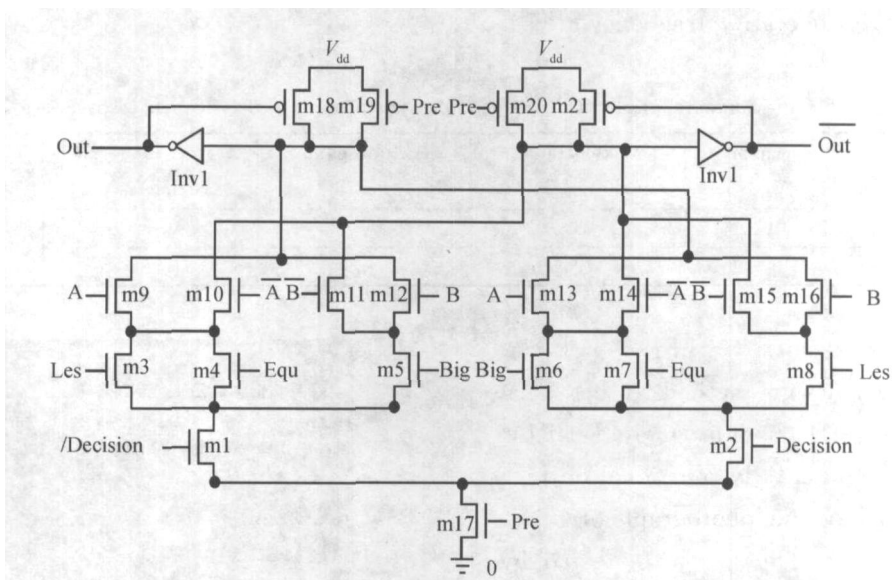

Fig. 4　Asynchronous 1bit selector unit

4.4　Asynchronous ACS

An asynchronous data-path ACS has two asynchronous adders, one asynchronous comparator and one asynchronous selector, shown in Fig. 5. It is controlled by local handshake signals instead of the globe clock. Each device is an unattached cell. There is no clock-distributing problem as synchronous circuits have. The asynchronous ACS processor only works when the input data are ready.

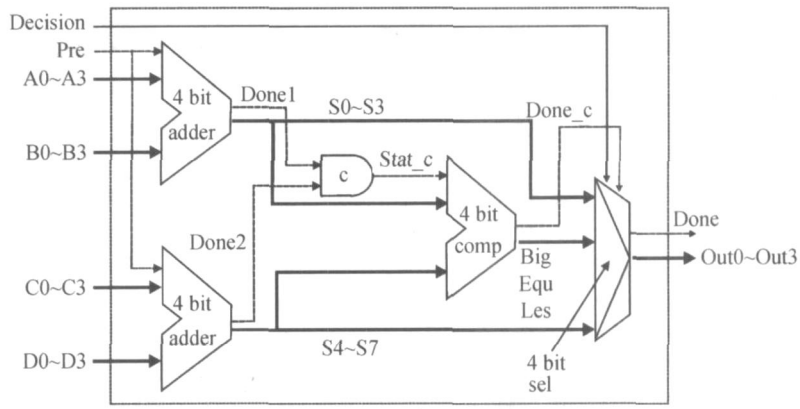

Fig. 5 Architecture of asynchronous 4bit ACS

5 Results

Another synchronous 4bit ACS processor is designed using the CSMC-HJ 0.6μm CMOS technology library. The power consumption and performance of two architectures are estimated by HSPICE simulation. In the simulation, there is no consideration of input and output pads. A 5V supply voltage and 20MHz operating frequency are assumed in power consumption simulation. Table1 summarizes the power consumption and performance simulation results. The results show that the power of asynchronous ACS design is reduced by 24% and the max operating frequency is up by 30%, compared with the conventional synchronous ACS. The critical path delay of synchronous ACS is much longer than the response time of asynchronous ACS.

Table 1 Comparison of synchronous and asynchronous 4bit ACS processors

	Power consumption / mW	Max operating frequency/ MHz	Critical path delay/ ns	Average case response time/ ns	Worst-case response time/ ns
Synchronous ACS	55.91	70	14.2	—	—
Asynchronous ACS	42.46	100	—	6.81	8.08

The asynchronous 4bit ACS processor is designed in full-custom design method. It has been fabricated in CSMC-HJ 0.6μm CMOS 2P2M mixed-mode process and is fully functional on first pass silicon. The layout and photograph of it are shown in Figs. 6 and 7. The chips are tested by HP82000 IC validity check system. Figure 8 shows that the actual output waves (Out0～Out3) coincide with the expectations. At a supply voltage of 5V, when it operates at 1MHz, the power consumption is 7.5mW; when it operates at 20MHz, the power consumption is 75.5mW.

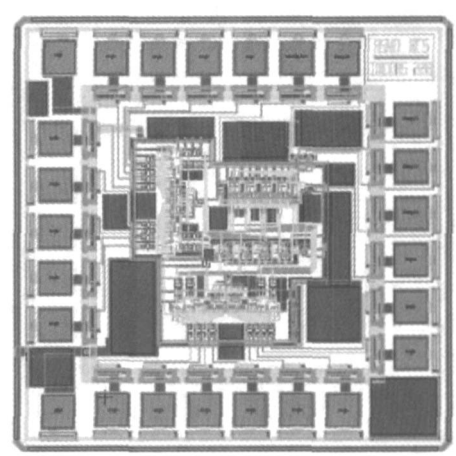

Fig. 6 Layout of asynchronous 4bit ACS

The high performance of asynchronous circuits

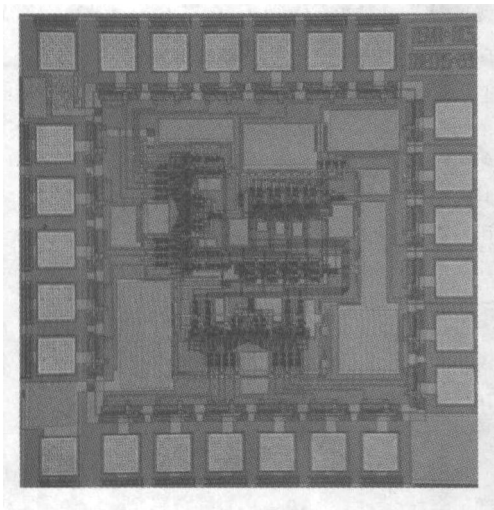

Fig. 7 Photograph of asynchronous 4bit ACS

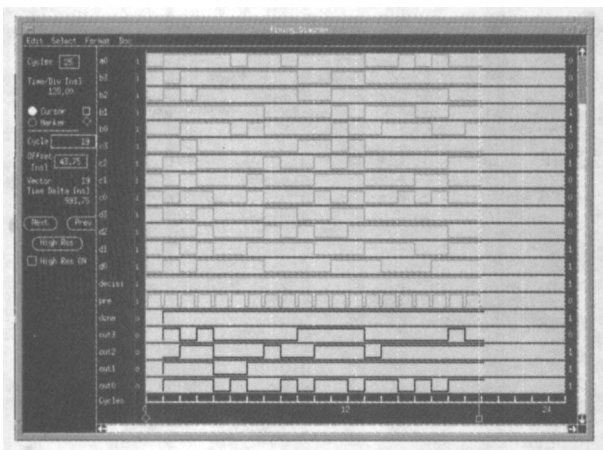

Fig. 8 Test waves in HP82000

is realized by the average performance of data-path. Response time is the popular measure for the performance of asynchronous circuits[9]. The response time of an asynchronous data-path is the delay between the request and the done signal. There are two kinds of response time, the worst-case response time and the average case response time. The worst-case response time is mainly dependent on the circuit structure and implementation. However, the average case response time relies not only on the circuit structure but also on the input data. The results of performance test of asynchronous 4bit ACS processor show that the worst-case response time is 23.37ns and the average case response time is 19.18ns.

In asynchronous circuits, delays are often data dependent. To improve the performance of asynchronous circuits, effort should be mainly paid to the average performance analysis of asynchronous data-path. A novel average performance analysis method, which is based on simulation and multi-delay modeling, is used to analysis the asynchronous ACS processor. The input data are divided into several classes. Every class of data has similar delay. The sizes of MOS transistors that mainly affect the average response time are adjusted. More attention is also paid to the delays of done signal generators to reduce the average response time.

6 Conclusion

In this paper, an asynchronous 4bit ACS processor for communication systems is implemented in 0.6μm CMOS mixed-mode technology. The asynchronous ACS processor will increase the efficiency for Viterbi decoder. It is a good way to realize the high-speed implementation of Viterbi algorithm. Compared with the synchronous 4bit ACS processor in power consumption and performance by simulation, it reveals that the asynchronous ACS processor has some advantages than the synchronous one. But asynchronous circuits need some additional circuits to control operation by using handshake signals. These circuits would go against power consumption and layout area of global circuit. It is a challenge for asynchronous logic design techniques to be largely accepted by mainstream designers because of the lack of design tools, algorithms, and methodology.

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一种适用于通讯系统的异步加-选择-比较器 *

赵 冰 仇玉林 吕铁良 黑 勇

(中国科学院微电子研究所, 北京 100029)

摘要: 介绍了一种适用于 Viterbi 解码器的异步 ACS(加法器-比较器-选择器)的设计. 它采用异步握手信号取代了同步电路中的整体时钟. 给出了一种异步实现结构的异步加法单元、异步比较单元和异步选择单元电路. 采用全定制设计方法设计了一个异步 4-bit ACS ,并通过 0. 6μm CMOS 工艺进行投片验证. 经过测试 ,芯片在工作电压 5V , 工作频率 20MHz 时的功耗为 75. 5mW. 由于采用异步控制 ,芯片在"睡眠"状态待机时不消耗动态功耗. 芯片的平均响应时间为 19. 18ns ,仅为最差响应时间 23. 37ns 的 82 %. 通过与相同工艺下的同步 4-bit ACS 在功耗和性能方面仿真结果的比较 ,可见异步 ACS 较同步 ACS 具有优势.

关键词: 异步集成电路; Viterbi 解码器; 加法器-比较器-选择器; 响应时间

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赵 冰 男,博士研究生,主要研究方向为高性能、低功耗异步集成电路设计.

仇玉林 男,教授,博士生导师,主要从事高性能、低功耗集成电路设计研究.

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