# Strained-Si pMOSFETs on Very Thin Virtual SiGe Substrates *

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**Abstract :** Strained-Si pMOSFETs on very thin relaxed virtual SiGe substrates are presented. The 240nm relaxed virtual $Si_{0.8}Ge_{0.2}$ layer on 100nm low-temperature Si (LT-Si) is grown on Si(100) substrates by molecular beam epitaxy. LT-Si buffer layer is used to release stress of the SiGe layer so as to make it relaxed. DCXRD , AFM , and TEM measurements indicate that the strain relaxed degree of SiGe layer is 85 % , RMS roughness is 1. 02nm , and threading dislocation density is at most $10^7 cm^{-2}$. At room temperature , a maximum hole mobility of strained-Si pMOSFET is $140 cm^2/(V \cdot s)$. Device performance is comparable to that of devices achieved on several microns thick relaxed virtual SiGe substrates.

**Key words :** strained-Si ; virtual SiGe substrates ; pMOSFET
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## 1 Introduction

Strained Si/relaxed SiGe heterostructures offer both high mobility and cutoff time for field effect and bipolar transistor technologies[1]. A recently obtained record of effective hole mobility is 30 % higher than that of conventional Si pMOSFETs[2].

Some strained-Si/relaxed-SiGe heterostructure devices require relaxed SiGe layers to serve as virtual substrates. To date , the most successful approach to achieve high quality virtual SiGe substrates is to grow a compositionally graded SiGe buffer layer on a Si(100) substrate[3]. But the virtual SiGe substrates are either too thick ( > 1μm) for subsequent device processing or plagued by high threading dislocation density. MBE growth of these structures leads to an unacceptable long growth time and a high material consumption. The thick virtual SiGe substrates by UHVCVD growth suffer from a low thermal conductivity and a loss of planarity. The self-heating of the strained Si devices arises from the lower thermal conductivity of SiGe compared with Si[4] and results in a significantly elevated channel temperature[5]. Recently , a highly interesting technique has been reported as effective in achieving a very thin strain relaxed SiGe buffer with a low threading dislocation density. Such as , growth of defect-rich layers at low temperatures[6] or $He^+$ ions implantation into Si substrate[7]. Up to now , SiGe buffers with 30 % Ge content and about 70 % relaxation have been realized with an excellent surface quality and a threading defect density of approximately $10^7 cm^{-2}$.

In this paper , we have studied the growth of very thin virtual SiGe substrates with low dislocation density using low temperature Si technology. Strained-Si pMOSFETs on 240nm thick virtual $Si_{0.8}Ge_{0.2}$ substrates are prepared. Finally we describe performance enhancements in strained-Si pMOSFETs on very thin virtual SiGe substrates.

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## 2 Material growth and device fabrication

Base requirement for growth of strained-Si layer is to obtain high-quality relaxed virtual SiGe substrates on Si substrates. In this study, samples are grown on 75mm n-type Si(100) substrate in a SIVA32(France) solid source MBE system and investigated by in suit reflection high-energy electron diffraction, which consists of 10nm Si/100nm low-temperature Si(LT-Si)/240nm $Si_{0.8}Ge_{0.2}$. A 10nm Si buffer layer was grown at 550 ℃ to cover the damaged layer generated by mechanical polishing of Si substrate. A 100nm LT-Si buffer layer was grown at 400 ℃, the surface atom migration was significantly restricted during the growth, and a high density point of defects was generated. Therefore, when the $Si_{0.8}Ge_{0.2}$ was grown on LT-Si buffer layer, the strain existing at the $Si_{0.8}Ge_{0.2}$/LT-Si interface could be released easily by generating dislocations in the LT-Si buffer layer at relatively low temperature. The $Si_{0.8}Ge_{0.2}$ layer was grown at 550 ℃.

The strain status and alloy composition are determined from X-ray double-crystal diffraction (DCXRD). Figure 1 shows the X-ray rocking curve of the sample. These measurements confirm that Ge composition of the SiGe layers is effectively controlled at about 20%. The degree of relaxed $R$ is approximate 85%. Such a thickness is much smaller than that of compositionally graded SiGe buffer systems having the same degree of relaxation. The surface morphology of sample is examined by atomic force microscope(AFM). The result is shown in Fig. 2, and RMS roughness is 1.02nm in a scanning range of 25μm ×25μm. Transmission electron microscopy (TEM) image of sample as shown in Fig. 3, reveals that most or all of the threading dislocations are contained below SiGe/LT-Si interface. This indicates that the threading dislocations density is at most $10^7 cm^{-2}$.

The structure of this strained-Si pMOSFET is shown in Fig. 4. The valence band offset of strained Si/relaxed SiGe is higher than 120meV[8], which is enough to confine holes in the relaxed SiGe layer. When the voltage of the gate is low, the concentration of holes in the interface of strained-Si/relaxed SiGe is larger than that in the interface of $SiO_2$/strained Si; consequently, the device works in the buried channel mode with high hole mobility due to lower interface scattering. When the voltage of the gate is high, the majority carriers are located in the interface of $SiO_2$/strained Si, so the device works in the surface channel mode with high hole mobility due to high hole mobility in the strained Si.

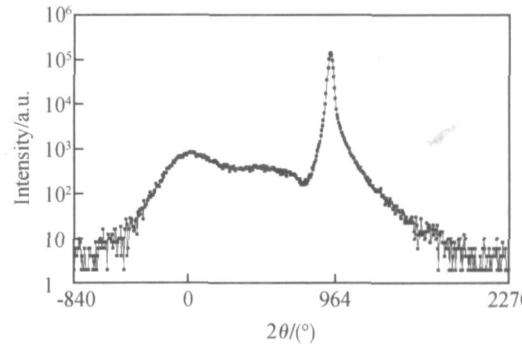


Fig. 1 X-ray rocking curve of virtual SiGe substrates

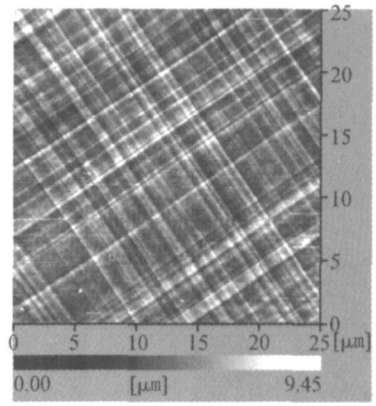


Fig. 2 AFM image of virtual SiGe substrates

The whole layers are grown by MBE at 550 ℃ expect LT-Si buffer layer, and four layers are deposited in turn: 10nm Si buffer/100nm LT-Si/240nm $Si_{0.8}Ge_{0.2}$/17nm strained Si. In order to fabricate pMOSFET, we add a light phosphorous doping to obtain a weak n-type. Devices are fabricated with standard CMOS fabrication process, expect

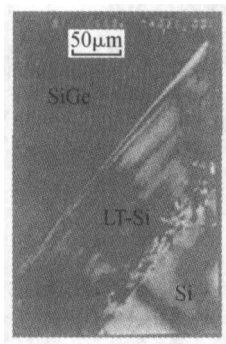


Fig. 3　TEM image of virtual SiGe substrates

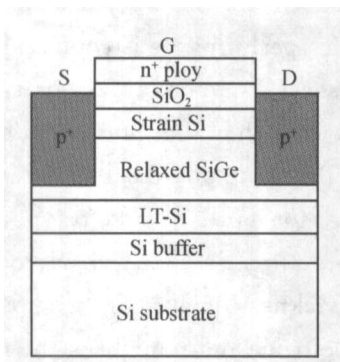


Fig. 4　Structure of strained-Si pMOSFET

for the gate oxidation and annealing. The high quality thin $SiO_2$ is prepared by dry oxidation for 5min, wet oxidation for 10min and dry oxidation for a further 5min at 800 ℃. After oxidation, more than 10 % HCl gas was added, which reduces the parasitic charge densities significantly. The RTA condition is 850 ℃, 60s, $N_2$ atmosphere. This gate oxide thickness is measured to be 10nm by the ellipsometer. All subsequent processing is carried out at 850 ℃ or below to avoid relaxing the strained Si layers and Ge atoms diffusing into the channel, or else the device performance will ultimately degrade.

Under the same process, we fabricate the strained-Si pMOSFET and the conventional bulk Si pMOSFET. The channel length and width of the devices are 4. 2 and 52μm, respectively.

## 3　Results and discussion

The DC output characteristics of the strained-Si pMOSFET are shown in Fig. 5. The strained-Si devices show good liner and saturation characteristics. The threshold voltages of strained-Si and bulk Si pMOSFET are approximately - 0. 4 and - 1. 0V.

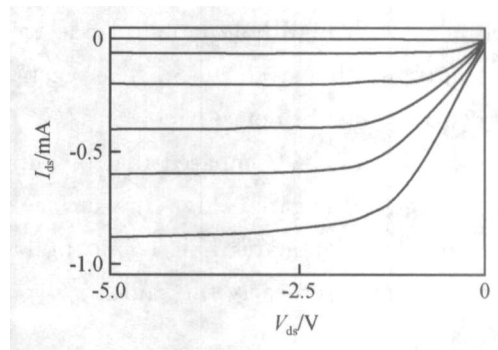


Fig. 5　Output characteristics of strained-Si pMOSFET

The leakage current of strained-Si devices at $V_{gs} = 0$V is observed, as shown in Fig. 6. It can be seen that the leakage current is 7nA at $V_{ds} = -5$V and $V_{gs} = 0$V. From these results, the low leakage current is thought to reduce self heating effects due to the very thin SiGe layer, and low defect density in strain Si layer and virtual SiGe substrates.

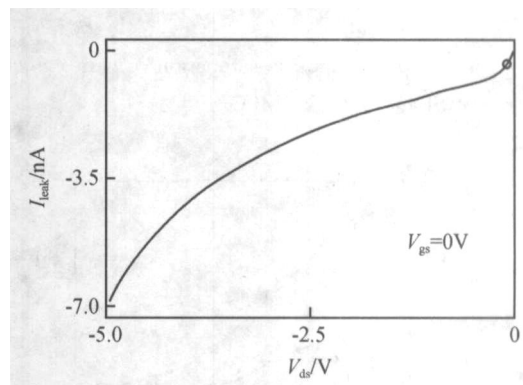


Fig. 6　Drain leakage current at $V_{gs} = 0$V as a function of $V_{DS}$

The linear transconductance ($g_m$) can be gotten from the output characteristics. Figures 6 and 8 show the transconductances $g_m$ and the hole mobility as a function of $V_{gs}$, respectively. The hole mobility of devices can be calculated by $I_{ds} \approx (W/L)\mu_P C_{ox}(V_{gs} - V_T)V_{ds}$, when $V_{ds} \ll V_{gs} - V_T$.

Figures 7 and 8 indicate, when the voltage of the gate is low, transconductances and hole mobility of strained-Si device are higher than those of bulk Si. This indicates that the majority holes are in the buried channel. The strained-Si/relaxed-SiGe

interface is with low threading dislocation density and interface scattering. When the voltage of the gate increases, the device works in the surface channel mode with high hole mobility due to high hole mobility in the strained Si. The peak hole mobility for strained-Si device is 140cm$^2$/(V ·s), which is enhanced 50 % compared that of bulk Si. But the voltage of the gate is high, the surface scattering mechanism dominates hole conduction, both transconductances are nearly the same.

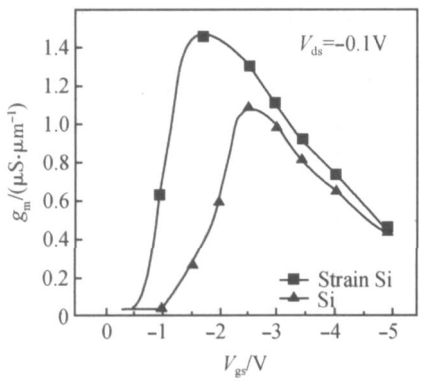


Fig. 7 Transconductance as a function of gate voltage of strained-Si and bulk Si pMOSFET

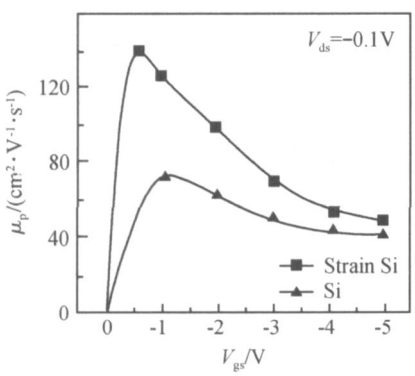


Fig. 8 Hole mobility as a function of gate voltage of strained-Si and bulk Si pMOSFET

The device performance of strained-Si pMOSFET is roughly equal to that in the most previous reports[1,9]. Further investigation is necessary to increase Ge composition, grow virtual SiGe substrates/LT-Si buffer layer optimized, and reduce defects.

## 4 Conclusion

In conclusion, relaxed virtual SiGe substrates on 100nm LT-Si layer can be reduced to 240nm. The very thin virtual SiGe substrates have low threading dislocation density, smoother surface in comparison with the comparable compositionally graded SiGe layers. Strained-Si pMOSFETs on very thin relaxed virtual SiGe substrates are presented. The device performance is comparable to those achieved on several microns thick virtual SiGe substrates, and better than that of conventional bulk Si pMOSFET. This kind of virtual substrates is an interesting tool for both n- and p-type strained-Si MOSFET structures in Si-based microelectronics. The thin thickness makes it compatible with CMOS technologies and minimizes the influence of low thermal conductivity of SiGe alloys.

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# 薄虚拟 SiGe 衬底上的应变 Si pMOSFETs *

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**摘要**：成功地试制出薄虚拟 SiGe 衬底上的应变 Si pMOSFETs. 利用分子束外延技术在 100nm 低温 Si(LT-Si)缓冲层上生长的弛豫虚拟 $Si_{0.8}Ge_{0.2}$ 衬底可减薄至 240nm. 低温 Si 缓冲层用于释放虚拟 SiGe 衬底的应力，使其应变弛豫. X 射线双晶衍射和原子力显微镜测试表明：虚拟 SiGe 衬底的应变弛豫度为 85%，表面平均粗糙度仅为 1.02nm. 在室温下，应变 Si pMOSFETs 的最大迁移率达到 140cm$^2$/(V·s). 器件性能略优于采用几微米厚虚拟 SiGe 衬底的器件.

**关键词**：应变硅；锗硅虚衬底；p 型场效应晶体管
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