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Improving Detectability of Resistive Shorts in FPGA Interconnects*

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Abstract: The behavior of resistive short defects in FPGA interconnects is investigated through simulation and theoretical analysis. The results show that these defects result in timing failures and even Boolean faults for small defect resistance values. The best detection situations for large resistance defect happen when the path under test makes a v-to-v' transition and another path causing short faults remains at value v. Small defects can be detected easily through static analysis. Under the best test situations, the effects of supply voltage and temperature on test results are evaluated. The results verify that lower voltage helps to improve detectability. If short material has positive temperature coefficient, low temperature is better; otherwise, high temperature is better.

Key words: FPGA; resistive shorts; detect; improvement

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1 Introduction

Short faults are an important type of manufacturing defects[1~4]. Using the spot defect model, it was shown that about 50% of all fabrication defects in CMOS circuits could be categorized as shorts[5]. A resistive short is a failure mode in which the short connection between two circuit nodes is resistive, increasing circuit delay and introducing timing faults. For small values of the defect resistance, they even cause hard failures. Unlike an ASIC, most of the area of an FPGA is dedicated to the routing resources and wires of different lengths; hence, short defects are more probable.

Testing of resistive short defects in FPGA interconnects was discussed only in Ref. [6]; the behavior of resistive short defects was studied through detailed simulation. Based on the test vectors applied, short defects result in timing failures and even Boolean faults for small defect resistance values. The authors believed that the best detection situation happens when the paths under test are making simultaneous transitions in the opposite directions. But this conclusion is only suitable for small defect resistance value, and yet not for large resistance value. Thus, the application of best detection situation may be limited.

In this paper, we addressed the problem of resistive short defects in FPGA interconnects and drew a conclusion about the best test situation different from Ref. [6] based on theoretical analysis and simulation results. Under the best detection conditions, several improved test techniques were studied. Test configurations that satisfy the best conditions are similar to Ref. [6]; we did not give detailed description in order to save space.

2 Fault model and analysis

2.1 FPGA architecture and circuit model

The FPGA model we used is a two dimension-

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al array of configurable logic blocks (CLBs). CLBs are connected through switch matrices and line segments. Inside each switch matrix there are programmable interconnect points (PIPs) and pass transistors controlled by user-programmable SRAM cells. These PIPs provide selective connectivity between pairs of line segments connected to the switch matrix. The PIP acts as a switch. If the switch is closed, the connection between two lines is established. Figure 1 shows the architecture of Xilinx Virtex FPGAs[6].

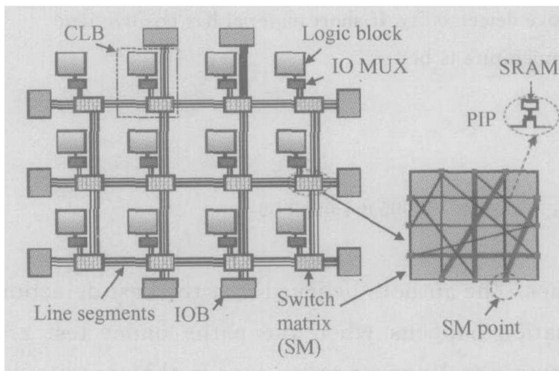

Fig. 1 Virtex FPGA architecture

The resistive short circuit model is shown in Fig. 2, where stuck-on transistors are closed PIPs. The choice of identical inverter paths is because of buffered segments and regular structure of FPGAs in which identical paths under test can be generated in test configurations[7]. We use a simple RC interconnect model with wire resistances R_1 and R_2, parasitic capacitances C_1 and C_2. Resistive short defect is marked by R_b.

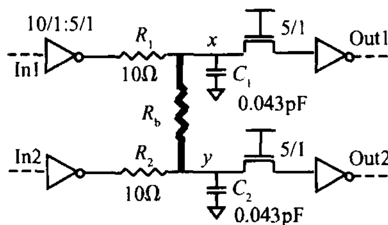

Fig. 2 Circuit model

2.2 Static analysis

In the static analysis, it is assumed that input signals remain constant and output signals are stable. Therefore, all interconnect parasitic capacitances and sink capacitances are ignored. When In1 and In2 are both high or low, the bridge has no impact on the circuit. When In1 is low and In2 is high, the circuit is shown in Fig. 3. A short fault results in intermediate voltage levels of bridged nodes. The logic interpretation of the intermediate voltage depends on the threshold voltage of driven inverter. For simplification, we assume the threshold voltage of inverter in Fig. 3 to be 50 % V_{dd}. An accurate theoretical analysis of the static behavior was provided in Ref. [8].

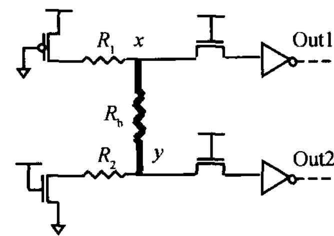

Fig. 3 Circuit model when (In1, In2) = (low, high)

Figure 4 gives the simulation result of Out1 for (In1, In2) = (low, high). It is clear when short resistance is below critical resistance R_c[9~11] there is a Boolean fault. According to Ref. [12], 10 % of resistive shorts have value of larger than 1kΩ. These shorts result in critical fault which must be tested through dynamic analysis.

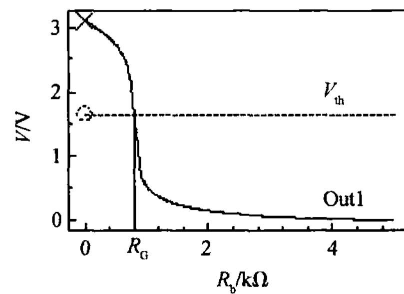

Fig. 4 Out1 voltage and short resistance

2.3 Dynamic analysis

In the dynamic analysis, there are four types of input signals: high, low, rising, and falling. For the sake of detecting delay of Out1 path, the input of the path must not be constant. There are totally 8 cases of input type combinations for In1 and In2. In

order to find best test condition, we carried out HSPICE and theoretical analysis of short-defected circuit of several resistance values. TSMC 0.35μm BSIM3 model was used throughout the paper. Delays of x from HSPICE, T_{sim}, were listed in Table 1.

The increased delay formula for resistive bridges[12] is

$$d' = \{-l\log_2[(0.5-h)/(g-h)]-1\}d_1 \quad (1)$$

where d_1 is the nominal delay of x, l, g, and h are chosen according to Table 2 in Ref. [12]. The delays with different input combinations, T_{the}, can be easily calculated and were summarized in Table 1.

The conclusion from HSPICE consists with that from theoretical analysis. As the results show, for a v-to-v' transition on the Out1 path, if the Out2 path remains at value v, it introduces more transition delay to the Out1 path. However, if the Out2 path remains at v', it speeds up the Out1 path transition. When two paths are making transitions in the opposite directions, it may cause an increased delay or a decreased delay. When two paths are making transitions in the same direction, delay is almost same as that of no short circuit, so is not be listed in Table 1. When Out1 path has a v-to-v' transition and Out2 path remains v, the increased delay is larger than that for opposite transition. Larger delay means higher detectability. Therefore, to maximize the delay, the best-input patterns for larger resistance value defect are (rising, low) and (falling, high). As for small resistance value defect, we can detect it easily using static analysis.

Table 1 Delay of x for several short resistance values 10^{-10}s

In1	In2	No short		50000Ω		20000Ω		10000Ω		5000Ω		1500Ω	
		T_{sim}	T_{the}	T_{sim}	T_{the}	T_{sim}	T_{the}	T_{sim}	T_{the}	T_{sim}	T_{the}	T_{sim}	T_{the}
Rising	High	1.11		0.99	0.9	0.85	0.70	0.68	0.52	0.45	0.32	0.07	0.07
	Low			1.14	1.15	1.16	1.24	1.21	1.39	1.34	1.68	1.95	2.55
	Falling			1.01	1.01	0.88	0.94	0.71	0.85	0.48	0.74	0.07	0.31
Falling	High	1.40		1.42	1.46	1.49	1.57	1.6	1.79	1.79	2.27	4.35	4.76
	Low			1.27	1.20	1.14	0.99	0.98	0.83	0.78	0.66	0.51	0.43
	Rising			1.33	1.33	1.21	1.29	1.1	1.27	0.98	1.40	1.20	2.73

The fault model in Fig. 2 is the same as that of Ref. [6], but our conclusion of the best detection situation is different from that of Ref. [6]. They drew their conclusion only based on Boolean fault, but we considered both Boolean fault and critical fault at the same time. The authors of Ref. [6] believed that the best detection situation happens when the paths under test are making simultaneous transitions in the opposite directions. The simulation results of Ref. [6] are shown in Fig. 5 in which Boolean faults are shown as shaded boxes. For small resistance value defect, when In1 and In2 occur opposite transition, there is a Boolean fault no matter what In1 is. But for larger resistance value defect, no any Boolean fault exists with all kinds of input combinations. Thus, their conclusion is only suitable for small resistance value defect, and yet not for larger resistance value defect.

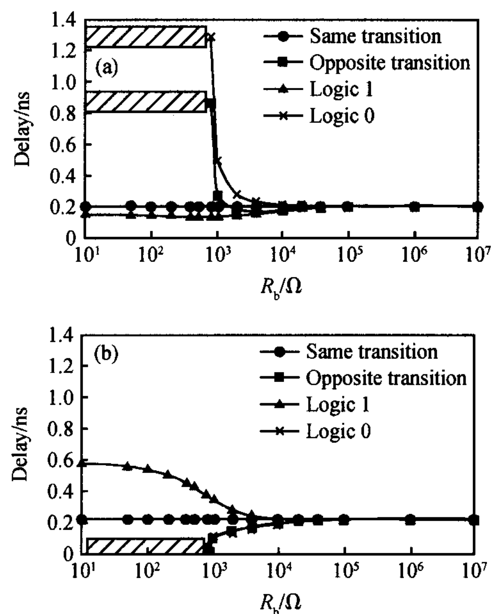

Fig. 5 Simulation results of Out1's transition for different input combinations[6] (a) In1 = Rising; (b) In1 = Falling

Even for small resistance value defects, they were detected using dynamic analysis[6] which is more complex than static analysis that was used by us. Therefore, our best detection condition is much easily carried out and more efficient than that in Ref. [6] because we can detect not only small resistance value defect but also larger resistance value defect.

3 Dependence on test condition

The objective of this section is to find dependence of testability on test condition under the best test patterns. The delay ratio is used as the detectability metric[13], which is the delay of the defective circuit over the delay of the good circuit; a larger value means higher resolution in detecting the delay fault. In what follows, we carried out the analysis for (In1, In2) = (falling, high). The analysis for another best pattern (In1, In2) = (rising, low) is similar.

From the circuit analysis in Ref. [12], we found when (In1, In2) = (falling, high) the circuit for Out1 in Fig. 2 can be simplified to the circuit in Fig. 6, where

$$C_e = C_1 + \frac{(R_n + R_2)^2}{(R_n + R_2 + R_b)^2} C_2 \tag{2}$$

$$R_e = (R_1 + R_p) \,/\!/\, (R_n + R_2 + R_b) \tag{3}$$

$$m = \frac{R_n + R_2 + R_b}{R_1 + R_p + R_n + R_2 + R_b} \tag{4}$$

where R_p and R_n are pull-up and pull-down resistances.

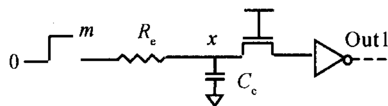

Fig. 6 Approximation circuit model for Out1 when In1 is falling and In2 is high

Define the delay of good circuit at x as d_0, and that of Fig. 6 as d_1, the delay ratio d_1/d_0 can be computed as

$$\frac{d_1}{d_0} = \frac{R_n + R_2 + R_b}{R_1 + R_p + R_n + R_2 + R_b} \times \left[1 + \frac{(R_n + R_2)^2}{(R_n + R_2 + R_b)^2} \times \frac{C_2}{C_1}\right] \times \left|\log_2\left[\frac{1}{2} \times \left(1 - \frac{R_1 + R_p}{R_n + R_2 + R_b}\right)\right]\right| \tag{5}$$

We assumed $R_1 = R_2$ and $C_1 = C_2$, because short defects often occur between the metal wires in the same layer and FPGA interconnect has the regular architecture. In order to obtain equal rising and falling time, pMOS and nMOS in the inverter should have similar on-state resistances, i. e. $R_n \approx R_p$. Based on the assumption, Equation (5) can be approximated to

$$\frac{d_1}{d_0} \approx \frac{1}{1 + \dfrac{1}{\dfrac{2(R_n + R_1)}{R_b} + \dfrac{R_b}{R_n + R_1} + 2}} \times \left|\log_2\left[\frac{1}{2} \times \left(1 - \frac{1}{1 + \dfrac{R_b}{R_1 + R_n}}\right)\right]\right| \tag{6}$$

MATLAB computation results show delay ratio is an increasing function of $(R_n + R_1)/R_b$.

3.1 Dependence on supply voltage

When one decreases supply voltage, R_n is increased. Therefore, delay ratio under lower voltage is larger than that of nominal voltage, vice versa. HSPICE simulations for the circuit model shown in Fig. 2 with various supply voltage values were performed. Figure 7 shows the resulting delay ratios as a function of defect size. As we expected, when supply voltage (2.5V) is below nominal voltage, the delay ratio is higher than that of the nominal voltage (3.3V). The improvement is obvious when defect resistance is below 3kΩ (larger than 25%), and maximal improvement is 160%. Furthermore, critical resistance value increases with decreased supply voltage.

3.2 Dependence on test temperature

Because interconnect resistance is much smaller than short defect resistance causing critical faults, according to Eq. (8), dependence of delay ratio on temperature is dominated by material of

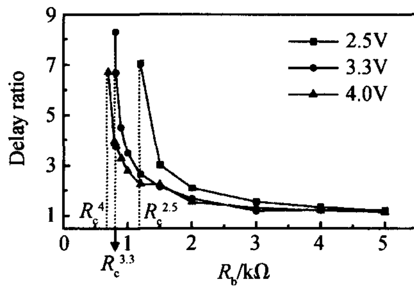

Fig. 7 Dependence of delay ratio on supply voltage

short defect. If short material has positive temperature coefficient, low temperature is better; otherwise, high temperature is better.

For example, we assumed defect material was Al that has positive temperature coefficient. HSPICE simulations for the circuit model shown in Fig. 2 with three test temperature 0, 25, and 100 ℃ were performed. These temperatures are used in the package tests in industry[14]. Figure 8 shows the resulting delay ratio as a function of defect size. As we expected, the delay ratio is higher when temperature (0 ℃) lower than room temperature (25 ℃). The improvement in delay ratio is obvious when defect resistance below 1.5kΩ (larger than 10 %), and maximal improvement reaches 46 %. As shown in Fig. 8, critical resistance value increases with decreased test temperature.

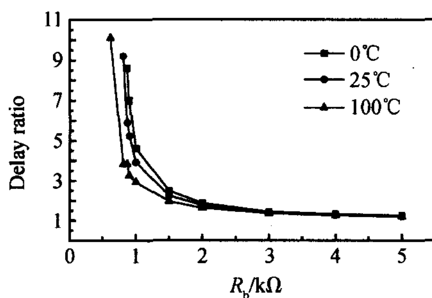

Fig. 8 Dependence of delay ratio on temperature

4 Examples

To verify the conclusions above, we carry out experiments for a small (500Ω) and larger (1500Ω) resistance value defects, assuming defect material Al. Simulation results for different input combinations are shown in Table 2, where B represents a Boolean fault. For a 500Ω short defect, any input combinations generate Boolean faults; so we can detect it easily using static analysis. For a 1500Ω short defect, we can find the delay for In2 = Low (High) is largest when In1 = Rising (Falling). Therefore, the best-input patterns for larger resistance value defect are (rising, low) and (falling, high). Simulation results for a 1500Ω short defect under different test conditions are shown in Table 3 when (In1, In2) = (falling, high). Lower voltage and temperature are helpful to increase delay, even causing Boolean faults. Obviously, the experimental results match the theoretical results well.

Table 2 Delay of x with different input combinations

10^{-10} s

In1	In2	500Ω	1500Ω
Rising	High	B	0.07
	Low	B	1.95
	Falling	B	0.07
Falling	High	B	4.35
	Low	B	0.51
	Rising	B	1.20

Table 3 Delay of x under different test conditions

10^{-10} s

Test conditions		1500Ω
Voltage/ V	2.5	B
	3.3	4.35
	4	3.04
Temperature/ ℃	0	5.05
	25	4.35
	100	3.55

5 Conclusion

In this paper, we investigated the problem of resistive short defects in FPGA interconnects. Results show small short defect can result in hard failure and large defects generate critical fault. Based on theoretical analysis and dynamic simulation, we achieved the best test situation different from Ref. [6]. The best test condition happens when the Out1 path makes a v-to-v' transition, and Out2 path remains at value v for large resistance

value defect. And small defects can be detected easily through static analysis. Our best detection condition is much easily implemented and more efficient than that of Ref. [6] because we can detect not only small resistance value defect but also larger resistance value defect. Under the best detection situations, the effects of test conditions on results were studied. The results verify lower voltage helps to improve detectability. If short material has positive temperature coefficient, low temperature is better; otherwise, high temperature is better.

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改善 FPGA 互连阻性短路的测试能力*

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摘要: 通过 HSPICE 模拟和理论分析研究了 FPGA 互连中的阻性短路缺陷行为. 结果表明, 阻性短路产生了时序故障, 小电阻缺陷甚至产生了布尔故障. 对于大电阻缺陷, 当被测通路进行 v-to-v' 转换, 且引起短路故障的另一条通路保持 v 值时, 最好检测方式发生. 另外, 使用静态分析可以很容易检测到小电阻缺陷. 在最好检测方式下, 评估了电源电压和温度对测试结果的影响. 结果表明低电压有助于改善测试, 短路材料有正温度系数时, 低温测试较好, 反之高温测试较好.

关键词: FPGA; 阻性短路; 检测; 改善

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