Bandwidth Design for CMOS Monolithic Photoreceiver *

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Abstract: A monolithic photoreceiver which consists of a double photodiode (DPD) detector and a regulated cascade (RGC) transimpedance amplifier (TIA) is designed. The small signal circuit model of DPD is given and the bandwidth design method of a monolithic photoreceiver is presented. An important factor which limits the bandwidth of DPD detector and the photoreceiver is presented and analyzed in detail. A monolithic photoreceiver with 1.71GHz bandwidth and 49dB transimpedance gain is designed and simulated by applying a low-cost 0.6μm CMOS process and the test result is given.

Key words: double photodiode; optoelectronics integrated circuit; photoreceiver
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1 Introduction

Electrical interconnects on boards and between boards have been becoming a problem due to the increase of chip and system clock frequencies. Optical interconnects and optical data transmissions via fibers are alternative to avoid the problem[1]. Photoreceiver is a key device in optical interconnects and optical data transmissions. To achieve high speed and high volume, the integration of the photodetector with the required circuitry is desirable for optical receiver. The optoelectronic integrated circuit (OEIC) receiver will be needed in the next years for optical interconnects and optical data transmissions.

Most modern CMOS and BiCMOS processes implement self-adjusting well formation and require only the lithography step for the formation of both n^- and p^- type wells[2]. The p^- type doping concentration in an n^+/p^- substrate photodiode is consequently higher than $10^{16}cm^{-3}$, and the space-charge region is very thin. Therefore, a large portion of the carriers is photo-generated outside the space-charge region and a large contribution of slow carrier diffusion to the photocurrent leads the bandwidth to be less than 7MHz. To avoid slow diffusion of photo-generated carriers without conducting additional process steps, a double photodiode (DPD) was suggested by Woodward and Krishnamoorthy[3,4]. The DPD detectors can be fabricated in commercial CMOS technologies without any process modification. Their OEIC receiver can operate at 1Gbit/s in 0.35μm CMOS process[4,5]. However, the design method of the amplifier in the OEIC receiver was not presented in Refs. [4,5] and the desired performance is difficult to achieve in a 0.6μm CMOS process; besides, the amplifier instability might be high due to their simple circuit structures.

In general, wide-band transimpedance amplifiers (TIAs) are the necessary front-ends for opto-

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electronic communication systems. To achieve higher gain and to get wider bandwidth, Park and Yoo[6,7] demonstrated a 2.5GHz regulated cascade (RGC) TIA in a 0.6μm CMOS process. But their design method is just useful for RGC TIA not for a monolithic photoreceiver because the photodiode model they used is a PIN (positive, intrinsic, and negative region diode) model, which can not be manufactured in standard CMOS process. In addition, although the RGC TIA can efficiently isolate the large junction capacitance of the photodiode, the slow diffusion carrier of any photodiode manufactured in standard CMOS process will affect bandwidth of photoreceiver, to which their report[6,7] did not take into account.

In this paper, we will demonstrate the bandwidth design method for an OEIC receiver. And we will firstly (to our knowledge) give a circuit model of the DPD detector. The simulation results and the chip photograph of the photoreceiver will be also illustrated.

2 Structure and model of DPD detector

DPD is a CMOS-process-compatible detector. Figure 1 shows its cutaway sketch[3,4]. p-diffusion is connected to the transimpedance amplifier, n-well is tied to the detector bias (positive) and the guard ring is grounded. So, this structure forms two junctions: n-p junction of n-well to p-substrate and p-n junction of p-diffusion to n-well. The n-well region is surrounded by the grounded p guard ring. Inside the n-well, an interdigitated network of the p source-drain material forms the active terminal of the detector. The n-well is tied to the detector bias and intends to screen the active terminal from the slowly responding bulk-generated carriers.

High capacitance is generally believed to be the main reason of limiting the detector's speed, but we have found a remarkable restrictive factor by the method of device simulation. Though the

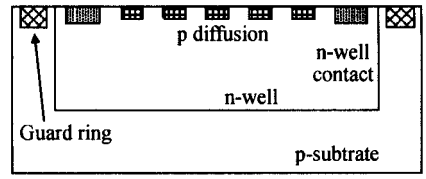

Fig. 1 Cross section of DPD detector structure

slow carrier diffusion in p-substrate can be avoided by applying two vertically arranged p-n junctions, it is unavoidable that the hole carrier diffuses slowly to the p-n junction in n-well. The noticeable slow speed of the hole carrier brings the DPD detector a delay time. Through a detailed simulation of the carrier movement[8], we can reasonably assume that the diffusing distance of the hole carrier is 1/2～1/3 of the depth of the n-well. Then, the circuit model of DPD detector which has taken the limitation factor into account can be deduced.

The circuit model of DPD detector can be obtained by consulting the circuit model of PIN photodiodes which has been presented in Ref. [9]. We can ignore the delay time generated by p-diffusion and depletion region. Then the current equation can be written as

$$I_{op} = C_{n0}\frac{dV_p}{dt} + \frac{V_p}{R_p} + \frac{V_p}{R_{pd}} + \beta_p P_{in} + I_{po} \quad (1)$$

$$I_J = I_p + I_i + C_j\frac{dV_j}{dt} + I_s \quad (2)$$

where I_{op} is the photo-generation current in n-well, C_{n0} is a constant and it can be thought as a capacitance, $V_p = \frac{qP_n}{C_{n0}}$, q is the electronic charge, P_n is the total excess holes in n-well, $R_p = \frac{\tau_p}{C_{n0}}$, τ_p is the hole lifetime in n-well, $R_{pd} = \mathrm{ch}(W_n'/L_p) - 1$, $\mathrm{ch}(x) = \frac{e^x + e^{-x}}{2}$, W_n' is the distance of the drifting hole carrier in n-well, L_p is the diffusion length of hole in n-well, I_{po} is a steady state value for the optical input, I_j is the output current of DPD detector, I_i is the photo-generation current in depletion region, $I_{op}/I_i \approx W_n'/W_i$, W_i is the depletion region width of the p-n junction. $I_p = \frac{V_p}{R_{pd}} + \beta_p P_{in} + I_{po}$, C_j

is the junction capacitance, I_s is the dark current under the inverse bias state, and it is independent of V_j. Let

$$V_p = V_{p0} + \Delta V_p, \quad I_p = I_{p0} + \Delta I_p,$$
$$I_{op} = I_{op0} + \Delta I_{op}, \quad I_i = I_{i0} + \Delta I_i,$$
$$V_j = V_{j0} + \Delta V_j,$$

where V_{p0} is the steady state value of V_p, etc., the disturbance equations of (1), (2) are given by

$$\Delta I_{op} = C_{n0} \frac{d\Delta V_p}{dt} + \frac{\Delta V_p}{R_p} + \frac{\Delta V_p}{R_{pd}} \tag{3}$$

$$\Delta I_j = \Delta I_p + \Delta I_i + C_j \frac{d\Delta V_j}{dt} \tag{4}$$

where $\Delta I_p = \frac{\Delta V_p}{R_{pd}}$. Although $\beta_r P_{in}$ is not a steady state value for the optical input, it is very small and independence of V_p, so it can be ignored in the disturbance equations. From Eqs. (3), (4), the small signal model for DPD detector can be constructed (see Fig. 2). R_s is the contact resistance.

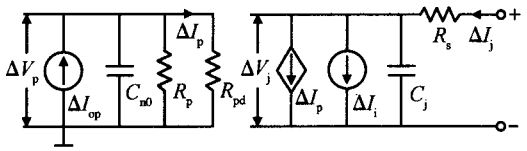

Fig. 2　Small signal model of DPD detector

3　Analysis of RGC TIA circuit and bandwidth of photoreceiver

Figure 3 shows the schematic diagram of a RGC TIA[6,7]. M1 and M2 make up of the RGC input stage and form the first gain stage. Due to the low impedance characteristics of the RGC circuit, the total input capacitance determines the non-dominant pole of the amplifier. A common drain stage (M3) is inserted between the RGC input stage and the transconductance stage, and works as a voltage follower. Without this voltage follower stage, the large input capacitance of M4 will restrict the potoreceiver's bandwidth. Meanwhile, this inserted voltage follower reduces the open-loop gain. Therefore it is necessary to optimize the size of M3 for the desired bandwidth and gain. The common source stage (M4) is the second voltage gain stage. For wide bandwidth, its gate-width should be selected to be small because of C_{gs4}. M5 and M6 are output buffers.

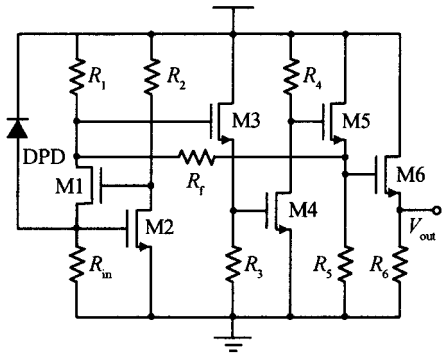

Fig. 3　Schematic diagram of RGC TIA

The input impedance of the RGC TIA can be yielded by small signal analysis,

$$Z_{in} = \frac{1}{g_{m1}(1 + g_{m2} R_2)} \tag{5}$$

where $1 + g_{m2} R_2$ is the voltage gain of the local feedback stage (M2 and R_2). The input impedance is so small that it efficiently isolates the large input parasitic capacitance, resulting in a potential for wideband width. The dominant pole of the amplifier is determined by the time constant (τ_1) at the highest impedance node which is the drain of M1,

$$\tau_1 = (R_1 \parallel R_{fm})(C_{d1} + C_{g3} + C_{fm}) = \frac{1}{\omega} \tag{6}$$

where C_{d1} is the total drain capacitance of M1, C_{g3} is the total gate capacitance of M3, R_{fm} and C_{fm} are the Miller's equivalent resistance of the feedback resistance R_f and Miller's equivalent capacitance of the parasitic capacitance of C_f, respectively. R_{fm} and C_{fm} are given by

$$R_{fm} = \frac{R_f}{1 + g_{m4} R_4} \tag{7}$$

$$C_{fm} = \frac{C_f}{1 + g_{m4} R_4} \tag{8}$$

There are several other non-dominant poles in the RGC TIA, which have been detailedly analyzed in Refs. [6,7]. In order to analyze RGC TIA and DPD together we can neglect the other non-dominant poles in RGC TIA.

Two poles are determined by the time constant (τ_2) and (τ_3) at the circuit model of the DPD

detector in Fig. 2,

$$\tau_2 = C_{n0}(R_p \parallel R_{pd}) = \frac{1}{\omega_2} \quad (9)$$

$$\tau_3 = C_j(R_s + Z_{in}) = \frac{1}{\omega_3} \quad (10)$$

For the low-pass characteristic with three poles, we get

$$A(j\omega) = \frac{A_{low}}{(1 + j\frac{\omega}{\omega_1})(1 + j\frac{\omega}{\omega_2})(1 + j\frac{\omega}{\omega_3})} \quad (11)$$

where A_{low} is the low-frequency gain. At 3dB frequency, the denominator of Eq. (16) should be

$$\left|(1 + j\frac{\omega}{\omega_1})(1 + j\frac{\omega}{\omega_2})(1 + j\frac{\omega}{\omega_3})\right| = \sqrt{2} \quad (12)$$

or

$$\left|1 - j\frac{\omega}{\omega_1}\times\frac{\omega}{\omega_2}\times\frac{\omega}{\omega_3} + j\omega\left(\frac{1}{\omega_1} + \frac{1}{\omega_2} + \frac{1}{\omega_3}\right) - \left(\frac{\omega^2}{\omega_1\omega_2} + \frac{\omega^2}{\omega_1\omega_3} + \frac{\omega^2}{\omega_2\omega_3}\right)\right| = \sqrt{2}$$

Assuming $\omega < \sqrt{\omega_i\omega_j}$ ($i, j = 1, 2, 3$ and $i \neq j$), the all product terms can be neglected. The one imaginary term will remain when

$$\frac{1}{\omega} = \frac{1}{\omega_1} + \frac{1}{\omega_2} + \frac{1}{\omega_3} = \tau_1 + \tau_2 + \tau_3 \quad (13)$$

where ω is the effective 3dB frequency and is the sum of three time constants. Thus, the - 3dB bandwidth of the OEIC receiver f_{3dB} is approximately given by

$$f_{3dB} = \frac{1}{2\pi(\tau_1 + \tau_2 + \tau_3)} \cong$$

$$(1 + g_{m4}R_4)/\{2\pi R_f(C_{d1} + C_{g3} + \frac{C_j}{(1 + g_{m4}R_4)}) +$$

$$2\pi(1 + g_{m4}R_4)(C_{n0}R_{pd} + C_j(R_s + Z_{in}))\} \quad (14)$$

According to Eq. (14), for wider bandwidth, R_{pd} should be reduced, that means W_n' should be reduced according to $R_{pd} = \mathrm{ch}(W_n'/L_p) - 1$. The W_n' is determined by selecting CMOS process and has the relationship with the depth and the doping concentration of the n-well in the DPD. The other factors to increase bandwidth are the C_j and Z_{in} (the series resistor R_s of the DPD detector is very small), C_j is determined by the area of the DPD detector, Z_{in} can be controlled by choosing the input stage of the RGC TIA. R_f also should be increased. Nevertheless, the affection degree of the junction capacitor C_j for 3dB bandwidth is not obvious, because the input impedance Z_{in} is very small due to the structure of the RGC input stage.

4 Simulation results

Figure 4 shows that W_n' and area of the DPD detector have obviously different influence on the bandwidth of the monolithic photoreceiver. W_n' is the diffusing distance of the hole carrier and it is about 1/2 ~ 1/3 of the depth of the n-well. For a 0.6μm CMOS process, the depth of n-wells is approximately 1 ~ 2μm, then W_n' is about 0.3 ~ 1.0μm. In Fig. 4(a), when the area of the DPD detector is fixed at 20μm × 20μm and W_n' value changes from 0.3 to 1.0μm, the bandwidth will decrease from 2.73 to 0.49GHz correspondently. When W_n' is fixed at 0.4μm and the area of the DPD detector increases from 10μm × 10μm to 40μm × 40μm, the bandwidth merely decreases from 2.65 to 1.88GHz correspondently in Fig. 4(b). Com-

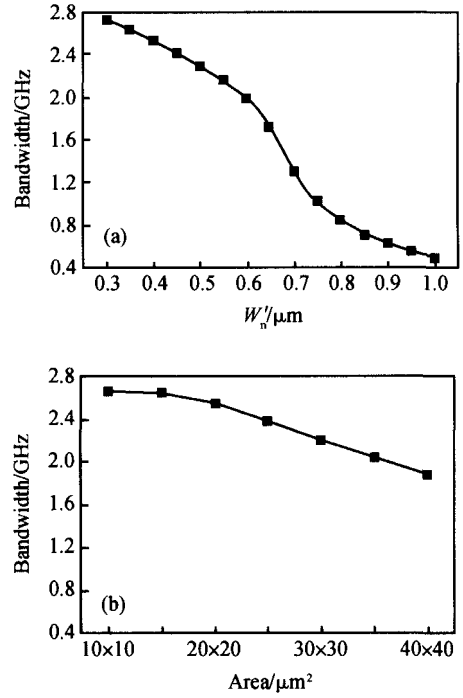

Fig. 4 Bandwidth of the monolithic photoreceiver based on different W_n'(a) and different area (b) of the DPD detector

pared with the two figures ,the area of the DPD detector is less limitative to the bandwidth because of the lower input impedance in the RGC input stage that can efficiently isolate the large DPD detector junction capacitance C_j. The junction capacitance C_j of 10μm ×10μm is about 25fF and C_j of 40μm × 40μm is about 400fF. Thus ,we can select the proper CMOS process ,which can make W_n' value smaller for wider bandwidth. Meanwhile ,we can properly use larger area 's DPD detector which can increase its performance when W_n' is small enough.

5　Optimization design and manufacture for photoreceiver

Available receiver bandwidth is optimized under the given input optical power and detector area. The model parameters are from CSMC-HJ 0. 6μm CMOS process ,a foundry in Wuxi , China. The simulation results of the RGC TIA are 3. 38 GHz bandwidth and 51. 1dB transimpedance gain. The simulation results of the photoreceiver with a 20μm ×20μm DPD are 1. 71 GHz and 49dB.

This photoreceiver has been realized in CSMC-HJ 0. 6μm CMOS process through MPW in China. Figure 5 shows the chip photograph of the photoreceiver.

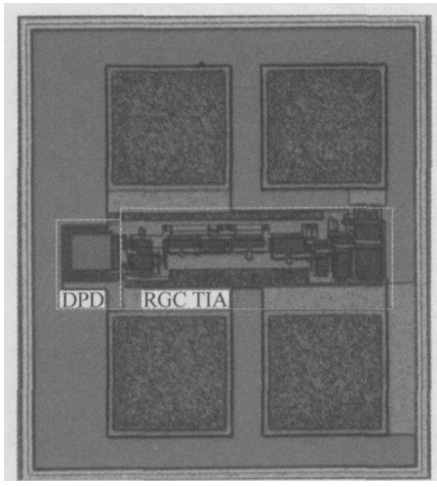

Fig. 5　Chip photograph of the photoreceiver

Figure 6 shows the optic frequency response of the photoreceiver , with input light of 0. 7mW on the photoreceiver. The experimental system consists of a high speed optical transmitter model , NF1780 , New Focus , and a network analyzer , HP8757C. From this figure the optic frequency response is about 1. 6GHz. The result is very near the design bandwidth.

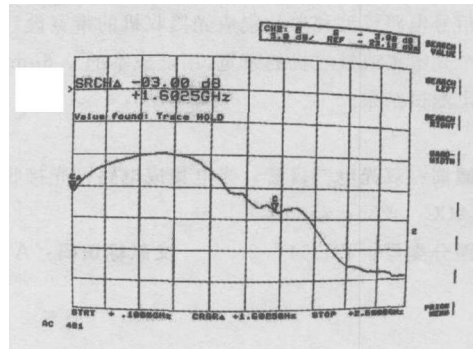

Fig. 6　Optic frequency response of the photoreceiver

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CMOS 单片光接收机的带宽设计 *

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摘要: 设计了一个由调节型级联跨阻抗放大器(TIA)和双光电二极管(DPD)构成的光电集成接收机. 给出了 DPD 小信号电路模型和单片集成光接收机的带宽设计方法,给出限制 DPD 和光接收机带宽的重要因素,分析和模拟了这个光电集成接收机的带宽,用低成本的 0. 6μm CMOS 工艺设计出 1. 71 GHz 带宽和 49dB 跨阻增益的接收机,并给出测试结果.

关键词: 双光电二极管; 光电集成电路; 光接收机
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