Compact Threshold Voltage Model for FinFETs *

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Abstract: A 2D analytical electrostatics analysis for the cross-section of a FinFET (or tri-gate MOSFET) is performed to calculate the threshold voltage. The analysis results in a modified gate capacitance with a coefficient H introduced to model the effect of tri-gates and its asymptotic behavior in 2D is that for double-gate MOSFET. The potential profile obtained analytically at the cross-section agrees well with numerical simulations. A compact threshold voltage model for FinFET, comprising quantum mechanical effects, is then proposed. It is concluded that both gate capacitance and threshold voltage will increase with a decreased height, or a decreased gate-oxide thickness of the top gate, which is a trend in FinFET design.

Key words: FinFET; 2D analytical electrostatic analysis; compact model; threshold voltage
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1 Introduction

DG-MOSFET and FinFET appear to be two of the most promising device structures[1~4] substituting current MOSFET beyond 65nm regime due to the electrostatic concern (i.e. off-state leakage current). Compact analytical modeling for these new structures is in order in anticipation of technology maturity. There have been active work on the compact modeling for DG-MOSFET, e.g. in Refs. [5~8]. However, analytical model for FinFETs is so far not seen yet, and it is critical to provide IC designers one because of FinFET's strong gate control capability and thus superior performance.

In this paper, a compact model for threshold voltage of FinFETs is presented based on 2D analytical electrostatic-analysis for the cross-section of a FinFET, comprising quantum mechanical effects. This compact model has the following two features: (1) since the derivation is fully physics-based, there are no fitting parameters and the analytical electrostatic potential profile agrees well with the numerical results; (2) the relation between device parameters and gate capacitance and threshold voltage are in explicit form, which makes it convenient to analyze the effect of the surrounding gate (both sides and on top) on device characteristics. It is concluded that gate capacitance and the threshold voltage increase with a decreasing height of channel slab and a decreasing gate-oxide thickness of the top gate.

2 Modeling and results

First of all, for the convenience of discussion, a diagram of the cross-section of a FinFET is plotted in Fig. 1. In our notation, a is the height of the silicon channel region, b is the width of the channel region, t_{ox1} is the double side-gate (both front and

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back) oxide thickness, t_{ox2} is the top-gate oxide thickness, and t_{ox3} is the buried oxide thickness.

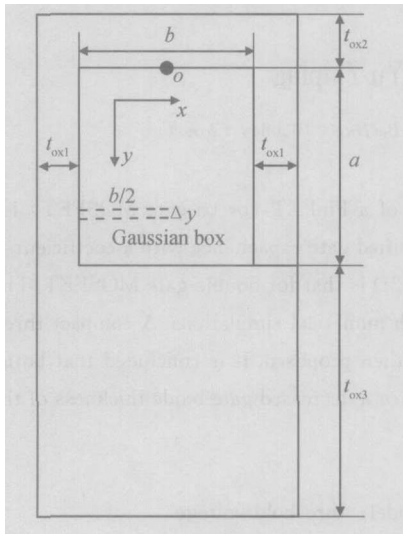

Fig. 1 Cross-section of FinFET. x is the direction along width while y is the direction along height. The origin of the 2D coordinate is set at o.

In Ref. [5], considering 1D electrostatics within the channel of a DG-MOSFET, the following expression of surface electron density n_e is obtained.

$$n_e = 2C_g(V_G' - \phi_c)/q \quad (1)$$

where $C_g = C_{ox}C_d/(C_{ox} + C_d)$ represents the gate capacitance per unit area with $C_{ox} = \varepsilon_{ox}/t_{ox}$ the oxide capacitance per unit area (ε_{ox} is oxide permittivity, t_{ox} gate-oxide thickness of a DG-MOSFET) and $C_d = 4\varepsilon_{Si}/d$ the depletion capacitance per unit area (ε_{Si} is silicon permittivity, d is width of a DG-MOSFET). $V_G' = V_G - (\phi_M - \chi + V_A - V_D)$ is the effective gate voltage with ϕ_M of the work function of the gate material, χ of the electron affinity of the semiconductor, $V_A = qn_A/2C_g$ (n_A is acceptor density per unit area) and $V_D = qn_D/2C_g$ (n_D is donor density per unit area). ϕ_c is the minimum point of the electric potential profile along the width direction, i.e. the electric potential at the center of the channel. Actually, the above equation reflects the relation of ϕ_c to n_e and V_G'. Therefore, for the FinFET case, if ϕ_c is defined as the minimum point of the electric potential profile at the cross-section, a similar equation as Eq. (1) may be found once the relation of ϕ_c to n_e and V_G' is derived according to 2D electrostatics.

From 2D numerical simulation, one knows that along the width direction (at any point of the height direction), the potential profile is parabolic with the minimum point at $x = 0$. Thus, ϕ_c for FinFETs can be defined as $\Phi(0, y_{min})$, which is obtained by

$$\left.\frac{d\Phi(0,y)}{dy}\right|_{y=y_{min}} = 0 \quad (2)$$

Consequently, the analytical form to the electric potential profile $\Phi(0, y)$ is essential to solve Eq. (2). The 2D Poisson's equation is presented for the first instance

$$\frac{d^2\Phi(x,y)}{dy^2} + \frac{d^2\Phi(x,y)}{dx^2} = \frac{q(N_e + N_A - N_D)}{\varepsilon_{Si}} \quad (3)$$

where N_e, N_A, and N_D are the electron concentration, the donor, and acceptor concentration, respectively. With the parabolic approximation of the electric potential along the x-direction, the electric potential may be expressed as

$$\Phi(x,y) = \sigma(y)x^2 + \tau(y) \quad (4)$$

The electric displacement continuity at the silicon/oxide interfaces is shown as

$$-\left.\frac{d\Phi(x,y)}{dx}\right|_{x=b/2} = -2\sigma(y) \times\left(-\frac{b}{2}\right) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \times \frac{V_G - (\phi_M - \chi) - \Phi(-b/2, y)}{t_{ox1}} \quad (5)$$

Therefore, the second derivative respect to x of $\Phi(x,y)$, i.e. $2\sigma(y)$, is obtained. Equation (3) at the 1D cut line of $x = 0$ is then rewritten as

$$\frac{d^2\Phi(0,y)}{dy^2} + \frac{8C_{ox1}}{b^2(C_{ox1} + C_d)}[V_G - (\phi_M - \chi) - \Phi(0,y)] = \frac{q(N_e + N_A - N_D)}{\varepsilon_{Si}} \quad (6)$$

Integrating both side by $\int_0^{b/2} dx$, one transforms Eq. (6) into Eq. (7),

$$\frac{d^2\Phi(0,y)}{dy^2} \times\frac{b\varepsilon_{Si}}{2} + C_g[V_G - (\phi_M - \chi) - \Phi(x,y)] = \frac{q(n_e + n_A - n_D)}{2} \quad (7)$$

Equation (7) is further solved analytically. The solution is as follows

$$\Phi(0,y) = A + B\frac{\sinh(y/D)}{\sinh(a/D)} + C\frac{\sinh[(a-y)/D]}{\sinh(a/D)} \quad (8)$$

where $A = V_G - (\phi_M - \chi - q(n_e + n_A - n_D)/2C_g$, $B = \phi_{0,a} - A$, $C = \phi_{0,0} - A$, $D = \sqrt{b\varepsilon_{Si}/2C_g}$ where $\phi_{0,a} = \phi(0, a)$ and $\phi_{0,0} = \phi(0,0)$ are two constants whose values need to be found. In Fig. 2, the analytical results of $\phi(-b/2, y)$ (this can be obtained straightforwardly from $\phi(0, y)$) and $\phi(0, y)$ of a FinFET are compared to numerical results (executed using DESSIS in ISE 8.0, a 2D self-consistent Poisson-Schrödinger solver[9]) at various V_G with given $\phi_{0,0}$ and $\phi_{0,a}$ (these two constants are provided by numerical simulation). The analytical profiles agree well with numerical ones and are not uniform along y-direction, which shows the difference between DG-MOSFETs and FinFETs. This proves the applicability of Eq. (8).

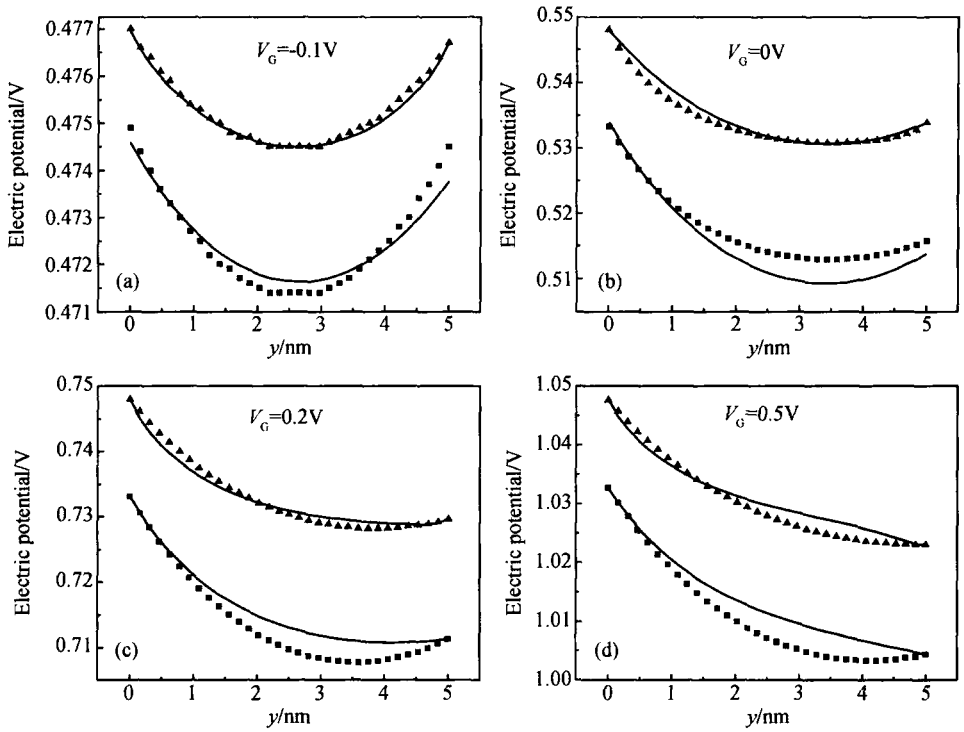

Fig. 2　$\phi(-b/2, y)$ and $\phi(0, y)$ profiles along height direction at various gate voltages　$a = b = 5$nm, $t_{ox1} = t_{ox2} = 1$nm and $t_{ox3} = 25$nm. Symbols stand for numerical simulation results (triangles for $\phi(-b/2, y)$ and squares for $\phi(0, y)$) while solid lines stand for analytical results.

Consider the boundary conditions $\phi(0, y)$ along the height direction: $\left.\frac{d\phi(0,y)}{dy}\right|_{y=0} = \frac{C_{ox2}}{\varepsilon_{Si}}\{\phi_{0,0} - [V_G - (\phi_M - \chi)]\}$ ($C_{ox2} = \varepsilon_{ox}/t_{ox2}$ is top-gate oxide capacitance per unit area) and $\left.\frac{d\phi(0,y)}{dy}\right|_{y=a} = \frac{C_{ox3}}{\varepsilon_{Si}}\{[V_B - (\phi_M - \chi)] - \phi_{0,a}\}$ ($C_{ox3} = \varepsilon_{ox}/t_{ox3}$ is the back-gate oxide capacitance per unit area and V_B is the back-gate voltage). Given these two equations, $\phi_{0,0}$ and $\phi_{0,a}$ are deduced,

$$\phi_{0,0} = (FG' + F')/(GG' - 1) \quad (9)$$

$$\phi_{0,a} = (F'G + F)/(GG' - 1) \quad (10)$$

where $F = E[V_G - (\phi_M - \chi)] + [\cosh(a/D) - 1]A$ with $E = C_{ox2}D\sinh(a/D)/\varepsilon_{Si}$, $F' = E'[V_B - (\phi_M - \chi)] + [\cosh(a/D) - 1]A$ with $E' = C_{ox3}D\sinh(a/D)/\varepsilon_{Si}$, $G = E + \cosh(a/D)$ and $G' = E' + \cosh(a/D)$. Thus, the analytical form of $\phi(0, y)$ is derived as a function of n_e and V'_G. Using Eq. (2) and Letting $E' \approx 0$ (holding true since the thickness of buried oxide is practically much larger than the channel width, i.e. $t_{ox3} \gg \varepsilon_{ox}D\sinh(a/D)/\varepsilon_{Si}$), the relation between ϕ_c and n_e and V'_{GS} is finally obtained,

$$n_e = 2C'_g(V'_{GS} - \phi_c)/q \quad (11)$$

This equation is very similar with Eq. (1) except for the substitution of C_g' for C_g and the corresponding replacement in V_{GS}' where $V_A = qn_A/2C_g'$ and $V_D = qn_D/2C_g'$. $C_g' = C_g/H$ with $H = 1 - \frac{E}{GG' - 1} \times [2e^{-a/2D}\sqrt{\cosh(a/D)} - e^{-a/D}]$, is denoted as tri-gate coefficient, which essentially reflects the effect of the top-gate. In Fig. 3, H is plotted versus a with different t_{ox2} and b. As it is shown in the figure, the tri-gate coefficient stays always lower than unity, implying larger gate capacitances of FinFETs than those of DG-MOSFETs. It may also be drawn that the larger the height is, the larger H is, meaning that the effect of the top gate is weaker since gate capacitance gets closer to the DG case. When $a \gg D$, H approaches to unity, leading Eq. (11) to Eq. (1) so that the asymptotic behavior to DG-MOSFETs is correct. H decreases with a decreasing t_{ox2} or an increasing b, meaning the effect of top gate is more severe with thinner top-gate oxide or wider width.

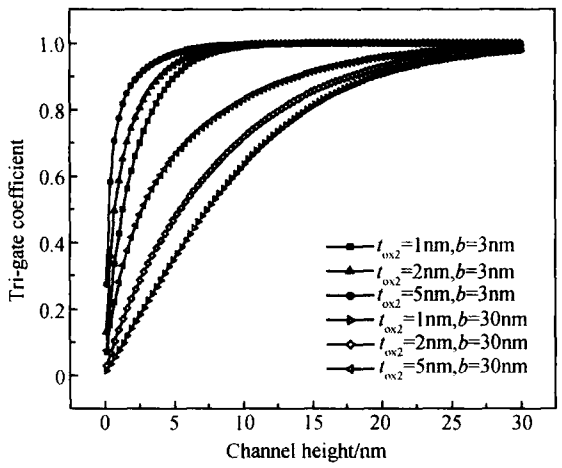

Fig. 3 Tri-gate coefficient H versus channel height a with different t_{ox2} and b $t_{ox1} = 1$nm and $t_{ox3} = 30$nm.

With the deduced Eq. (10), the threshold voltage model is finally derived as follows (the procedure of which is similar with that in Ref. [5] and therefore is not presented here),

$$V_T = \Phi_M - \chi + V_A - V_D + \frac{k_B T}{q} \lg\left(\frac{2C_g' k_B T}{q^2 N_c}\right) \tag{12}$$

where k_B is the Boltzmann constant, T is the temperature, and N_c is the effective density of states. This formula comprises quantum mechanical effects[5]. In Fig. 4, V_T is plotted against temperature for different t_{ox1}, t_{ox2}, a, and b. It is concluded that V_T decreases when any of these four device parameters increases. It should be noted that the temperature coefficient of V_T increases and the curve of $V_T - T$ becomes more linear with an increasing value of any of these four parameters. Although the parameters along height direction (t_{ox2} and a) affect V_T less severe than the parameters along width direction (t_{ox1} and b) do, they do have an influence on V_T and thus the device characteristics.

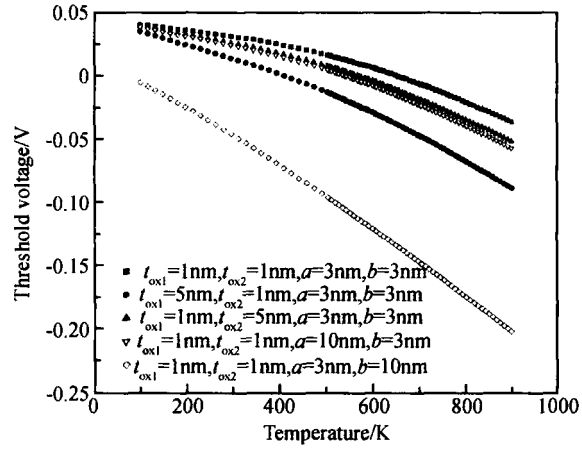

Fig. 4 Threshold voltage V_T versus temperature T with different t_{ox1}, t_{ox2}, a, and b $t_{ox3} = 30$nm.

3 Conclusion

In this paper, a compact threshold voltage model for FinFETs is presented with the relation to device parameters clearly clarified. It is concluded that both gate capacitance and threshold voltage will increase with decreasing of height or top-gate oxide thickness.

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FinFET 器件的集约阈电压模型 *

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摘要: 对 FinFET 器件(或称三栅 MOSFET 器件)的二维截面做了解析静电学分析以得出阈电压的计算公式. 结果显示,由于三栅结构在高度方向的限制作用,需要引入一个 H 系数来修正栅电容,随着高度不断变大,它渐近于双栅 MOSFET 器件的情况. 由该解析模型得出的电势分布与数值模拟结果吻合. 提出了一个包含量子效应的 FinFET 器件的集约阈电压模型,结果表明,当高度或者顶栅的氧化层厚度变小时,栅电容及阈电压都会上升,这与 FinFET 设计时发现的趋势是相符合的.

关键词: FinFET 器件; 二维解析静电学分析; 集约模型; 阈电压

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