Elevated Source/Drain Engineering by Novel Technology for Fully-Depleted SOI CMOS Devices and Circuits

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Abstract: 0.35μm thin-film fully-depleted SOI CMOS devices with elevated source/drain structure are fabricated by a novel technology. Key process technologies are demonstrated. The devices have quasi-ideal subthreshold properties; the subthreshold slope of nMOSFETs is 65mV/decade, while that of pMOSFETs is 69mV/decade. The saturation current of 1.2μm nMOSFETs is increased by 32% with elevated source/drain structure, and that of 1.2μm pMOSFETs is increased by 24%. The per-stage propagation delay of 101-stage fully-depleted SOI CMOS ring oscillator is 75ps with 3V supply voltage.

Key words: FDSOI; CMOS; elevated source/drain
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1 Introduction

As CMOS technology continues to scale down, fully-depleted SOI (FDSOI) technology assumes a prominent position as a potential solution to the problems associated with continued device scaling[1]. Some of the benefits of using FDSOI are reduction of junction capacitance, immunity for radiation, latch up-free for complementary metal-oxide-semiconductor (CMOS)[2], suppression of the short-channel effects[3], process simplicity[4], higher device packing density, and so on. FDSOI devices are also superior to thick-film, partially-depleted SOI (PDSOI) devices, because FDSOI MOSFETs have no body effect[5].

The FDSOI technology offers a potential solution to control short channel effects by reducing the silicon film thickness. However, aggressive silicon film thickness reduction increase the parasitic source/drain series resistance[6]. Furthermore, conventional process cannot be used on this ultra-thin silicon film due to incomplete silicide formation. The resulting high parasitic source/drain series resistance degrades the device performance and obscures the advantages of FDSOI[7]. Therefore, reducing the source/drain resistance has become an important issue for ultra-thin FDSOI MOS devices.

In order to suppress and avoid the risk of siliciding the whole silicon film, a new technology to form elevated source/drain structure is brought forward firstly. With this technology, the problem of high source/drain series resistance can be resolved and enough thickness of silicon was provided to form $TiSi_2$.

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2 Device fabrication

2.1 Fabrication flow

The SIMOX wafers used were fabricated by Shanghai Simgui Technology Co. Ltd. The SIMOX wafer had buried oxide layer with the thickness of 370nm and SOI film layer with the thickness of 190nm.

Until the gate formation ,the process technology is conventional CMOS technology. The process flow is described as below.

The SOI film thickness was thinned down to ~50nm by two-step oxidation and oxide strip. The isolation technology used is LOCOS. BF_2^+ was implanted with energy of 40keV and dose of $4\times10^{12}\,cm^{-2}$ as nMOSFETs V_T adjust implant ,and 40keV $6\times10^{11}\,cm^{-2}$ as pMOSFETs V_T adjust implant. After growing a 12nm gate oxide ,300nm polysilicon layer was deposited. P^+ with energy of 70keV and dose of $8\times10^{15}\,cm^{-2}$ was implanted into the polysilicon. The gate was patterned and etched to 0.35 ~1.2μm range. Then phosphorus with energy of 10keV and dose of $3\times10^{13}\,cm^{-2}$ was implanted in nMOSFETs. BF_2^+ with energy of 10keV and dose of $3\times10^{13}\,cm^{-2}$ was implanted in pMOSFETs. The purpose of the implantation is to form LDD structure.

2.2 Novel technology

The next process is to produce elevated source/ drain structure by a novel technology. Figure 1 shows an abbreviated process flow of thin-film FDSOI device with elevated source/ drain structure. After LDD implantation , 180nm thick TEOS oxide was deposited. The first spacer was formed by RIE process. Then BF_2^+ was implanted with energy of 40keV and dose of $2\times10^{15}\,cm^{-2}$ as the first p^+ implantation. As^+ was implanted with energy of 60keV and dose of $2\times10^{15}\,cm^{-2}$ as the first n^+ implantation. Second TEOS oxide with the thickness of 300nm was deposited after first

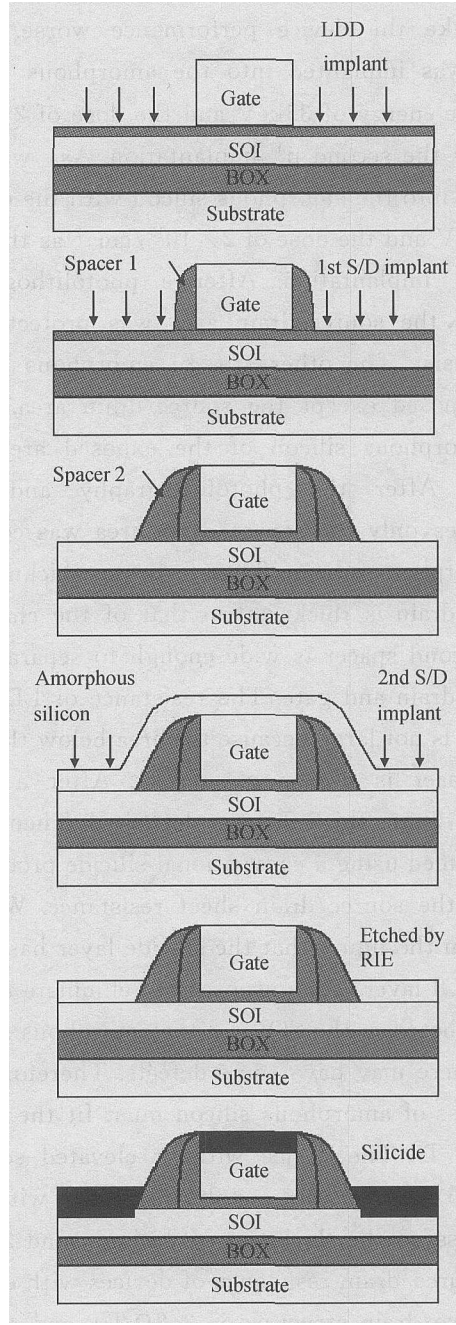

Fig. 1 Process flow of novel technology to form elevated sourced/ drain structure

source/ drain implantation. After the second spacer formation ,a layer of amorphous silicon with the thickness of 45nm was deposited by LPCVD. This layer of amorphous silicon is to form the elevated source/ drain structure. The reason of not using polysilicon is the deposition temperature of amorphous silicon is much lower than that of polysilicon. This reduces the dopant diffusion effect that

can make the device performance worse. Then BF_2^+ was implanted into the amorphous silicon with the energy of 35keV and the dose of 2×10^{15} cm^{-2} as the second p^+ implantation. As^+ was implanted into the amorphous silicon with the energy of 50keV and the dose of $2\times10^{15}/cm^{-2}$ as the second n^+ implantation. After a photolithography process, the source/drain area was protected by photoresist. The other area of amorphous silicon was exposed except the source/drain area. Then the amorphous silicon of the exposed area was etched. After the photolithography and RIE processes, only the source/drain area was covered by amorphous silicon. Therefore, the thickness of source/drain is thicker than that of the channel. The second spacer is wide enough to separate the source/drain and gate. The resistance of LDD extension is not large because the area below the second spacer is n^+ or p^+ region. After a RTA process, 30nm thick Ti was deposited. Then $TiSi_2$ was formed using a conventional silicide process to reduce the source/drain sheet resistance. We can see from the figure that the silicide layer has eaten some SOI layer. The purpose is to eliminate the interface between the SOI and the amorphous silicon since there may have some defects. Therefore, the thickness of amorphous silicon must fit the thickness of Ti. The device without elevated source/drain structure cannot supply the silicon with that thickness, so the thickness of Ti is around 20nm. The source/drain resistance of devices with elevated source/drain structure is 3.8Ω/□, and that of devices without elevated source/drain structure and 20nm thick Ti to form silicide is 5.8Ω/□.

3 Discussion

Figures 2 and 3 show the subthreshold characteristics of nMOSFETs and pMOSFETs, respectively. The gate length is 0.35μm, the gate oxide thickness is 12nm. The channel dopant of nMOSFETs(pMOSFETs) is BF_2^+ with concentration of $4\times10^{12}cm^{-2}$ ($6\times10^{11}cm^{-2}$). It is obviously that the both nMOSFETs and pMOSFETs have quasi-ideal subthreshold properties; the subthreshold slope of nMOSFETs is 65mV/decade, while that of pMOSFETs is 69mV/decade. When the silicon thin-film enters into the fully-depleted region, its subthreshold slope is much better with value close to the ideal case-(kT/q)(ln10) mV/decade due to the buried oxide isolation between the channel and the grounded substrate. Furthermore, we can see from the Figs. 2 and 3 that the DIBL effect is very little in either nMOSFETs or pMOSFETs.

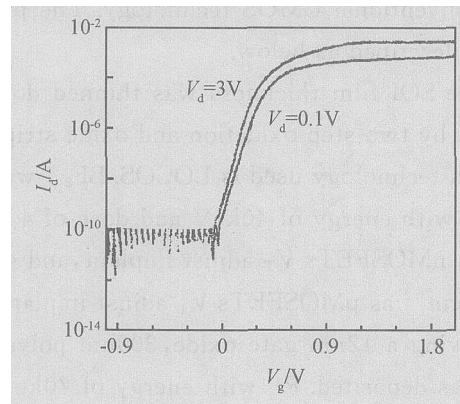

Fig. 2 Subthreshold characteristics of nMOSFETs

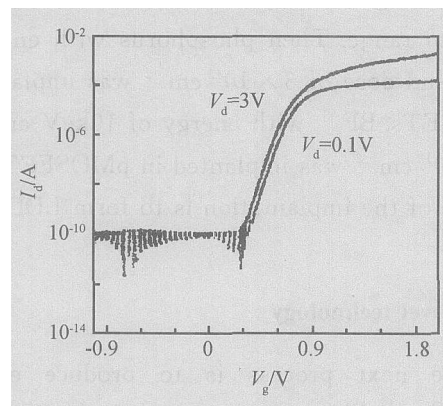

Fig. 3 Subthreshold characteristics of pMOSFETs

The comparison of saturation currents between elevated source/drain devices and normal devices is shown in Figs. 4～7. In this case, we use 1.2μm gate length devices because we have no 0.35μm devices experiments results before. The gate oxide thickness is 12nm, too. The channel dopant and concentration of nMOSFETs and pMOSFETs are same with that of the 0.35μm gate length devices. The processes of the two kinds of

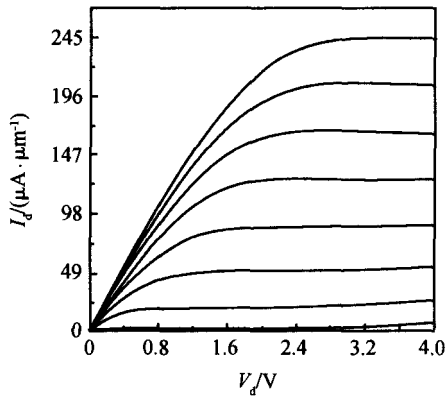

Fig. 4　Output characteristics of 1. 2μm nMOSFETs with elevated source/ drain structure

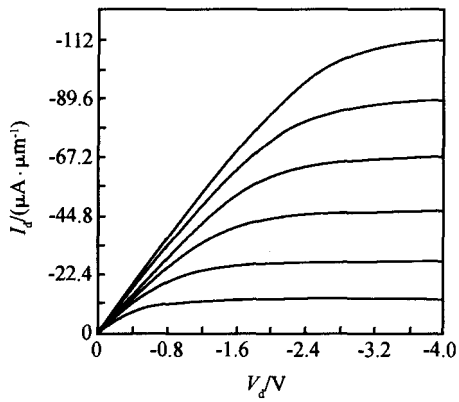

Fig. 5　Output characteristics of 1. 2μm pMOSFETs with elevated source/ drain structure

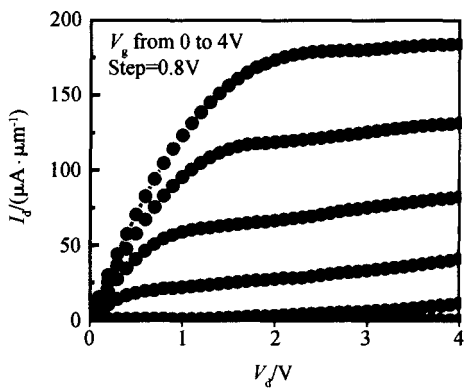

Fig. 6　Output characteristics of 1. 2μm nMOSFETs without elevated source/ drain structure

devices are almost same except the processes to form elevated source/ drain structure. The saturation current of nMOSFETs was increased by 32 % with elevated source/ drain structure ,while the saturation current of pMOSFETs was increased by 24 %. Using the elevated source/ drain structure by novel process technology , the drain current has been improved substantially.

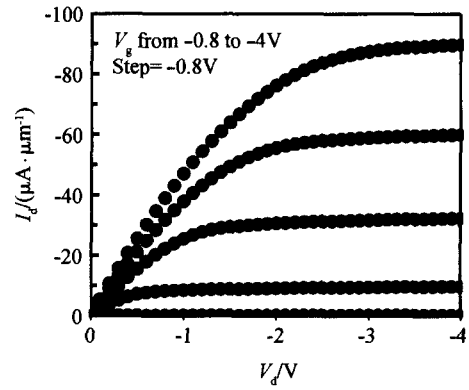

Fig. 7　Output characteristics of 1. 2μm pMOSFETs without elevated source/ drain structure

Figure 8 shows the propagation delay of 101-stage thin-film FDSOI CMOS ring oscillator. The per-stage propagation delay of 101-stage SOI CMOS ring oscillator is 75ps with 3V supply voltage. The speed of FDSOI CMOS circuits is faster than that of partially-depleted SOI CMOS circuits and bulk circuits due to high mobility ,high transconductance ,and low parasitical capacitance.

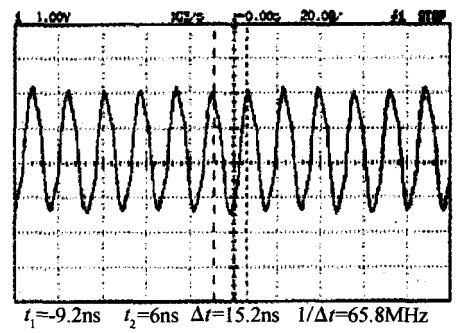

Fig. 8　Propagation delay of 101-stage FDSOI CMOS ring oscillator

4　Conclusion

We have successfully fabricated the thin-film FDSOI devices with elevated source/ drain structure. The novel technology to form elevated source/ drain structure is brought forward first. Both nMOSFETs and pMOSFETs have quasi-ideal

subthreshold properties. The DIBL effect of them is little. The saturation current is improved substantially with the elevated source/drain structure. The per-stage propagation delay of 101-stage FD-SOI CMOS ring oscillator is 75ps with 3V supply voltage.

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采用新的抬高源漏工艺技术制作的全耗尽 SOI CMOS 器件和电路

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摘要: 采用新的工艺技术,成功研制了具有抬高源漏结构的薄膜全耗尽 SOI CMOS 器件. 详细阐述了其中的关键工艺技术. 器件具有接近理想的亚阈值特性, nMOSFETs 和 pMOSFETs 的亚阈值斜率分别为 65 和 69mV/dec. 采用抬高源漏结构的 1.2μm nMOSFETs 的饱和电流提高了 32%, pMOSFETs 的饱和电流提高了 24%. 在 3V 工作电压下 101 级环形振荡器电路的单级门延迟为 75ps.

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