Off-State Breakdown Characteristics of Body-Tied Partial-Depleted SOI nMOS Devices

Wu Junfeng, Zhong Xinghua, Li Duoli, Kang Xiaohui, Shao Hongxu, Yang Jianjun, Hai Chaohe, and Han Zhengsheng

(*Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: Partial-depleted SOI(silicon on insulator) nMOS devices are fabricated with and without silicide technology, respectively. Off-state breakdown characteristics of these devices are presented with and without body contact, respectively. By means of two-dimension(2D) device simulation and measuring junction breakdown of the drain and the body, the difference and limitation of the breakdown characteristics of devices with two technologies are analyzed and explained in details. Based on this, a method is proposed to improve off-state breakdown characteristics of PDSOI nMOS devices.

Key words: partial-depleted SOI; body-tied; breakdown; silicide; H-gate
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1 Introduction

SOI(silicon on insulator) technology has been credited with the most prospective technology that may replace the bulk CMOS technology. And due to good scalability and strong resistance to harsh environments SOI devices are more suitable for future integrated circuits. However, because of the existence of floating body effect in SOI nMOSFET, which leads to undesirable effects in many applications, people have to adopt a variety of methods to eliminate it. The most direct way is to add a contact to the body, thus eliciting redundant holes from floating area. Such structure is similar to bulk-silicon devices because the body potential is set as a fixed value in SOI devices like in bulk-silicon devices; however, characteristics of body-tied devices on SOI are not exactly the same as those of devices on bulk silicon in which there is extra buried oxide layer between two silicon layers. Therefore, it is still necessary to make research on characteristics of body-tied SOI devices. Like bulk silicon devices, through off-state breakdown characteristic, which is among key parameters of devices and circuits, the leakage current under the static condition can be obtained. There are many proposals to improve breakdown characteristic, however, these proposals generally need complex design and processing conditions[1~5]. By now, due to good compatibility with CMOS bulk-silicon technology and easier body-tied design, T-gate (H-gate) structure is still very popular[6].

In this paper, we make an investigation on off-state breakdown characteristics of H-gate PDSOI nMOS devices fabricated with and without silicide technology under the condition $V_{gs} = 0$V. We discuss the mechanism of such breakdown characteristics and propose a way to improve the breakdown characteristics.

Wu Junfeng male, was born in 1980. He is now engaged in research on SOI devices, technologies, and circuits. Email: jfwu@mails.gscas.ac.cn

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2 nMOSFET fabrication

To avoid the lateral leakage current[7] (which can influence the breakdown characteristics of devices) possibly caused by processing conditions, we design the H-gate nMOSFET with $w/l = 50/2$. Devices are isolated by LOCOS(local oxidation of silicon). The SOI material is 400nm thick in Si layer, 370nm thick in BOX (buried oxide) and p-type substrate. We divide SOI nMOSFET into two groups. One group is fabricated with silicide technology and the other is fabricated without silicide technology. Gate length is 2μm and gate oxide is 20nm thick. The dose of back channel implantation of boron is $2 \times 10^{13}\ cm^{-2}$, and the dose of front channel implantation of BF_2 is $1 \times 10^{11}\ cm^{-2}$. In order to activate the impurities implanted in the silicon film, a rapid thermal processing (RTP) at 1000 ℃is performed. In two groups, the same dose and energy of arsenic is implanted to source and drain. Especially, in the second group, to form silicide, we add a LDD (light doping drain) implantation of phosphorus of the dose $5 \times 10^{13}\ cm^{-2}$ after the gate is formed; 300nm spacer is formed before the implantation of the source and the drain. Figure 1 shows the schematic cross sections of two-group device structures and layout of H-gate devices.

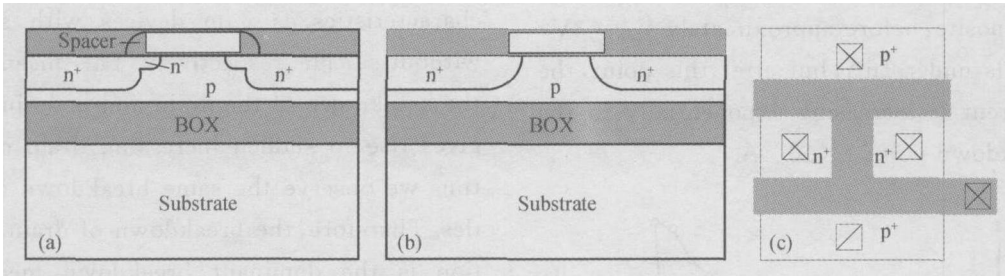

Fig. 1 (a) Structure of nMOS device with silicide; (b) Structure of nMOS device without silicide; (c) Layout of H-gate

3 Results and discussion

3.1 Results

After the formation of devices, we measure the off-state breakdown curves with HP4145A semiconductor parameter analyzer. In our test, the source, the substrate, and the gate are always grounded. And we define the current 1×10^{-5} A as the breakdown point. Figure 2 shows the breakdown characteristics of devices under the condition that body contact is floating and grounded, respectively. From the figure, we can clearly see the soft breakdown characteristics and low breakdown voltage for devices with floating body compared to devices with body contact. This is because of the existence of a parasitic bipolar transistor in PDSOI nMOS devices with floating body and it is this parasitic bipolar transistor that causes such breakdown characteristics[8]. For body-tied devices, the body contact can elicit redundant holes from the body area, thus suppressing the "kink effect", decreasing the drain current and impact-ionization rate; moreover, the body contact inhibits parasitic bipolar from working due to it is grounded. Thus the breakdown characteristics are better than those of devices with floating body.

To more clearly compare off-state breakdown characteristics of devices with body contact, we convert the type of y-axis in Fig. 2 from linear coordinate to denary logarithmic coordinate and only show the breakdown characteristics of nMOS devices with body contact in Fig. 3. In Fig. 3, there is a conspicuous dissimilarity between the curves of devices with silicide and without silicide. For devices without silicide, there is almost steep increasing at approximately $V_{ds} = 9$V, and before $V_{ds} = 9$V,

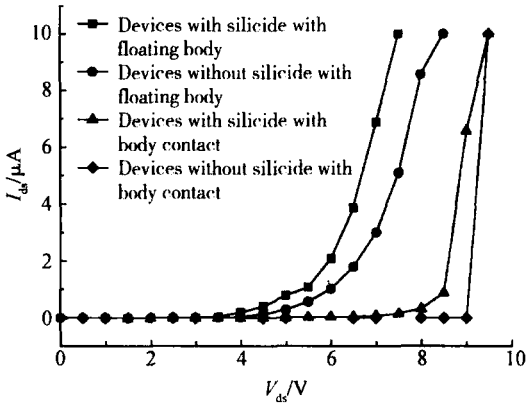

Fig. 2 Breakdown characteristics of nMOS devices

the current is small than 1nA and can be considered as no leakage current before the breakdown of devices. For devices with silicide, the situation is almost the opposite: before approximately $V_{ds} = 3V$, the current is under 1nA, but after this point, the leakage current is increasing exponentially to the preset breakdown point 1×10^{-5}A.

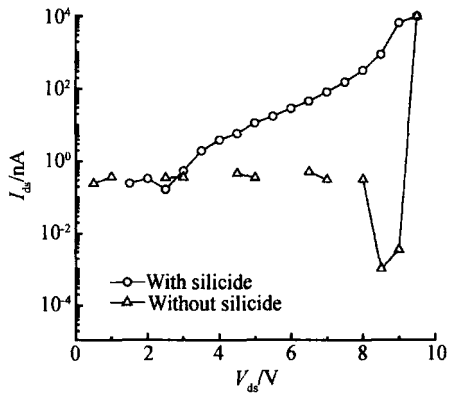

Fig. 3 Breakdown characteristics of devices when body contact is grounded

3.2 Discussion

To find out the cause of such dissimilarity, we measured breakdown voltage of pn junction of the body and the drain (the gate, the source, the substrate is floating) in the samples from those devices with and without silicide. Figure 4 shows the breakdown characteristics of junction of the body and the drain.

From Fig. 4, we notice that the breakdown characteristic of the junction is almost the same as

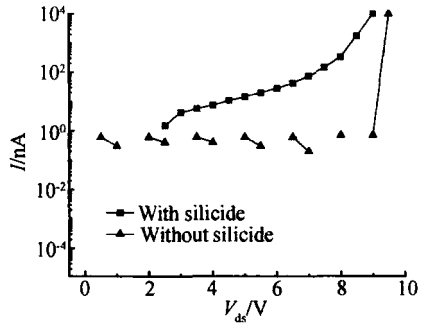

Fig. 4 Breakdown curves of the body and drain junction

that of devices. In addition, in the device measurement, we find that body-tied devices with gate length of 5, 10μm (the processing condition is the same as 2μm devices) have the same breakdown characteristics as 2μm devices with silicide and without silicide, respectively. This means that it is the breakdown of the drain and body junction that gives rise to sudden increasing drain current and thus we observe the same breakdown characteristics. Therefore, the breakdown of drain-body junction is the dominant breakdown mechanism of these devices. To clarify this phenomenon, we can first compare nMOS devices on bulk silicon with those on SOI when the doping concentration of the drain and the substrate (for SOI devices, the body) are the same. Generally, the off-state breakdown mechanism of nMOS devices on bulk silicon is gate-modulating breakdown[9]. However, for body tied SOI nMOS devices, due to existence of BOX and body-contact, the length of the body electrode to the drain and body junction is less than the length of substrate electrode to the drain and substrate junction in bulk-silicon nMOS devices, which have no body-contact. Correspondingly the breakdown voltage of the pn junction of body and drain in SOI devices is less than that of substrate and drain in bulk-silicon devices. Figure 5 shows the schematic of the pn junction of body and drain and the drain part of body tied devices. Because we need implant certain concentration of boron in back channel in order to suppress back channel inversion, when the doping concentration reaches the ex-

tent that the breakdown voltage of the pn junction of drain and body is smaller than one caused by gate-modulating breakdown mechanism, it is the breakdown of the pn junction of the drain and the body that chiefly determines the breakdown of body-tied SOI nMOS devices.

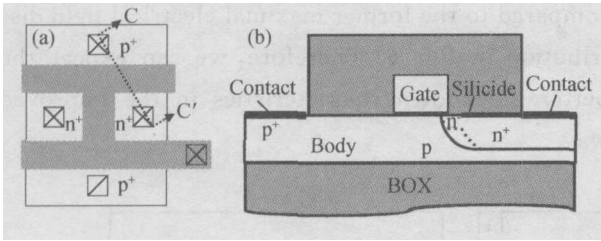

Fig. 5　(a) pn junction of body and drain; (b) Drain part of the devices with and without silicide (broken line represents LDD in devices with silicide) along line CC′ showed in (a)

Now we discuss the dissimilarity of breakdown characteristics of nMOS devices with and without silicide. To more clearly explain this dissimilarity, we conduct a two-dimension (2D) process and device simulation. All the simulation conditions are the same as processing conditions and test conditions of real nMOS devices. But because the real body-tied device is three-dimension (3D) structure, 2D simulation is still different from the real situation and here we only make qualitative analysis. Figure 6 shows at V_{ds} = 6V, the distribution of maximal electrical field of devices from the source to the channel to the drain in Si layer with silicide and without silicide, respectively. From Fig. 6, we can see that the maximal electrical field of devices with silicide in the drain is larger than those without silicide. Especially in the part of connection of the channel and the drain, for devices with silicide, the maximal electrical field reaches about 2.2×10^6 V/cm, while that for devices without silicide is only about 1.1×10^6 V/cm. Larger electrical field causes devices with silicide to be easier to reach breakdown point, which leads to leakage current. But LDD structure in devices with silicide makes the maximal electrical field decrease dramatically to a "valley" as shown in Fig. 6(b), so the devices in lower voltage will not breakdown entirely and only local breakdown will occur. Thus as V_{ds} increases, the breakdown area extends and the increasing leakage current can be observed. In comparison, for devices without silicide, the junction cannot reach the break point until at V_{ds} = 9.5V as shown in Fig. 3. The reason that devices with silicide have larger maximal electrical field is the exsitance of silicide. Silicide can dramatically reduce the resistance of drain part and voltage drop, while for devices without silicide, there will be more voltage dropping on the resistance of the drain and correspondingly the voltage drop on the pn junction of the drain and the body is less when the same voltage is applied to the drain and the body for devices with and without silicide, respectively.

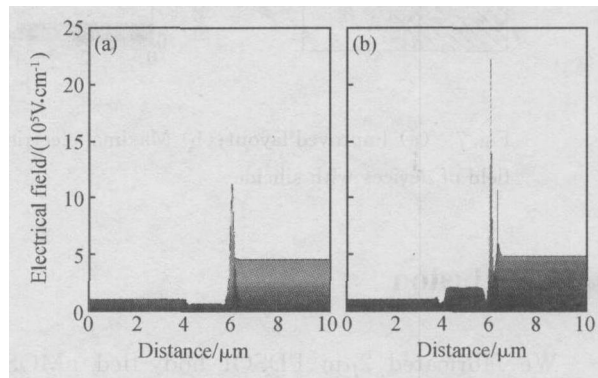

Fig. 6　Maximal electrical field distribution of devices without silicide (a) and with silicide (b)

3.3　A way to improve off-state breakdown voltage

Because the breakdown mechanism of body tied nMOS devices is mainly determined by pn junction of the drain and the body, we propose a method to improve the breakdown characteristic. Here we can simply see the pn junction of the drain and the body as unilateral abrupt junction due to the very high concentration of arsenic in the drain and comparably very low concentration of boron in the body. Thus for the unilateral abrupt junction, we can make use of the experimental formula[10],

$$V_{BS} = 60(E_g/1.1)^{3/2}(N_B/10^6)^{-3/4}$$

where E_g refers to the width of forbidden band, N_B refers to the impurity concentration of low-doping side.

According to this formula, lowering the doping concentration in the body contributes to improving breakdown voltage of pn junction of the drain and the body. In order not to influence the threshold voltage, we may only change the doping concentration of the back channel, and in order to guarantee the high threshold voltage of back gate and the good body contact, we adopt the way as shown in Fig. 7. We only implant half layout (the shade part) in the back channel implantation, that is, there is no back channel implantation in the drain part. To demonstrate the effect of this method, we simulated the distribution of maximal electrical field shown in Fig. 7. From the distribution of maximal electrical field, we can see that the obvious decreasing of maximal electrical field in the drain as compared to the former maximal electrical field distribution in Fig. 6. Therefore, we can expect the better breakdown characteristics in the improved way.

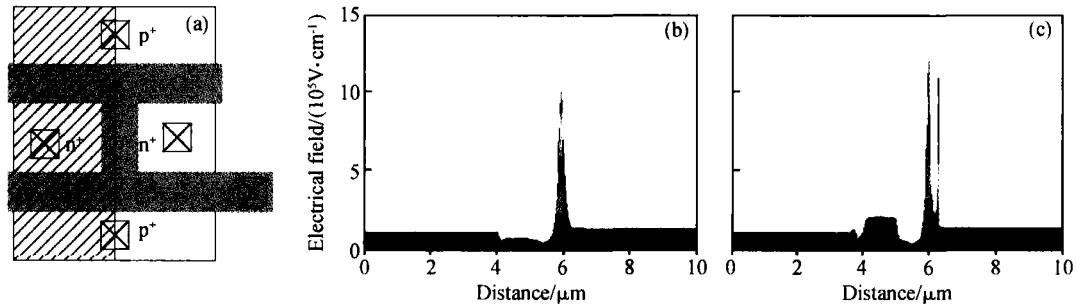

Fig. 7 (a) Improved layout; (b) Maximal electrical field of devices without silicide; (c) Maximal electrical field of devices with silicide

4 Conclusion

We fabricated 2μm PDSOI body-tied nMOS devices with silicide and without silicide, and measured the off-state breakdown characteristic of body-tied nMOS devices. By testing the breakdown characteristics of pn junction of the drain and the body, we analyze the breakdown mechanism of the body-tied PDSOI nMOS devices. In addition, we employ 2D process and device simulation to explain the dissimilarity of breakdown characteristics of devices of different technologies. In the end, by analyzing the breakdown formula of pn junction, we propose a way to improve the off-state breakdown characteristic of body-tied nMOS devices.

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部分耗尽 SOI 体接触 nMOS 器件的关态击穿特性

吴峻峰　钟兴华　李多力　康晓辉　邵红旭　杨建军　海潮和　韩郑生

(中国科学院微电子研究所, 北京　100029)

摘要: 分别采用具有硅化物和不具有硅化物的 SOI 工艺制成了部分耗尽 SOI 体接触 nMOS 晶体管. 在体接触浮空和接地的条件下测量了器件的关态击穿特性. 通过使用二维工艺器件模拟 ,并测量漏体结的击穿特性 ,详细讨论和分析了所制成器件击穿特性的差异和击穿机制. 在此基础上 ,提出了一个提高 PD-SOI 体接触 nMOS 击穿特性的方法.

关键词: 部分耗尽 SOI; 体接触; 击穿; 硅化物; H-gate

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吴峻峰　男 ,1980 年出生 ,目前从事 SOI 工艺、器件和电路方面的研究. Email :jfwu @mails. gscas. ac. cn

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