Electrical Properties of Ultra Thin Nitride/Oxynitride Stack Dielectrics pMOS Capacitor with Refractory Metal Gate

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Abstract: Electrical properties of high quality ultra thin nitride/oxynitride (N/O) stack dielectrics pMOS capacitor with refractory metal gate electrode are investigated, and ultra thin (< 2 nm) N/O stack gate dielectrics with significant low leakage current and high resistance to boron penetration are fabricated. Experiment results show that the stack gate dielectric of nitride/oxynitride combined with improved sputtered tungsten/titanium nitride (W/TiN) gate electrode is one of the candidates for deep sub-micron metal gate CMOS devices.

Key words: equivalent oxide thickness; nitride/oxynitride gate dielectric stack; high *k*; boron-penetration; metal gate

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1 Introduction

The continuous down scaling of thermal gate oxide has encountered a series of difficulties such as the excessive direct tunneling current, the strong tendency for boron penetration, poly gate depletion effect, and quantum mechanical effect[1~4]. To get over these challenges mentioned above, adopting oxynitride and high *k* material as gate dielectric have been reported by many authors. High quality Si_3N_4 gate dielectric has also been demonstrated by jet vapor deposition (JVD)[5].

While to improve the poor interface properties, nitride/oxynitride stack dielectrics are used to replace the single nitride dielectric to take the advantages of both the nitride film and thermal oxide film. It is well known that the thermal oxide can preserve the excellent oxide/Si interface characteristics, while the nitride film exhibits about twice of the dielectric constant of oxide, which effectively reduces the equivalent oxide thickness (EOT), that is increasing the physical thickness, so that the tunneling leakage current is reduced greatly and boron penetration is suppressed strongly.

Optimized sputtered W/TiN stack, as a refractory metal gate electrode, exhibits high thermal stability and high process compatibility. It has also thoroughly eliminated poly depletion and boron penetration and greatly decreased the gate resistance[6]. W/TiN, a midgap material, can be used as a gate material to fabricate both nMOS and pMOS simultaneously[7]. In this paper, characteristic of N/O stack gate dielectric with W/TiN gate electrode are analyzed with pMOS capacitors. Experiments show that this gate stack structure has gained excellent electrical properties.

2 Experiment

A local oxidation of silicon (LOCOS) isolated pMOS capacitor structure of W/TiN/Si_3N_4/oxynitride/n-sub was fabricated as shown schematically in Fig. 1. The bottom oxynitride film (0.7 ~ 0.8nm) was formed by oxidation of N^+ implanted

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silicon substrate at 670 ℃ in N_2. Ultra thin Si_3N_4 films (1.2～1.6nm) were deposited using LPCVD deposition by SiH_2Cl_2 and NH_3 at the ratio of

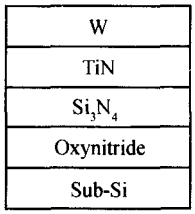

Fig. 1 Schematic structure of pMOS capacitor with N/O stack gate dielectric and refractory metal gate

SiH_2Cl_2/NH_3 = 6/1 at 715 ℃, chamber pressure 36.664Pa. After thermal annealing, 35nm TiN film was reactively sputtered using Ar and N_2 gas mixture followed by metal W deposition, then W/TiN electrode patterning and RIE. Finally, W/TiN capacitor samples were annealed in H_2 and N_2 gas mixture for 25min. In the poly gate capacitor case, 200nm poly was deposited by LPCVD followed by BF_2 implantation with doses of 1.5×10^{15} and $2\times10^{15}cm^{-2}$ and RTA with different activation time. EOT is extracted by fitting the measured high frequency capacitance-voltage (C-V) data at accumulation to C-V simulation including poly depletion effect and quantum mechanical effect[8].

3 Results and discussion

3.1 Gate leakage currents

The gate leakage currents versus the gate voltage of both p^+-gate/Si_3N_4/SiO_2/n-sub pMOS capacitors and W/TiN/Si_3N_4/SiO_2/n-sub pMOS capacitors with various EOT of stack N/O under the electron-accumulation conditions are shown in Fig. 2, and compared with that of pure oxide. Here the gate voltage refers to the voltage which applies to the gate dielectric ($V_{ox} = V_g - V_{fb}$) and N was implanted at a energy of 15keV and a dose of $3\times10^{14}cm^{-2}$. As shown in Fig. 2, when the EOT of the capacitors is reduced to the region where DT (direct tunneling) dominates, the N/O stack gate dielectric of 1.9nm with poly gate shows lower leakage current than thermal oxide with EOT of 2.0nm by several orders of magnitude while the N/O stack films of 1.7nm with W/TiN gate shows more than one order magnitude lower leakage current at lower field. The reasons why oxynitride grown on N implanted silicon for N/O stack gate dielectric is with significantly reduced leakage current are as below: one is that the oxidation retardation effect reduces the rate of oxidation greatly, which makes the oxynitride more density, uniformity as well as finer interface between silicon and oxide[9]; another is that LPCVD Si_3N_4 with higher dielectric constant, which increases the physical oxide thickness, can also contribute to the lower gate leakage currents. The leakage current of W/TiN gate capacitor with EOT 1.7nm is much lower than that of pure oxide with EOT 2.0nm sample at lower field. The cause of higher leakage current of the metal gate capacitor is that the EOT is 0.2nm thinner than that of the poly gate capacitors.

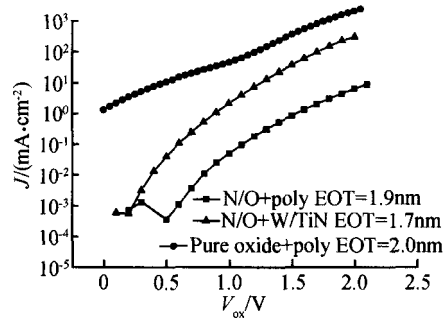

Fig. 2 J-V characteristics of different dielectric films and different gate materials $V_{ox} = V_g - V_{fb}$.

3.2 C-V characteristics

The C-V characteristics of pMOS capacitors with different gate electrode materials are shown in Figs. 3 and 4. A C-V simulator was used to fit the high frequency C-V data of the fabricated poly-Si gate capacitors and W/TiN gate capacitor respectively to extract the EOT of the ultra thin dielectrics. From Figs. 3 and 4, we can find that the extracted EOT of the poly capacitor is 1.9nm and that of the metal gate is 1.7nm. The C-V curve

mismatch of the simulator and the samples fabricated by us at lower gate voltages is mainly caused by the difference of the interface charges between the simulator and those of the samples. It should be noted that although the process of fabricating the N/O stack dielectric for both poly capacitor and W/TiN gate capacitor is the same except gate electrode material, the capacitance of the W/TiN gate is much larger than that of poly gate as shown in Fig. 5. The reason is that the W/TiN gate capacitor has eliminated the poly-Si depletion effect so that further reduces the EOT of the N/O stack gate dielectrics.

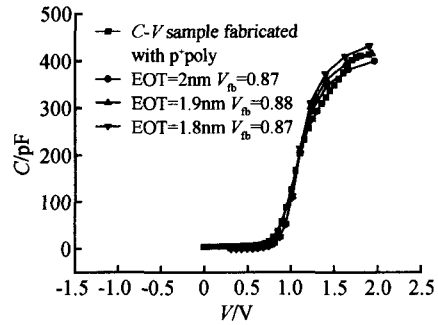

Fig. 3　*C-V* fit curves for p^+ poly gate electrode capacitor

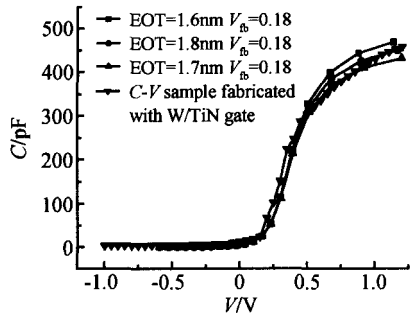

Fig. 4　*C-V* fit curves for W/TiN stack gate electrode capacitor

The hysteresis of the *C-V* characteristics with the N/O stack gate can be found from the amount of flatband shift between two different retrace sweep directions in high frequency *C-V* curves. The hysteresis characteristic, which reflects the number of interface states, is due to electron/hole trapping at the inversion mode and ejection at the accumulation mode[10]. As the film thickness is reduced to less than ~2.0nm, the amount of flatband voltage shift has reached to few micro voltage range, as shown in Fig. 5. So it can be seen that the hysteresis of *C-V* characteristics is very small (few mV) for ultra thin N/O stack layers and good interface characteristic is obtained.

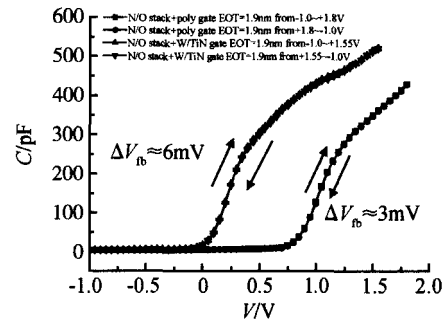

Fig. 5　Hysteresis of *C-V* characteristics of the N/O stack film with poly gate and metal gate

3.3 Suppression of B penetration

The samples of Si_3N_4/oxynitride stack gate dielectric show less boron penetration than that of pure oxide film due to the obstruction of the Si_3N_4 layer and the N located in the oxynitride layer as shown in Figs. 6, 7 and Table 1. It should be noted that one of the functions of introducing N into the oxide films can be regarded as knitting up the broken chemical bonds such as dangling bonds (O3 ≡ Si ·) and oxygen vacancy bonds (≡Si · · Si ≡) to form relatively complete Si—N bond structure. Another benefit is that strong Si—N bonds instead of

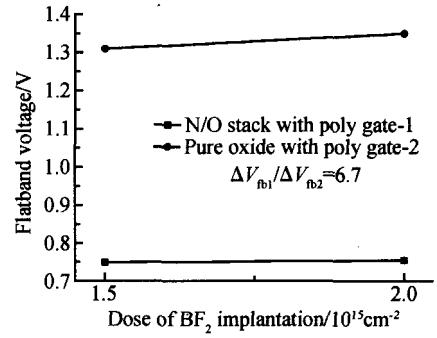

Fig. 6　Effect of implantation to flatband voltage for p^+ poly gate MOS capacitor with different gate dielectric

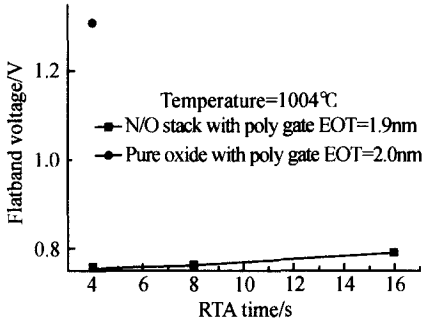

Fig. 7 Effect of RTA activation time on flatband voltage for p^+ poly gate MOS capacitor with N/O stack dielectric

weak bonds such as Si—OH, Si—H, and Si—O in interface of Si/SiO_2 improve the characteristics of the interface[11]. In addition, there is thicker physical thickness of Si_3N_4 film in N/O stack. In our experiment from Table 1, it can be seen that the metal gate capacitor (less than 0.15V) is with the slightest flatband voltage and the flatband voltage of the N/O stack dielectric with poly-Si gate is lower than that of thermal gate oxide. It should be indicated that different BF_2 implant dose in the p^+ poly or different RTA activation time also has effect on the flatband as shown in Figs. 6 and 7. As shown in Fig. 6, the poly-Si capacitor with the N/O stack dielectric has much lower shift of flatband voltage than that of pure oxide when the dose of BF_2 implantation changes from 1.5×10^{15} to $2\times10^{15}\,cm^{-2}$. From Fig. 7, it can be seen that the different activation time has little effect on the flatband of N/O stack dielectric capacitor. These results show that poly-Si capacitor with the N/O stack dielectric can strongly suppress the boron penetration. In addition, boron penetration induced low field leakage current is also suppressed considerably by the fabrication of N/O stack with N implantation prior to gate oxidation.

Table 1 Different capacitor and flatband voltage

Capacitor	Dose of BF_2 implantation/ $10^{15}cm^{-2}$	RTA time/ s, temperature/ ℃	Flatband voltage/ V
N/O stack with poly gate (EOT = 1.9nm)	1.5	4, 1005	0.72
N/O stack with W/ TiN gate (EOT = 1.7nm)	—	—	0.105
Pure oxide with poly gate (EOT = 2.0nm)	1.5	4, 1005	1.31

The larger capacitance as shown in Fig. 5 and lower flatband voltage as shown in Table 1 show that the gate depletion effects and the boron penetration phenomenon are completely eliminated in the metal gate pMOS capacitor. The reason is that there are no introduction of B ions in the metal gate material which is responsible for inducing poly-Si depletion and boron penetration.

4 Conclusion

The N/O stack gate dielectric is compared with other films and W/ TiN gate electrode capacitor with N/O stack dielectric shows much lower leakage current, complete elimination of both boron penetration and poly-Si gate depletion, comparing with pure oxide. These results demonstrate that ultra thin LPCVD Si_3N_4 with oxynitride grown on N implanted Si substrate as base layer can be used as gate dielectrics and sputtering W/ TiN can be used as gate electrode material. So these technologies could be one of the candidates for next generation metal gate CMOS FET.

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超薄氮氧叠层栅介质的金属栅 pMOS 电容的电学特性

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摘要：研究了高质量超薄氮化硅/氮氧化硅(N/O)叠层栅介质的金属栅 pMOS 电容的电学特性，制备了栅介质等效厚度小于 2nm 的 N/O 复合叠层栅介质，该栅介质具有很强的抗硼穿通能力和低的漏电流. 实验表明这种 N/O 复合栅介质与优化溅射 W/TiN 金属栅相结合的技术具有良好的发展前景.

关键词：等效氧化层厚度；氮化硅/氮氧化硅复合叠层栅介质；高 k；硼穿通；金属栅

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