# A 12bit 300MHz Current-Steering CMOS D/A Converter *

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**Abstract:** The proposed DAC consists of a unit current-cell matrix for 8MSBs and a binary-weighted array for 4LSBs, trading-off between the precision, speed, and size of the chip. In order to ensure the linearity of the DAC, a double Centro symmetric current matrix is designed by the $Q^2$ random walk strategy. To achieve better dynamic performance, a latch is added in front of the current switch to change the input signal, such as its optimal cross-point and voltage level. For a 12bit resolution, the converter reaches an update rate of 300MHz.

**Key words:** D/A converter; current-steering; CMOS mixed integrated circuit; cross-point; $Q^2$ random walk
**EEACC:** 1265H; 1280; 2570
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## 1 Introduction

The digital to analog converter (DAC), widely used in the modern digital and analog circuits, is a very important component of the interface. The current steering DAC is based on an array of matched current cells organized in unary encoded or binary weighted elements that are steered to the DAC output depending on the digital input code. The segmented architecture is most frequently used to combine high conversion rate and high resolution. In this architecture the least significant bits steer binary weighted current sources, while the most significant bits, which are thermometer encoded, steer a unary current source array[1]. The influence of current switches on output glitch of the high-speed current-steering CMOS DAC is thoroughly analyzed, and the methods for reducing glitch are presented[2].

The proposed DAC in this work is composed of a unit current-cell matrix for 8MSBs and a binary-weighted array for 4LSBs to obtain high linearity at 12bit level. In double centro symmetric current matrices, the $Q^2$ random walk strategy is adopted to improve the nonlinearity, which can be degraded by the symmetric error and two-dimensional graded error of the DAC. In order to achieve better dynamic performance, a latch has been added in front of the current switch to change the input signal, such as its optimal cross-point and voltage level. The delay time difference of digital signals is minimized with the intermediate latches placed in front of the related decoders. In addition, a clock tree is designed to make sure that the difference in delay among all the branches from the source pins to drive pins after routing is minimized.

## 2 DAC architecture

Considering a $N$ bit current steering segmented DAC with a unit current source $I$: the $N_1$ MSBs control $2^{N_1} - 1$ equal current source of $2^{N_2} I$, and the $N_2$ LSBs control $N_2$ binary weighted current sources multiple of $I$. A simple estimation for the integral nonlinearity (INL) is found by adding the variances of $2^N - 1$ uncorrelated current sources[3]. One sigma confidence value for the INL is given by

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$$\mathrm{INL} \approx \sqrt{2^{N-1}}\,\frac{\sigma}{I} \times \mathrm{LSB} \qquad (1)$$

where $\sigma/I$ is the unit current source relative standard deviation. Equation (1) shows that the INL is independent of the used segmentation and it is only a function of the required accuracy. The worst differential nonlinearity (DNL) is defined in the transition from the binary weighted LSBs to the unity decoded MSBs[3]. One sigma confidence value for the DNL is given by

$$\mathrm{DNL} \approx \sqrt{2^{N_2}}\,\frac{\sigma}{I} \times \mathrm{LSB} \qquad (2)$$

The INL related yield specification imposes a maximum constraint on the allowed mismatch of the unit current source. This constraint results in a minimum channel area dimension for the transistor as is given by

$$WL = \frac{I^2}{2\sigma^2}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS} - V_T)^2}\right] \qquad (3)$$

where $A_\beta$ and $A_{VT}$ are mismatch technology parameters and $V_{GS} - V_T$ is the gate overdrive voltage of the current source transistor.

To achieve good DNL and INL specification, the number of bits implemented in the binary weighted part of the DAC should to be small[1]. For every extra bit implemented in the unity decoded part, however, the number of control lines needed to select the current sources doubles and the decoding logic complexity increase significantly. Equally important, the area used by the decoding inside the matrix increases and consequently the process and electric systematic errors become more difficult to compensate[1]. A direct consequence is often a reduction in the maximum operating speed. In addition, the area occupied by interconnections inside the decoding circuit quickly increases. The area of interconnections is obtained using silicon ensemble (SE) that is used to produce a layout of the netlist generated by the synthesis tool. The 12bit DAC is implemented as a segmented current DAC. Figure 1 gives a schematic representation of the realized chip. The DAC is composed of the unit current-cell matrix for 8MSBs and the binary-weighted array for 4LSBs, considering the error of circuit, speed, yield, and chip area at 12bit resolution.

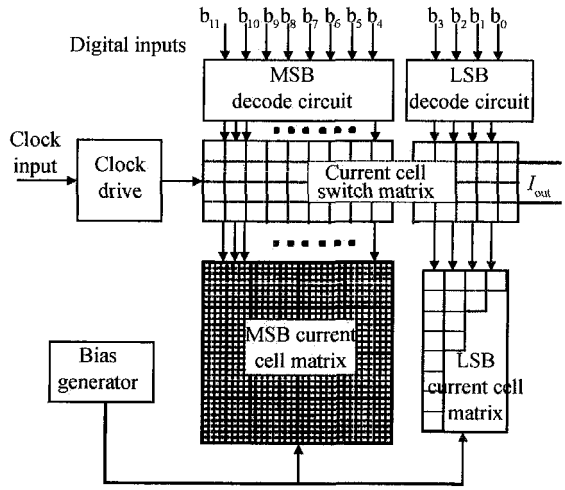


Fig. 1 Simplified DAC architecture with current

## 3 Static performance

In the unit decoded matrix, it is difficult to make current sources identical due to layout mismatches, output impedance of the current source and switch, edge effects, voltage drops in the supply lines, thermal gradients, doping gradient, and oxide thickness. The nonlinear secondary effects cause graded, symmetrical, and random errors, thus result in the reduced linearity of DACs. The proposed DAC employs a novel switching scheme to minimize the degradation of integral linearity caused by mismatches of current sources. This switching scheme will be referred to as quad quadrant ($Q^2$), because four (quad) units in every quadrant compose one current source[4]. The switching sequence of the unit current cells in the matrix for 8MSBs is illustrated in Fig. 2. The 256 current sources are divided into 16 centro symmetric regions, and then the 16 current sources in every region are divided into 16 centro symmetric regions. Since the 16 current sources in every region do not have exactly the residue, there is a remaining small

second-order residue. By "random walking" through the 256 current sources, the residual error is not accumulated but rather "randomized", hence named $Q^2$ random walk switching scheme. Only 255 current sources are required for the DAC function. One of the 256 current sources is used as a biasing circuit.

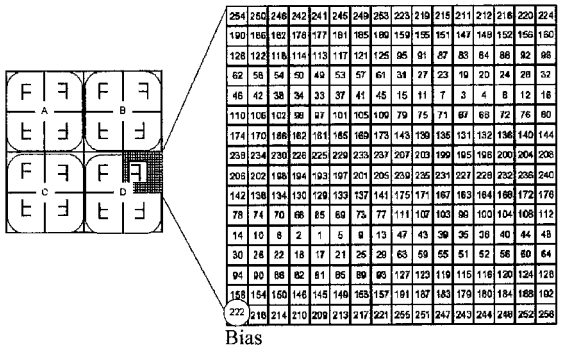


Fig. 2　Switching sequence of the $Q^2$ random walk switching scheme

## 4 Dynamic performance

It is well known that the dynamic performance of a current steering DAC is limited by three factors: (1) voltage fluctuation in the output nodes of the current sources due to improper timing of the switching OFF and ON of the transistors; (2) digital signal feed-through through the gate-drain capacitance from the current switches directly to the output; (3) imperfect synchronization of the control signals of the switching transistors[5,6].

Figure 3 shows the figure of the unit current cell of a current-steering DAC where the parasitic capacitance $C_p$ is indicated. The unit current cell consists of the pMOS switching transistors $M_{S1}$ and $M_{S2}$, the output resister $R_L$, and the pMOS current source transistor $M_C$. To determine the dimensions of the transistor $M_{S1}$, $M_{S2}$ and $M_C$ are taken into account[7]. pMOS can decrease the high frequency noise generated by common substrate at the n-well process.

During the switching OFF or ON state of the transistor, the discharge or charge of the parasitic capacitance $C_p$ takes place, leading to a deterioration of the dynamic performance of the DAC. Especially, two switching transistors can be at the OFF-state simultaneously for a short period of time. In order to avoid this situation, the general way is to adjust the cross-point of control signals, and the time of two switching transistors being at the ON-state must be shortened. Therefore, the cross point must be carefully selected.

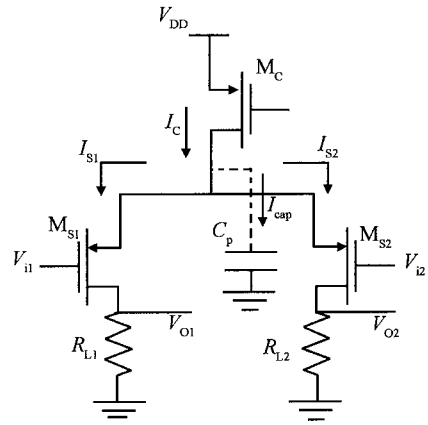


Fig. 3　Basic current cell block

As shown in Fig. 3, at the node A:

$$I_s = I_1 + I_2 + I_{cap} \tag{4}$$

where $I_s$ is the current of the cell, $I_1$ and $I_2$ are the output current of two switching transistors, and $I_{cap}$ is the discharge and charge current of the parasitic capacitance $C_p$.

Provided that $I_{cap} = 0$, the voltage variation at the node A is minimized when the switching control signals change. Namely,

$$I_s = I_1 + I_2 \tag{5}$$

Even as the switching control signals appear in the cross-point and the two pMOS switching transistors are at the ON-state, the current of the two pMOS switching transistors can be approximately expressed as

$$I_1 = \frac{\mu_p C_{ox}}{2} \times \frac{W}{L} (V_{GS1} - V_T)^2 \tag{6}$$

$$I_2 = \frac{\mu_p C_{ox}}{2} \times \frac{W}{L} (V_{GS2} - V_T)^2 \tag{7}$$

where $\mu_p C_{ox}$ is the device-transconductance parameter and $V_{GS}$-$V_T$ is the gate overdrive voltage of the transistor. When the switching control signals appear in the cross-point, the following formula is ob-

tained.

$$V_{GS1} = V_{GS2} = V_{GS(CP)} \tag{8}$$

Combining Eqs. (6)～(8), we obtain

$$V_{GS(CP)} = V_T + \sqrt{I_C/2K}$$
$$K = \mu_p C_{ox} W/2L \tag{9}$$

when one pMOS switching transistor is in the ON-state and the other is in the OFF-state, the voltage is given by

$$V_{GS(ON)} = V_T + \sqrt{I_C/K} \tag{10}$$

Combining Eqs. (9) and (10), the optimal cross-point voltage is calculated by the following formula.

$$V_{G(CP)} = V_{GS(ON)} - V_{GS(CP)} = \left(1 - \frac{1}{\sqrt{2}}\right)\sqrt{I_S/K} \tag{11}$$

For the nMOS transistor, the optimal cross-point voltage is higher than $V_{G(CP)}$, namely $V_{DD} - V_{G(CP)}$.

This project is to minimize the feedthrough to the output lines. The drain of the switching transistors is isolated from the output lines by adding two cascaded transistors (with the same dimensions as the switching transistors), as shown in Fig. 4[8].

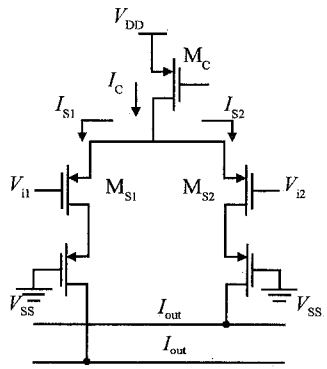


Fig. 4 Current cell with cascaded transistors

The proposed DAC employs extra digital latches just in front of the unit current cells to synchronize the digital inputs as well as employ the cascaded current sources to minimize the current variation effect. This is to overcome the skew between the row and the column select signals in the local decoder.

## 5 DAC implementation

The chip photograph is shown in Fig. 5. The chip has been implemented in a 2-poly and 4-metal 0.35μm CMOS process of Chartered Foundry and occupies the active die area of 1.0mm ×1.6mm. The digital encoder is placed on the top of the chip, far away and well shielded form the sensitive analog parts. During the layout of the current sources matrix, cadence Skill language is used to help the sorting and routing of the unit current sources, which greatly improves the design efficiency and guarantees the success of the tape out. Different power supply lines have been used for different parts of the circuit to reduce the noise coupling to the sensitive analog blocks[8]. Finally, in the very few exception where digital signals cross sensitive analog lines, a cleanly biased metal line is used as a shield. The clock driver which drives the digital encoder and analog latches in the switch array has been added to the chip. The clock is distributed through a tree to ensure low skew between the different analog latches (see Fig. 5). The clock tree is routed on the top level metal layer (lowest resistance).

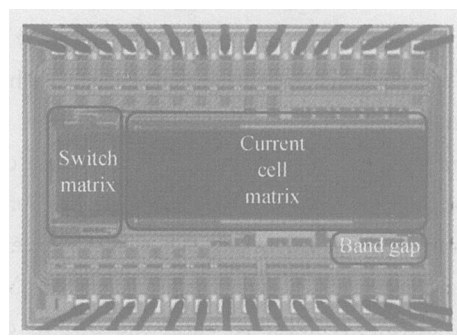


Fig. 5 Chip photograph of the D/A converter

## 6 Experiment results

The DAC is measured at 3.3V and the maximum output current for the 50Ω termination resister is 20mA to obtain the maximum single-ended analog output voltage of 1V. As show in Fig. 6, the

measured DNL and INL of the prototype DAC are within ±1. 1LSB and ±1. 6LSB, respectively. Figure 7 shows the output spectrum of the DAC with a 9MHz input signal at a 300MHz update rate. The measured spurious-free dynamic range (SFDR) is 66dB. Figure 8 shows the measured SFDR of the prototype DAC with different input signal frequencies at 300MHz. Table 1 summarizes the performance of the DAC and the AD9753 of the analog device. Their performances are very similar.

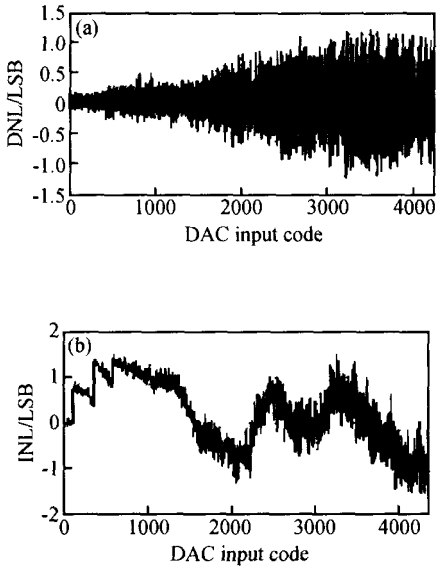


Fig. 6　DNL (a) and INL (b) measurement

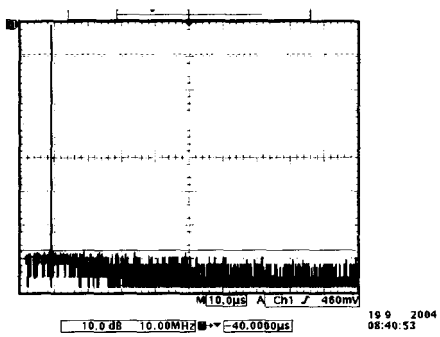


Fig. 7　Output spectrum at 300MHz update rate approximately 9MHz signal

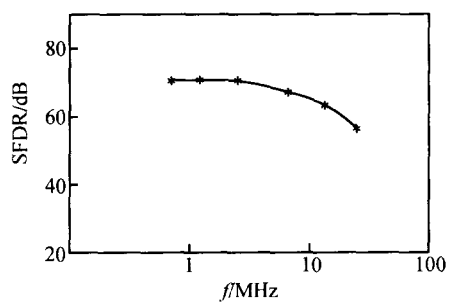


Fig. 8　Measured SFDR

Table 1　Comparison of performance of 12bit DACs

| Parameter | This paper | AD9753[9] |
|---|---|---|
| Resolution | 12bit | 12bit |
| Update rate | 300MHz | 300MHz |
| DNL | 1. 1LSB | 1. 0LSB |
| INL | 1. 6LSB | 1. 5LSB |
| SFDR | 66dB (9MHz @300MSPS) | 69dB (26MHz @300MSPS) |
| Power voltage | 3. 3V | 3. 3V |
| Power dissipation | 150mW @300MHz, 3. 3V | 155mW @300MHz, 3. 3V |
| Process | 0. 35μm | 0. 35μm |

## 7　Conclusion

In this paper a 3. 3V 12bit 300MHz CMOS DAC for a high-speed direct digital frequency synthesizer is designed and implemented. The DAC employs a novel switching scheme called $Q^2$ random walk. In order to achieve better dynamic performance, a latch has been added in front of the current switch to change the input signal, such as its optimal cross-point and voltage level. The DAC consumes 150mW in the total power consumption with a 3. 3V supply at 300MHz. The measured DNL and INL are within ± 1. 1LSB and ±1. 6LSB, respectively, and the SFDR is 66dB for a 9MHz input at an update rate of 300MHz.

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# 12 位 300MHz 电流驱动型 DAC*

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**摘要**: 在电路误差、电路占用芯片面积相互折中和妥协的前提下提出了一种 8+4 结构的电流驱动型数模转换器. 采用 $Q^2$ random walk 方法设计了一个新型的双中心对称的电流矩阵, 确保数模转换器的线性度. 分析并求出了最佳电平交叉点, 设计了电平钳位锁存器对开关电平限幅, DAC 动态性能得到改善. 在 12 位分辨率下, 刷新率达到 300MHz 以上.

**关键词**: D/A 转换器; 电流驱动; CMOS 混合集成电路; 电平交叉点; $Q^2$ random walk

**EEACC**: 1265H; 1280; 2570

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