Analysis and Optimum Design of Differential Inductors Using Distributed Capacitance Model *

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Abstract : A distributed capacitance model for monolithic inductors is developed to predict the equivalently parasitical capacitances of the inductor. The ratio of the self-resonant frequency (f_{SR}) of the differential-driven symmetric inductor to the f_{SR} of the single-ended driven inductor is firstly predicted and explained. Compared with a single-ended configuration ,experimental data demonstrate that the differential inductor offers a 127 % greater maximum quality factor and a broader range of operating frequencies. Two differential inductors with low parasitical capacitance are developed and validated.

Key words : distributed capacitance model ; self-resonant frequency ratio ; quality factor ; differential inductor ; optimum design

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1 Introduction

A monolithic inductor is an important component in highly integrated radio frequency circuits (RF ICs) for wireless communication systems. But a monolithic inductor has a low quality factor Q due to metal ohmic loss and conductive silicon substrate loss. Many researchers found quite a few methods to improve the Q of the monolithic inductor[1]. The Q and f_{SR} (self-resonant frequency) are the two most important parameters of the monolithic inductor. The lower parasitical capacitance the inductor has ,the higher Q and f_{SR} are.

It should be noted that the differential circuits (amplifiers ,mixers ,and oscillators) are commonly used in monolithic transceiver designs because of their robustness and superior noise rejection properties (e. g. power supply noise rejection). A symmetric inductor consumes less chip area as compared to single-ended equivalents when used in a typical circuit. A symmetric inductor that is excited differentially (also called a differential inductor) can realize a substantially greater factor without altering the fabrication process[2].

The distributed capacitance model (DCM) for monolithic inductors , which is for a single-ended inductor but not for the differential inductor has been studied in recent years[3~5].

In this paper ,from the view of the parasitical capacitance of the inductor ,the reason for a differential inductor with both a higher Q and f_{SR} is analyzed and firstly interpreted by DCM. Two differential inductors with the low equivalently parasitical capacitances (C_{m_m}) between the two terminals are developed and validated.

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2 Distributed capacitance model

Inductors that are driven differentially or single-ended (See Fig. 1) have different equivalent parasitic capactiances (C_{eq}). The equivalent capacitance of the spiral inductor can be expressed as[3]

$$C_{eq} = C_{m\_m} + C_{m\_s} \quad (1)$$

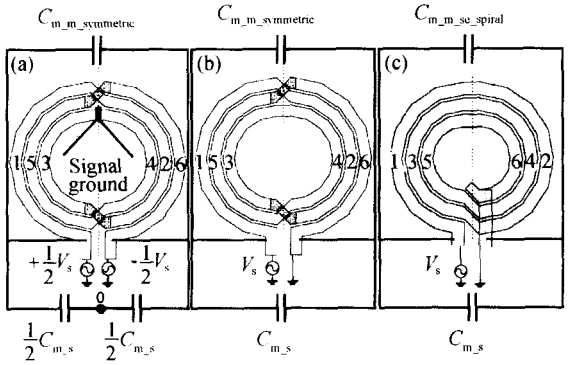

Fig. 1 Planar monolithic inductors with the same track width, space, inner, and outer radius (a) Differential-driven symmetric configuration (DSPI); (b) Single-ended-driven symmetric configuration (SSPI); (c) Single-ended spiral configuration (SEPI) 1, 2, 3, 4, 5, and 6 are current flow direction in inductor, i. e. AC signal voltage profile or half-turns serial number; Capacitances are the equivalently parasitical capacitance of the monolithic inductor.

The DSPI can be regarded as two single-ended planar inductors having same the C_{m_s}, whose connection point is signal ground and whose C_{m_s} are in series. The C_{m_m} of the DSPI are partly in series connection and partly in parallel as shown in Fig. 2 (a). The C_{m_m} of the SSPI are partly in series connection and partly in parallel and its C_{m_s} are in parallel as shown in Fig. 2 (b). The C_{m_m} of the SEPI are in series connection and its C_{m_s} are in parallel. Voltage profiles of three inductors are different as shown in Fig. 2.

2.1 Assumptions and definitions

To accurately quantify the C_{m_m} and C_{m_s} in inductors, the DCM can be used to analytically calculate them rather than qualitatively approximate. The DCM is validated by the previous papers[3,4].

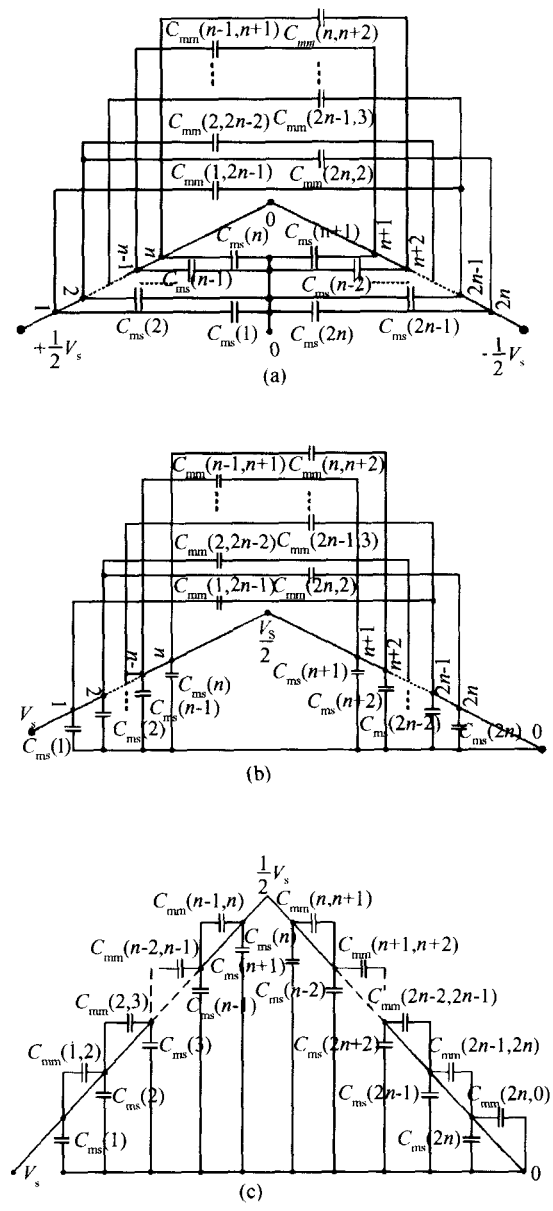

Fig. 2 Voltage profile and distributed capacitance model of the n-turn planar inductor (a) DSPI; (b) SSPI; (c) SEPI

This paper also applies the same method for the differential inductors. The fundamental assumptions of the DCM can be derived from the voltage distribution over the inductor, which is called voltage profile[4]. For the conveniences of calculation and analysis, the following assumptions are made.

(1) The same layer metal traces of the inductor have the same resistivity ρ, current, metal track width w (at least in the same half-turn), and metal thickness t;

(2) Voltage distribution is proportional to the lengths of the metal tracks[4];

(3) The kth unit voltage difference between the adjacent half-turns is regarded as a constant and is determined by averaging the beginning voltage and the ending voltage of the half-turns, regardless of the type of the inductor.

The length of each half-turn can be defined as $l_1, l_2, \cdots, l_m, l_{2n}$ (n is the half-turn number, sequential m represents current flow direction in the inductor), and the total length is defined as l_{tot} ($= l_1 + l_2 + \cdots + l_{2n}$). The AC signal voltage of one terminal of the inductor is V_{beg}, while that of the other is V_{end}. By assumptions, AC signal voltage at the end terminal of the mth half-turn inductor [$V_{end}(m)$] can be expressed as

$$V_{end}(m) = \frac{\sum_{j}^{m+1} l_j}{l_{tot}} (V_{beg} - V_{end}) \tag{2}$$

The AC signal voltage at the beginning terminal of the mth half-turn inductor [$V_{beg}(m)$] equals $V_{end}(m-1)$. $V_{beg}(0) = V_{beg}$.

2.2 Equivalent capacitance formula

The lowest layer metal track of the mth half-turn inductor is equally divided into k units ($i \to \infty$). According to assumption (2), the voltage of the ith unit is V_i,

$$V_i = V_{beg}(m) - \frac{i}{k}\Delta V_m(i) \tag{3}$$

where $\Delta V_m(i) \overset{k\to\infty}{\equiv} \frac{1}{k}(V_{beg}(m) - V_{end}(m))$. Therefore, the electrical energy stored in the capacitor between the ith unit metal and the substrate can be expressed as

$$\Delta E_{c,ms}(i) = \frac{1}{2} C(i) (\Delta V_m)^2$$

$$= \frac{1}{2} C_{ms} \frac{wl}{k} \times \left[\frac{1}{k}(V_{beg}(m) - V_{end}(m))\right]^2 \tag{4}$$

where C_{ms} represents the capacitance per unit area between the mth half-turn and the substrate. The electrical energy stored in the equivalent capacitance between the metal tracks of the $L_{ms}(m)$ and the substrate can be derived[6]

$$E_{c,m\_s} = \frac{1}{6} C_{ms} wl (V_{beg}^2 + V_{end}^2 + V_{beg} V_{end}) \tag{5}$$

Whatever the structure of the inductor is, the entire E_{c,m_s} can be figured by adding all the $E_{c,m\_s}(m)$.

The two terminal voltages of the DSPI are $+\frac{1}{2}V_s$ and $-\frac{1}{2}V_s$, respectively. Hence

$$E_{c,ms\_diff} = \frac{1}{2} \times \frac{1}{12} C_{ms} wl_{tot} V_s^2 = \frac{1}{2} C_{m\_s\_diff} V_s^2$$

So,

$$C_{m\_s\_diff} = \frac{1}{12} C_{ms} wl_{tot} \tag{6}$$

where $C_{m\_s\_diff}$ is the equivalent capacitance between the metal track and the substrate of the DSPI.

The signal terminal voltage of the SEPI is V_s and that of the other terminal is 0, hence

$$E_{c,ms\_diff} = \frac{1}{2} \times \frac{1}{3} C_{ms} wl_{tot} V_s^2 = \frac{1}{2} C_{m\_s\_se} V_s^2$$

So,

$$C_{m\_s\_se} = \frac{1}{3} C_{ms} wl \tag{7}$$

where $C_{m\_s\_se}$ is the equivalent capacitance between the metal track and the substrate of the SEPI.

According to Eqs. (6) and (7), under the same equivalent-area between the metal track and the substrate, we can get the following equation

$$C_{m\_s\_diff} = \frac{1}{4} C_{m\_s\_se} \tag{8}$$

2.3 Equivalent capacitance C_{m_m} formula

The voltage difference between the ith and jth half-turn can be expressed as

$$\Delta V_{i,j} = V_i - V_j = \frac{\sum_{k}^{j} l_k}{l_{tot}} \times (V_{beg} - V_{end}),$$
$$0 \le i, j \le n \tag{9}$$

The electrical energy stored in the equivalent capacitance between the metal tracks of the ith half-turn and jth half-turn can be expressed as

$$E_{c,m\_m}(i,j) = \sum_{k}^{2n-2} \Delta E_{c,m\_m}(k) = \frac{1}{2} \times \frac{C_{mm\_ij} W (l_i + l_j) \left(\sum_{k=i+1}^{j} l_k\right)^2}{2 l_{tot}^2} (V_{beg} - V_{end})^2 \tag{10}$$

where C_{mm_ij} is the unit capacitance between the ith and jth adjacent half-turns of the inductor; W is the metal tracks width w of the inductor when the ith half-turn and jth half-turn are stacked or metal thickness t when the ith half-turn and jth half-turn are in the same layer.

Regardless of the structures (stacked, spiral, symmetric, etc.), and driven modes (differentially or single-ended), the electrical energy stored in the equivalent capacitance between the metal can be expressed as the sum of the electrical energy stored in the equivalent capacitance between the metal traces at the same layers and at the adjacent layers. Different C_{m_m} formulas can be derived from Eq. (10) and $E_{c,mm} = \frac{1}{2} C_{m\_m} (V_{beg} - V_{end})^2$. We define the C_{m_m} of the DSPI as $C_{m\_m\_diff}$, the C_{m_m} of the SSEI as $C_{m\_m\_diff\_se}$, and the C_{m_m} of the SEPI as $C_{m\_m\_se\_spiral}$. Thus,

$$C_{m\_m\_diff} = C_{m\_m\_diff\_se} = \sum_{i=1}^{n-1} C_{mm}(i, 2n-i) \frac{w(l_i + l_{2n-i})}{2} \left(\frac{l_i}{l_{tot}} \right)^2 + \sum_{i=2}^{n} C_{mm}(i, 2n-i+2) \frac{w(l_i + l_{2n-i+2})}{2} \left(\frac{l_i}{l_{tot}} \right)^2 \quad (11)$$

$$C_{m\_m\_se\_spiral} = \sum_{i=1}^{2n-2} \left(C_{mm}(i, i+2) \frac{w(l_i + l_{i+2})}{2} \left(\frac{l_i + l_{i+2}}{l_{tot}} \right)^2 \right) \quad (12)$$

3 Experiment and discussions

In order to verify accuracy, the inductors have been fabricated in a 0.35μm two-poly four-metal CMOS processes as shown in Fig. 3. The prototype chips also include the de-embed layouts to calibrate the on-wafer testing wiring and pads[7]. The S parameters are measured by a network analyzer and Cascade Microtech Probe Station using coplanar ground-signal-ground probes.

3.1 Ratio of self-resonant frequency

The equivalent capacitance of the inductor can be calculated when the inductance is gotten. According to previous equations, the self-resonant frequency ratio of the optional two inductors with equivalent inductance L_{eq1}, L_{eq2} and the equivalent capacitor C_{eq1}, C_{eq2}, respectively, can be expressed as

$$\text{Ratio}_{f_{SR}} = \frac{f_{SR}^{L_1}}{f_{SR}^{L_2}} = \sqrt{\frac{L_{eq2} C_{eq2}}{L_{eq1} C_{eq1}}} \quad (13)$$

The inductance $L_{unsymmetric}$ equals $L_{symmetric}$ approximately, if the current flows in the same direction along each adjacent conductor of the planar inductors with the same geometric parameters [such as Figs. 1(a), (b), and (c)], and the voltage difference between the adjacent turns of the DSPI and SSPI is larger than those of the SEPI, so $C_{m\_m\_SSPI} = C_{m\_m\_DSPI} > C_{m\_m\_SEPI}$, but $4C_{m\_s\_DSPI} = C_{m\_s\_SSPI} = C_{m\_m\_SEPI}$, therefore, $f_{SR\_DSPI} > f_{SR\_SEP} > f_{SR\_SSPI}$ and $Q_{DSPI} > Q_{SEPI} > Q_{SSPI}$. This conclusion and Equation (13) can offer design guidelines for inductor and circuit configurations.

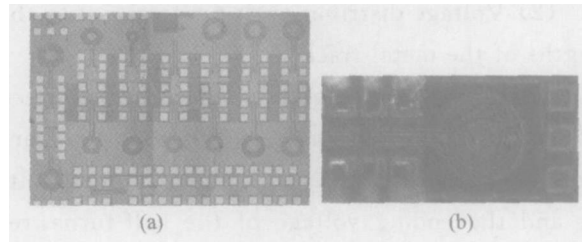

Fig. 3 Die photos of the inductors in 0.35m CMOS processes (a) and one inductor with probes (b)

The self-resonant frequency ratio ($\text{Ratio}_{f_{SR}}$) of the DSPI to the same inductor that is driven single-ended can be expressed as

$$1 < \text{Ratio}_{f_{SR}} = \frac{f_{SR\_diff}}{f_{SR\_se}} = \sqrt{\frac{4 + C_{m\_m} / C_{m\_s\_diff}}{1 + C_{m\_n} / C_{m\_s\_diff}}} < 2 \quad (14)$$

Figure 4(b) shows that the $\text{Ratio}_{f_{SR}}$ decreases with the $C_{m\_m} / C_{m\_s\_diff}$. The $\text{Ratio}_{f_{SR}}$ can be predicted and explained from Eq. (14). Compared with a single-ended configuration, the experimental data demonstrate that the differential inductor offers a 127% greater Q_{max} and a much broader range of operating frequencies. In Fig. 4(a) $\text{Ratio}_{f_{SR}}(L_1) / \text{Ratio}_{f_{SR}}(L_2) = 1.55$. The pn junction is formed at the interface

between the n-well and p-substrate, and the pn junction capacitor is in series with the oxide capacitance between the inductor and the silicon substrate, thus the equivalent C_{m_s} are greatly reduced, but the C_{m_m} of both inductors are the same, i. e. $C_{m\_m}/C_{m\_s\_diff}$ is variable, which results in the different $\text{Ratio}_{f_{SR}}$. The patterned ground shielding made of the lowest layer metal reduces the substrate loss more than the patterned n-well floating does, therefore, $Q_{se}^{L_1} > Q_{se}^{L_2}$ at a low frequency and $Q^{L_1} < Q^{L_2}$ at a high frequency due to $f_{SR}^{L_2} > f_{SR}^{L_1}$.

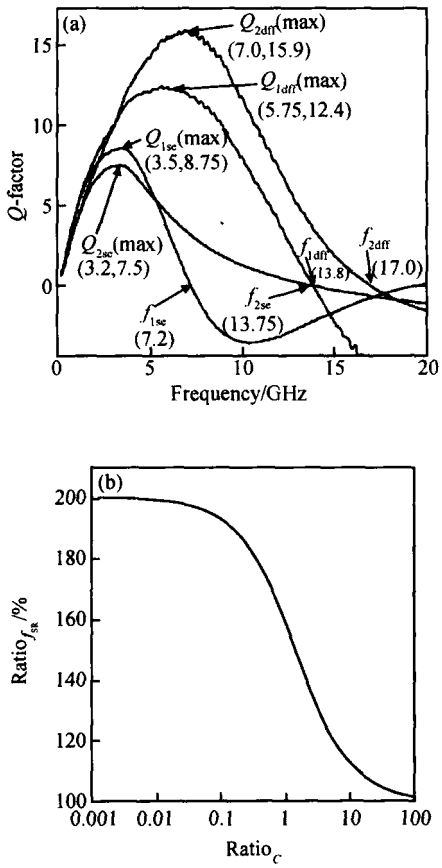

Fig. 4　(a) Q factor as a function of fregnency; (b) $\text{Ratio}_{f_{SR}}$ as a function of $\text{Ratio}_C = C_{m\_n}/C_{m\_s\_diff}$

3.2　Optimum design of differential inductor

The lower the total parasitic capacitance is, the higher quality factor the inductor has. Two kinds of optimum designs of the DSPI are developed. $C_{m\_m\_diff}$ is reduced by decreasing the voltage difference between the adjacent turns in Fig. 5 (a) through multilevel interconnects and by increasing the space of adjacent turns with larger voltage difference as shown in Fig. 5(b). According to Eq. (6), the C_{m_m} will be reduced if the lowest metal tracks layer of the stacked or 3D inductor has the voltage which is nearer to the signal ground. Compared to the conventionally differential inductor with the same width and turns, two differential inductors with low C_{m_m} structures have high Q and f_{SR} as shown in Fig. 6.

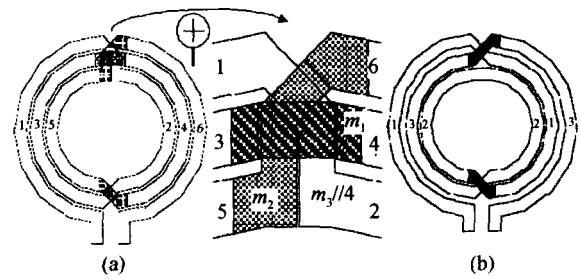

Fig. 5　Two differential inductors with low C_{m_m}　1, 2, 3, 4, 5, and 6 are current in inductor flow direction, i. e. AC signal voltage profile. In m_i, i represents metal layer number.

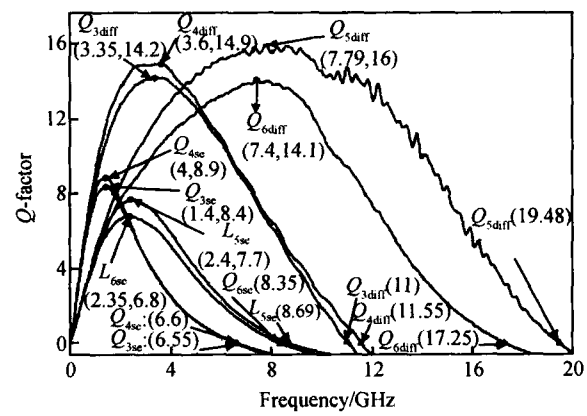

Fig. 6　Q and f_{SR} of two differential inductors with low C_{m_m}　L_3 is the inductor in Fig. 5(b) and L_5 is the inductor in Fig. 5(a); L_4 and L_6 are the conventionally differential inductor with the same width and turns as L_3 and L_5, respectively.

3.3　Prediction errors

Table 1 is the prediction errors of the inductors with the DCM. The prediction error of f_{SR} with the DCM is less than 10 %, demonstrating the accuracy of the DCM. The DCM would have higher accuracy for the different structure inductors if the

current crowding effects are considered in assumption (2).

Table 1 Prediction errors with DCM

f_{SR}	L_{1se}	L_{2se}	L_{3se}	L_{4se}	L_{5se}	L_{6se}
Error/ %	6.4	8.2	5.6	7.3	6.7	7.2
f_{SR}	L_{1diff}	L_{2diff}	L_{3diff}	L_{4diff}	L_{5diff}	L_{6diff}
Error/ %	8.3	9.2	6.4	9.5	7.8	8.9

4 Conclusion

The DCMs of inductors are developed to accurately quantify the C_{m_m} and the C_{m_s} of the symmetric and single-ended inductor. The C_{m_s} of the differential inductor is only a quarter of the C_{m_s} of the single-ended inductor, therefore, the differential inductor has higher a Q and f_{SR}. The ratio of the f_{SR_diff} to the f_{SR_se} are firstly predicted and explained. Two optimum differential-inductors with low C_{m_m} are developed and validated.

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用分布电容模型分析和优化差分电感*

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摘要: 建立了预测片上等效寄生电容的片上电感分布电容模型. 预测和解释了差分电感的自激振荡频率的差异. 实测数据显示, 与单端驱动模式下的相同对称电感相比, 差分驱动模式电感提高最大品质因数 127 %, 具有更大的工作频率范围. 设计和验证了低寄生电容的差分电感.

关键词: 分布电容模型; 自激振荡频率比; 品质因素; 差分电感; 优化设计

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