A VHF PECVD Micro-Crystalline Silicon Bottom Gate TFT with a Thin Incubation Layer *

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Abstract : The incubation layer with amorphous structure between the substrate and crystalline layer may obviously affect the performance for a microcrystalline Si thin film transistor (μc-Si TFT) ,especially for the bottom gate TFT (BG-TFT) . It is found that decreasing the ratio of $SiH_4/(H_2 + SiH_4)$ is an effective way to decrease the incubation layer thickness of μc-Si directly deposited by VHF PECVD without any further thermal or laser treatment. Based on the μc-Si with a thin incubation layer ,the BG-TFT with Al/ SiN_x/ μc-Si/ n^+-μc-Si/ Al structure is fabricated. The ratio of on-state current to off-state current is up to 10^6 ,the mobility is around 0. 7$cm^2/(V \cdot s)$,and the threshold voltage is about 5V.

Key words : microcrystalline silicon ; incubation layer ; silicon concentration ; bottom gate μc-Si TFT
PACC : 7360 ; 7360F ; 7390
CLC number : TN321$^+$. 5 **Document code : A** **Article ID :** 0253-4177(2005)06-1121-05

1 Introduction

With the development of new panel display technology ,such as AMOLED ,thin film transistors with good performance and low cost are required. Recently ,intrinsic μc-Si (microcrystalline silicon) without any further treatment by thermal or laser annealing is extremely appealing due to its higher mobility and better stability than amorphous silicon (a-Si) TFT and lower cost than polycrystalline (poly-Si) TFT[1,2]. Compared with the mature a-Si TFT technology ,μc-Si TFT could be used in higher-resolution displays ,or it would allow the use of smaller size TFT to increase optical aperture. Furthermore , the fabrication process of bottom-gate (BG) μc-Si TFTs is almost compatible with that of the a-Si TFTs ,that is to say ,the same product line with which today produce a-Si TFT could easily be switched to BG μc-Si TFT production. Generally

* Project supported by the National Natural Science Foundation of China (Nos. 60437030 ,60077011 ,and 69907002) ,the National High Technology Research and Development Program of China (No. 2002AA303261) , and the Natural Science Fundation of Tianjin (No. 02360211)

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Received 4 November 2004 ,revised manuscript received 21 February 2005

speaking, technology of a-Si TFTs is relatively mature and the research for poly-Si TFTs also has been developed widely and much novel technologies[3] have been applied. However, research for μc-Si TFT is still in the beginning steps, its performance is far from perfect and the factors that affect its characteristics are complex. One of them is that an incubation layer with amorphous structure clings on top of the substrate though the rest of the film may exhibit a high crystallinity[4~6]. The incubation layer may obviously affect the performance for TFT, especially for BG μc-Si TFT. In this paper, the studies on the incubation layer are presented and the performance of a BG μc-Si TFT with a thin incubation layer is shown.

2 Experimental details

μc-Si thin films were deposited by VHF-PECVD with the active frequency of 60MHz, the silicon concentration diluted by hydrogen ($S_c = SiH_4/(SiH_4 + H_2)$) was varied from 0.67% to 8%, film thickness changed from 10nm to 1000nm and the pressure and substrate temperature were fixed at 120Pa and 220 ℃, respectively. The same excited power, 25W, was applied for all samples. The crystallinity of μc-Si is measured by Raman scattering using a 632.8nm He-Ne laser. Here, the crystalline volume fraction (X_c) was used to describe the crystalline degree of the films. As well known, the X_c of the sample can be deduced from its Raman scattering spectra by the ratio of $X_c = I_c/(I_c + I_a) = (I_{520} + I_{510})/(I_{520} + I_{510} + I_{480})$, where I_c is the crystalline intensity peak at 520 and 510, and I_a is the amorphous intensity at 480cm^{-1}. Conduction activation energy (E_a) was measured utilizing the equipment designed by ourselves. The film thickness is measured by an AMBIOS Technology Inc. XP-2™ Profilometer with an ability to measure precision step heights from under 10nm to as large as 100μm and to measure micro-roughness, with 0.1nm resolution over short distance, as well as waviness.

For the fabrication of the BG μc-Si TFT, a four-mask process with specially designed layout was used. First, we thermally evaporated Al, and patterned it using reactive ion etching to form the gate electrode. Then, deposited 200nm SiN_x as the gate insulator. Next, 160nm of intrinsic μc-Si as the channel layer and 50～100nm of n^+ μc-Si as the contact layer were grown on the SiN_x substrate orderly without breaking vacuum. Afterwards, the channel was defined by photolithography and wet etching, then Al was thermally evaporated and patterned by wet etching to form the source and drain electrodes. The active channel was configurated by conventional back-channel etching. Finally, we opened the contact holes to the TFT gate electrode.

3 Results and discussion

3.1 Incubation layer

To achieve a good μc-Si TFT, crystallinity of the μc-Si film is an essential factor. Figure 1 shows the Raman spectra of the 1000nm thick μc-Si film with increasing hydrogen dilution under other identical deposition conditions. It can be observed that the Raman spectra peak gradually changes from an amorphous band at 480cm^{-1} to the crystal band at 520cm^{-1} above a certain threshold dilution ratio around the S_c of 6%. However, it is different when a thinner (<0.2μm) μc-Si is used as the TFT chan-

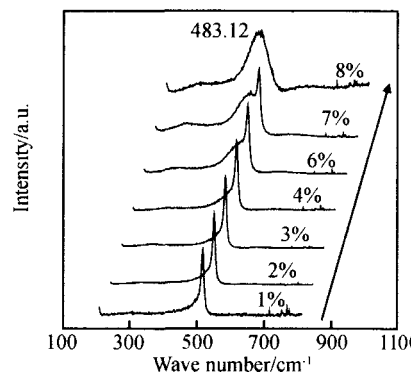

Fig. 1 Raman spectra of the 1000nm μc-Si film

nel as shown in Fig. 2. For the thinner μc-Si film, the phase transition point is around 4 % of S_c. This could be attributed to the effect of the initial amorphous layer that is called the incubation layer, existing between the substrate and the crystalline layer. Apparently, the thinner the μc-Si film is, the more obvious the effect of the incubation layer is, which will make the μc-Si TFT, especially the bottom gate TFT, show characteristics of an a-Si TFT instead of the advantages of a μc-Si TFT. According to our experiment results, decreasing S_c is an effective way to thin the incubation layer.

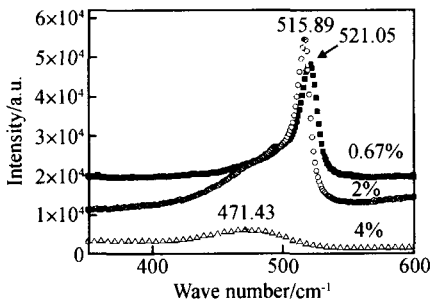

Fig. 2　Raman spectra of the 160nm μc-Si film with variable S_c

When S_c = 4 %, the thickness of the incubation layer is above 200nm, which is thicker than the channel thickness of μc-Si TFT, while it is down to 60～70nm for S_c = 2 % and becomes thinner (about 20nm) for S_c = 0. 67 % as shown in Figs. 3 (a) and (b), respectively. From Fig. 4, it is important to note that for μc-Si film deposited at S_c = 0. 67 %, the X_c of its 20nm incubation layer is nearly 50 %, which can be seen in Fig. 5. Increasing the film thickness, X_c tends to rise slowly. X_c of the μc-Si film deposited at S_c = 2 % with 60nm incubation layer is nearly 20 % and shows the same trendency.

Thus far, we have effectively thinned the initial amorphous incubation layer in the μc-Si film by simply using high H dilution of SiH_4. However, the drawback of too high an H dilution is that it results in a lower deposition rate and lower activation energy (E_a). The deposition rate of a μc-Si film deposited at S_c = 0. 67 %, 25W, and 120Pa is only 0. 968nm/s and the E_a is about 0. 1eV. The film

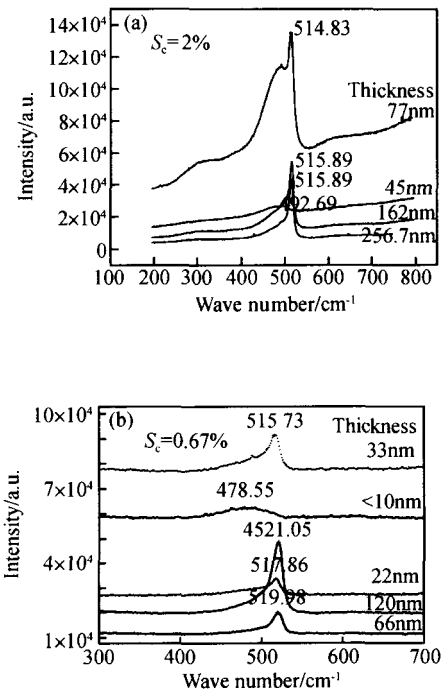

Fig. 3　Raman spectra for μc-Si film deposited at S_c = 2 % (a) and 0. 67 % (b) with variable film thickness

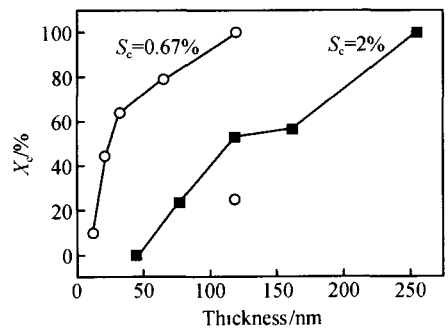

Fig. 4　Variation of X_c with the thickness of μc-Si thin film at different silicon concentration

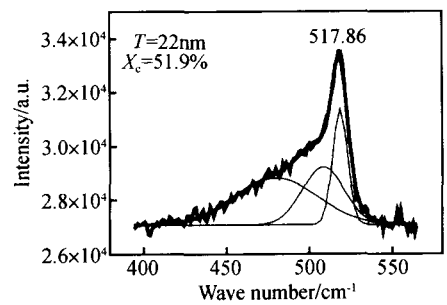

Fig. 5　Analysis of Raman for 22nm at S_c = 0. 67 %

with so low an E_a can not be used to make a TFT. The drastic decreasing of E_a may be caused by the

oxygen contamination. For the growth of μc-Si, atomic hydrogen reaching the film-growing surface breaks weak Si—Si bonds in the amorphous network structure, leading to a removal of Si atoms weakly bonded to another Si. This site is replaced with a new film precursor SiH_3, creating rigid and strong Si—Si bonds, giving rise to an ordered structure[6]. Under too high an H dilution condition, the role of the atomic hydrogen etching is too great, which leads to much void in the μc-Si film between the columnar grains, and then oxygen penetration into it[7]. Strong oxygen contamination makes the threshold voltage of the TFT negative and gives rise to a large leakage current as well as the deterioration of gate modulation effect. In addition, Schropp *et al*. has found that oxygen incorporation increases linearly with decreasing deposition rate[8]. Therefore, from the view of an oxygen contamination point, the S_c should not be too low.

Considering the incubation layer thickness and the oxygen contamination, we try to choose the S_c for the μc-Si film used as the TFT channel as 2 %. In this case, its E_a is 0.45eV and the thickness of the incubation layer is about 60nm (X_c of the incubation layer is about 30 %), which may be relatively suitable for the BG μc-Si TFT. The optimum structure has to be studied further in the future.

3.2 BG μc-Si TFT

Bottom gate TFTs were fabricated with the μc-Si deposited at an S_c of 2 %. The almost same fabrication processes as those for making a-Si TFT were employed to fabricate a μc-Si TFT. The transfer characteristic curve of the resulted TFT without any other treatment and LDD structure is shown in Fig. 6. The ratio of on-state current to the off-state current (I_{on}/I_{off}) is up to 10^6, the mobility is around 0.7$cm^2/(V \cdot s)$, and the threshold voltage is about 5V. The TFT characteristics are comparable to those of the μc-Si TFT reported by other research groups. Further optimization, such as the μc-Si grain size, the film density, and interface treatment, is still required to make the BG μc-Si TFT show more obvious advantages than a-Si TFT.

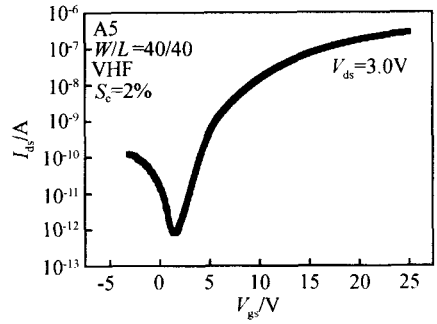

Fig. 6 Transfer characteristics of μc-Si TFT

4 Conclusion

Decreasing the silicon concentration is an effective way to achieve a μc-Si film with an ultrathin (< 20nm) incubation layer or much less by VHF-PECVD. However, too high an H dilution leads to too a low deposition rate and serious oxygen contamination. From the view of the above two points, a μc-Si film deposited at S_c of 2 % is suitable for the application of the bottom gate TFT and this TFT without any other treatment and LDD structure shows relatively good performances. Nevertheless, further optimization of the μc-Si film is still required to achieve a better bottom gate μc-Si TFT.

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薄起始层的 VHF PECVD 底栅微晶硅薄膜晶体管*

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摘要: 对微晶硅薄膜晶体管,尤其对底栅型晶体管,在衬底和晶化层间存在一层非晶相起始层,这将严重影响器件性能. 文中采用降低硅烷浓度的方法简便有效地减薄了用超高频化学气相法直接沉积的微晶硅薄膜起始层的厚度,得到起始层厚度小于 20nm 的微晶硅薄膜. 在硅烷浓度为 2 %的条件下采用四版工艺制备了具有 Al/ SiN_x/ μc-Si/ n^+-μc-Si/ Al 结构的底栅微晶硅 TFT,其开关比(I_{on}/ I_{off})达到 10^6,场效应迁移率为 0. 7cm^2/ (V ·s),阈值电压为 5V 左右.

关键词: 微晶硅; 起始层; 硅烷浓度; 底栅薄膜晶体管
PACC: 7360; 7360F; 7390
中图分类号: TN321$^+$. 5　　**文献标识码**: A　　**文章编号**: 0253-4177(2005)06-1121-05

*国家自然科学基金(批准号:60437030, 60077011 和 69907002),国家高技术研究发展计划(批准号:2002AA303261)和天津市自然科学基金(批准号:02360211)资助项目

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2004-11-04 收到,2005-02-21 定稿