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A 5mW 1.8V Low Over-Sampling Ratio ΣΔ Modulator with 81dB Dynamic Range*

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Abstract: This work demonstrates that the ΣΔ modulator with a low oversampling ratio is a viable option for the high-resolution digitization in a low-voltage environment. Low power dissipation is achieved by designing a low-OSR modulator based on differential cascade architecture, while large signal swing maintained to achieve a high dynamic range in the low-voltage environment. Operating from a voltage supply of 1.8V, the sixth-order cascade modulator at a sampling frequency of 4-MHz with an OSR of 24 achieves a dynamic range of 81dB for a 80-kHz test signal, while dissipating only 5mW.

Key words: ΣΔ modulator; low over sampling ratio; low power; low voltage
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1 Introduction

The rapid growth in wireless communication systems with the trend toward increased digital signal processing and early digitization also increased the dynamic range and bandwidth required of the analog-to-digital converters (ADC), stimulating interest in ADCs with high resolution, wide bandwidth, and low power dissipation.

Among the wide variety of ADC architectures, the ΣΔ oversampled ADC is the most suitable option to meet the needs of current and emerging wireless transceivers, for its insensitivity to component mismatch if resolutions beyond 14 bits are envisioned[1~3].

ΣΔ modulation has been used successfully in many audio applications that require resolution as high as 16 to 18bits over signal bandwidths in the range of tens of kilohertz. In such applications, high oversampling ratios (OSR) in the range of 64 to 256 are commonly used without constraints imposed by technology, bandwidth, and power budget. However, state-of-art ΣΔ modulators employ limited low oversampling ratios due to such constraints.

Even in systems such as the global system for mobile communications (GSM), with signal bandwidths of only 100kHz, low power consumption requires ΣΔ modulators adopted in such systems have low OSRs in a range of 8 to 30[4~6]. However, characteristics of high resolutions should still be maintained.

To achieve this, the architecture must be chosen so as to adequately suppress the in-band quantization noise in the modulator output. Meeting this at low oversampling ratios is a great challenge.

The experimental ΣΔ modulator introduced in this work achieves a dynamic range of 81dB with a sampling rate of 4MHz at an OSR of 24. It operates at a supply voltage of only 1.8V with a total power dissipation of only 5mW.

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2　modulators at low oversampling ratios

If a white-noise model is assumed for the quantizer error, then the dynamic range of an ideal noise-differencing ΣΔ modulator, wherein only quantization noise is considered, is given by

$$DR_Q = \frac{3}{2}\left[\frac{2L+1}{\pi^{2L}}\right] M^{2L+1}\left[2^B - 1\right]^2 \qquad (1)$$

where L is the order of the modulator, B is the number of bits in the quantizer, and M is the OSR.

From Eq. (1), it follows that as the OSR is lowered to increase the Nyquist conversion rate or decrease sampling rate, the order of the modulator and/or the number of bits in the quantizer must be increased in order to maintain a given dynamic range. The effectiveness of increasing the order of a single-loop single-bit modulator by increasing the order of filtering in the modulator's forward path degrades rapidly at low oversampling ratios. Moreover, techniques that must be used to stabilize a high-order loop typically increase the baseband noise power relative to that assumed in Eq. (1).

The difficulties encountered in implementing stable single-loop modulators at low OSRs can be eased to some extent by multibit quantization[3]. However, some linearization means must be found to overcome the influence of mismatch-induced errors in the multibit DAC on the modulator performance. Such techniques like trimming, calibration, and dynamic element matching contribute a rise in cost, area, and complexity of ΣΔ modulators.

An alternative approach to realize high-order noise shaping at low oversampling ratios consists of cascading several low-order ΣΔ stages. In a cascaded/MASH modulator, the quantization noise of the first stage is measured in the following stage and canceled in the subsequent digital signal processing. Circuit nonidealities, such as capacitive mismatch appeared also in other structures of ΣΔ modulators, still cause a fraction of the first-stage quantization noise to leak to the overall modulator output and typically limit the achievable dynamic range. But the in-band quantization noise power no more than 30~ 40dB above the total baseband thermal noise power is sufficiently small to prevent noise leakage at the first stage from degrading the overall modulator performance[7].

A cascade ΣΔ modulator with single-bit quantizer is chosen to explore how oversampling ratio can be used effectively.

3　modulators architecture

A linearized block diagram of the experimental switched-capacitor (SC) cascade ΣΔ modulator is shown in Fig. 1. It consists of three second-order stages with single-bit quantization.

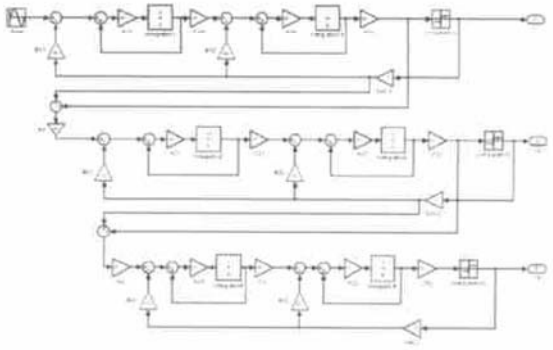

Fig. 1　Linearized block diagram of single-bit cascade ΣΔ modulator

An essential issue in the design of high-speed/low-power ΣΔ modulators is to reduce the capacitive load of the operational transconductance amplifiers (OTA) as much as possible. This can be achieved by reducing the sampling capacitance of OTAs. However, in high-resolution ΣΔ modulators, the sampling capacitance is determined by noise requirements due to the KT/C noise of the switches. Therefore, there must be a power-speed-resolution tradeoff of the ΣΔ modulators.

We assume the input signal is V_{ref}, the signal-to-noise ratio (SNR) due to KT/C noise can be written as

$$SNR_{KT/C} = \frac{(2V_{ref})^2}{2} \times \frac{C_s M}{4kT} \qquad (2)$$

where C_s is the sampling capacitance. If it is assumed that linear setting to within 0.5 LSB of the asymptotic value is required to avoid distortion that results from incomplete settling, and if the input transistors are assumed to have a square-law response, then, following a derivation similar to that presented in Ref. [8], the power dissipation in the first integrator can be approximated by

$$P \approx \ln(2^{N+1}) \frac{C_L}{f}(V_{GS} - V_T) V_{DD} \frac{1}{T_{int}} \quad (3)$$

where $V_{GS} - V_T$ is the overdrive voltage of the input transistors, N is the linearity expressed in number of bits, C_L is the equivalent capacitance load of the integrator, and V_{DD} is the voltage supply. T_{int} is the time available for charge transfer to the integration capacitor, which under the assumption of 50% duty cycle, is given by

$$T_{int} = \frac{1}{2f_s} - T_{ovh} \quad (4)$$

where the timing overhead T_{ovh} accounts for the finite rise, fall, and nonoverlap times of the clock signals.

Then we introduce a merit of SNR/power as

$$\frac{SNR_{KT/C}}{P} \approx \frac{1}{2\ln 2^{N+1}} \times \frac{(2V_{ref})^2}{(V_{GS} - V_T) V_{DD}} \times G_{int} \times \frac{Mf T_{int}}{4kT} \quad (5)$$

where G_{int} means gain of the integrator. It follows that SNR performance achieved by unit power dissipation can be optimized by increasing gain of the integrators and decreasing the voltage supplies at a low oversampling ratio, while increasing amplitude of the input signal. As shown in Eq. (2), the white noise floor of the modulator is mainly determined by the first integrator sampling capacitance, which should be suppressed to the level well below the circuit noises. The sampling capacitance of the last stage is determined by matching considerations, and the capacitances in the other stages are scaled down progressively. While scaling down the OTAs in $V_{GS} - V_T$ terms, we can still maintain the merit shown in Eq. (5), thereby, significantly reducing the power consumption and the die area.

Behavioral simulations using Matlab were performed to find the integrator gains that maximize the dynamic range while avoiding both clipping distortion at the output of integrators and excessive leakage of the first-stage quantization noise into the output. Finite gains of OTAs have also been taken into account in the behavioral simulations[9], which can thus determine the minimum required OTA gains to avoid performance degradation. A minimum gain of 80 dB is selected for the OTAs. In fact, we can scale down the gains of the other OTAs except the first to decrease the power dissipation further.

Behavioral simulations predict a quantization noise floor of - 95dB for the modulator of Fig. 1.

4 Circuit implementation

A fully differential switched-capacitor implementation of the sixth-order cascaded ΣΔ modulator in Fig. 1 has been integrated in a 0.18μm single-poly six-metal-layer mixed-signal CMOS technology. As noted previously, because of the noise shaping provided by each stage, the circuits in the first stage are subject to the most stringent requirements. This section therefore focuses primarily on the circuit implementation of the first stage, with special consideration given to the difficulties encountered in the design for operation at a supply voltage as low as 1.8V.

4.1 Bootstrap switching sample-and-hold circuits

As shown in Fig. 2, the circuit is used to sample the continuous-time input signal to the modulator. The size of the sampling capacitors is dictated by thermal noise considerations and equals 2.5pF. A principal consideration in the design of this sample-and-hold circuit is its linearity, since errors introduced at this point add directly to the input signal. In this circuit, errors and distortion due to signal-dependent sampling timing are minimized through the use of two-phase nonoverlapped clocking with delayed bottom-plate switching[10].

The dynamic tracking nonlinearity introducing

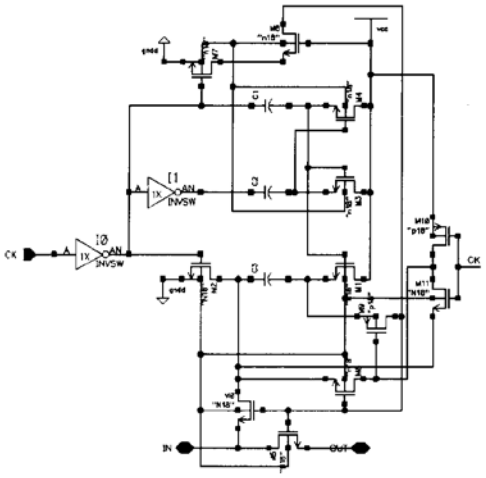

Fig. 2　Schematic of the bootstrapped sample-and-hold circuit

sampling distortion at low OSRs is caused by signal-dependent on-resistance and junction capacitance of the input sampling switches, which gets worse if a voltage supply of only 1.8V taken into account. As shown in Eq. (2), larger input signals improve the SNR performance of the modulator but incur larger distortion because voltage supply limits the sampling linear-region as

$$LR_{HALF} = V_{DD} - V_T - V_{CM} \qquad (6)$$

where V_T is the threshold voltage of the switch transistor, and V_{CM} is the input common-mode voltage. With V_{DD} of 1.8V, V_T of 0.5V, and V_{CM} of 0.9V, the linear region is much smaller than 0.4V. When the amplitude of input signal reaches to or beyond that, overall performance degrades precipitately.

To improve the linearity of the sampling operation significantly, an NMOS sampling switch with bootstrapped clocking is used[11]. The sizes of the bootstrapping capacitors and the sampling switch S_1 are the critical parameters governing the linearity of the sample-and-hold circuit. The size of the bootstrapping capacitor is determined by clock and expected precharge voltage, which determines sampling linear-region for input continuous-time signals. For a given value of both bootstrapping capacitor and sampling capacitor determined by KT/C noise performance as noted previously, increasing the width of the input sampling switch, and thus decreasing the switch on-resistance, improving the THD up to the point where the charge injection from the switch to sampling capacitor becomes significant. Therefore, a bootstrapping capacitor of 1.6pF and a sampling switch transistor size of 200μm/0.18μm were used to meet the linearity goal for the overall ΣΔ modulator. Moreover, the input common-mode voltage of the integrators is designed as 0.7V to achieve more linearity.

4.2　Delay-controlled clock generator

Operation of the modulator is controlled by a nonoverlapping two-phase clock (CK1-CK2), which is generated by the proposed circuit shown in Fig. 3.

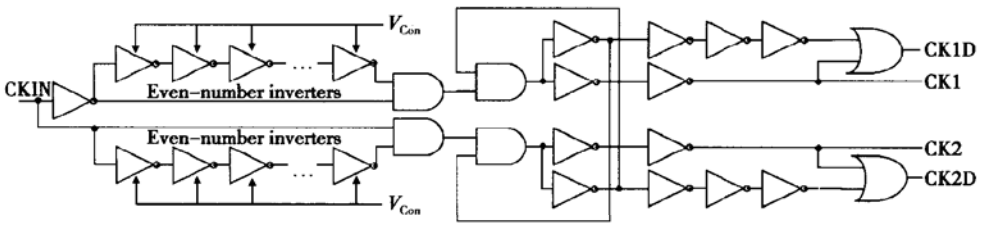

Fig. 3　Diagram of nonoverlapping two-phase clock generator

Due to the delay of the inverter the output signal is slightly shifted in phase. Thus, in the switching-off of phase 1, both the clock and its version with delayed falling edge may be overlapping (high) for a short time interval t_s, as shown in Fig. 4. Therefore, SW1 and SW1D are still conducting at the same time, and a low impedance path exists between the input signal and virtual ground,

which still cause a signal-dependent charge injection to deposit on the sampling capacitor.

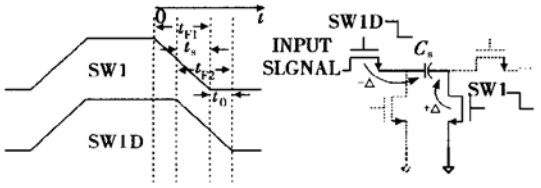

Fig. 4 Distortion due to overlapping falling-edge clocks

It is assumed that transistor of SW1 still works in the linear region, and charge injection is determined by how much charge this transistor can transfer to deposit on the sampling capacitor, thus we have

$$\begin{aligned} I(t) &= K\left\{[V_{gs}(t) - V_T]V_{ds} - \frac{1}{2}V_{ds}^2\right\} \\ \mathrm{d}Q_{ch} &= I(t)\,\mathrm{d}t \\ \mathrm{d}V_{ch} &= \frac{\mathrm{d}Q_{ch}}{C_s} = \frac{I(t)\,\mathrm{d}t}{C_s} \end{aligned} \tag{7}$$

Moreover, we assume SW1 falls linearly, which can be given by

$$V_{gs}(t) = -\frac{V_{DD}}{t_{F1}} \times t + V_{DD} \tag{8}$$

where t_{F1} is the falling-edge time interval for SW1. Therefore, charge injection can be obtained by integrating voltage variance in the time range between $t_{F1} - t_s$ and t_{F1}

$$\int_{V_{IN}}^{V_{IN}+V_{ch}} \mathrm{d}V_{ch} = \int_{t_{F1}-t_s}^{t_{F1}} \frac{K\left\{[V_{gs}(t) - V_T]V_{ds} - \frac{1}{2}V_{ds}^2\right\}}{C_s}\,\mathrm{d}t \tag{9}$$

From Fig. 4, we can see

$$t_s = t_{F2} - t_0 \tag{10}$$

where t_{F2} is the falling-edge time interval of SW1D, t_0 is the time interval that SW1 has switched off completely while SW1D is still switching off. Substituting Eqs. (8) and (10) into Eq. (9), the charge injection is given by

$$\begin{aligned} V_{ch} = {} & \frac{V_{ds}K}{C_s}\left\{-\frac{V_{DD}}{2t_{F1}}[-(t_{F2}-t_0)^2 - 2t_{F1}(t_{F2}-t_0)]\right\} \\ & + \frac{V_{ds}K}{C_s}(V_{DD} - V_T)(t_{F2} - t_0) \end{aligned} \tag{11}$$

In Eq. (11) we assume V_{ds} is very small, and so V_{ds}^2 has been omitted. It follows that there is no charge injection, if t_{F2} equals to t_0, which as expected means SW1 should completely switched off before SW1 begins to switch off.

The proposed circuit shown in Fig. 3 meets the requirement by adding an OR gate controlled by SW1 to the output of the SW1D. Furthermore, to make sure the two-phase clock nonoverlapped, a new Delay-plus-AND unit has been designed. Compared with Ref. [12], it eases critical requirements for feedback circuits and suppresses the distortion due to overlapping clocks with only a little more cost of area and power dissipation.

4.3 Operational transconductance amplifiers

The nonideality study of the previous section revealed that the main requirements for the OTA are a high gain (> 80dB) and a large dominant closed-loop pole (> 40MHz). The latter is estimated by the analysis given in Ref. [12], which concluded that the frequency of the closed-loop pole should be three times larger than the sampling frequency of the modulator. In this case, we chose a closed-loop pole at ten times the sampling frequency, thereby providing some margin for other nonidealities.

A gain-boosted folded-cascode amplifier shown in Fig. 5 is adopted to implement SC integrators for both high-gain and low-power considerations. The output swing of the OTA's determines the reference voltages, which set the capacitive load of the OTA and thereby its power consumption. In Refs. [13, 14], a simple gain-boosting structure with just two transistors greatly reduced the output swing of the OTA, for it requires a V_{gs} over the top and bottom transistors of the folded-cascode output branch. For a voltage supply of 1.8V, the resulting output swing is unacceptably low.

In this case, only a V_{dsat} is required over these transistors, and resulting output swing is increased.

The dynamic common-mode feedback (CMFB) circuit[13] composed of the switched-ca-

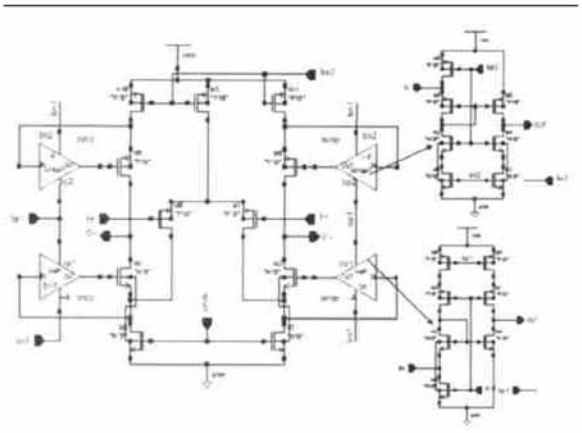

Fig. 5 Schematic of gain-boosted cascode OTA

pacitor circuits is used for power consideration and convenience of arbitrary CMFB voltage.

5 Simulation results

A layout of the experimental modulator is shown in Fig. 6. The total area, excluding the bond-pads, is 1.8mm^2. A bandgap reference voltage biasing circuit was integrated in the chip to produce the biasing current, which is duplicated in the local bias circuits.

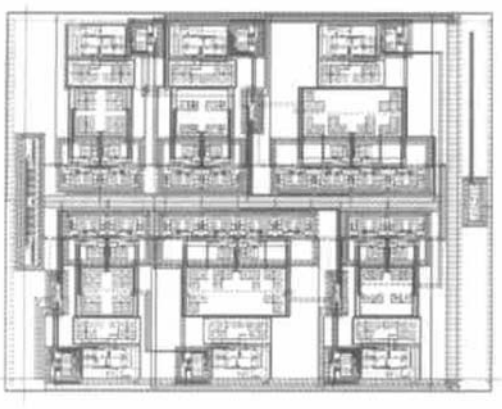

Fig. 6 Layout of ΣΔ modulator

The experimental modulator operates at a 4MHz sampling rate, which corresponds to a 167kHz Nyquist conversion rate for an OSR of 24. When operated at a 1.8V supply, the modulator dissipates only 5mW. The plot of the measured signal-to-noise ratio (SNR) versus input amplitude is shown in Fig. 7. It indicates that the experimental modulator achieves a dynamic range of 81dB.

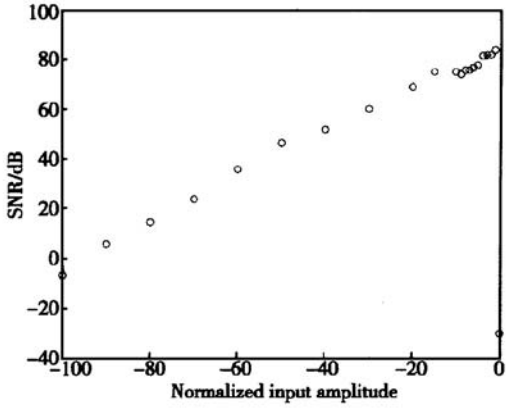

Fig. 7 SNR of ΣΔ modulator

6 Conclusion

This work shows that the ΣΔ modulator with a low oversampling ratio is a viable option for the high-resolution digitization in a low-voltage environment. Low power dissipation is achieved by designing a single-bit low-OSR modulator based on differential cascade architecture, while large signal swing maintained to achieve a high dynamic range in the low-voltage environment.

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1.8V 电源电压 81dB 动态范围的低过采样率 调制器*

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摘要: 采用 222 级联全差分结构和低电压、高线性度的电路设计实现了高动态范围、低过采样率的 ΣΔ 调制器. 在 1.8V 工作电压, 4MHz 采样频率以及 80kHz 输入信号的条件下, 该调制器能够达到 81dB 的动态范围, 功耗仅为 5mW. 结果表明此结构及电路设计可以用于在低电压工作环境的高精度模数转换中.

关键词: ΣΔ 调制器; 低过采样率; 低功耗; 低电源电压

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