第25卷第2期 半 导 体 学 报 Vol. 25, No. 2
2004年2月 CHINESE JOURNAL OF SEMICONDUCTORS Feb., 2004

A New Lifetime Prediction Model for pMOSFETs Under $V_g = V_d/2$ Mode with 2.5nm Oxide*

Hu Jing, Zhao Yao, Xu Mingzhen and Tan Changhua

(*Institute of Microelectronics, Peking University, Beijing 100871, China*)

Abstract: Gate current for pMOSFETs is composed of direct tunneling current, channel hot hole, electron injection current, and highly energetic hot holes by secondary impact ionization. The device degradation under $V_g = V_d/2$ is mainly caused by the injection of hot electrons by primary impact ionization and hot holes by secondary impact ionization, and the device lifetime is assumed to be inversely proportional to the hot holes, which is able to surmount Si-SiO_2 barrier and be injected into the gate oxide. A new lifetime prediction model is proposed on the basis and validated to agree well with the experiment.

Key words: hot carriers; recombination; electron injection; secondary impact ionization

EEACC: 0170N; 2560R

CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2004)02-0152-06

1 Introduction

Hot carrier degradation has been recognized as a major reliability and performance concern in today's submicron complementary metal oxide semiconductor (CMOS) field effect transistor (FET) technology[1~4]. Although the nMOSFETs have been extensively investigated, the hot carriers in pMOSFETs have received relatively less attention due to their historically low impact to the reliability of conventional CMOS circuits. As the CMOS technology enters the submicron and deep-submicron regions, the degradation caused by the pMOSFETs has become comparable with that of the nMOSFETs. Then it is very important to investigate the behavior and underlying physics of pMOSFETs hot carrier degradation mechanism[1].

The physical mechanism responsible for the gate current increase is a chain of impact ionization events leading to carrier pair generation deep inside the MOS depletion region[2~4]. The high electric field is responsible for the heating of electrons created by primary impact ionization at the drain edge. Next, these hot electrons ionize deep in the substrate by the acceleration of high lateral and vertical electric filed and generate secondary holes (h3), which flow toward the Si-SiO_2 interface. It has been demonstrated that the high energies of the h3 are at the origin of interface states creation

* Project supported by State Key Development Program of Basic Research of China (No. G2000036503) and by Motorola Digital DNA Laboratory

Hu Jing male, was born in 1976, PhD candidate. His research interests include small-scaled MOS devices and reliability, device modeling and characterization, and hot-carrier effects.

Zhao Yao male, was born in 1980, PhD candidate. His research interests include small-scaled MOS devices and reliability, device modeling and characterization, and hot-carrier effects.

Xu Mingzhen female, was born in 1939, professor. Her research interests include the electrical characterization and reliability project of MOSFET's with ultrathin gate dielectric, and reliability project of MOSFET's, high field physics of thin gate oxide and breakdown mechanism and modeling.

Received 23 May 2003, revised manuscript received 22 August 2003 ©2004 The Chinese Institute of Electronics

and of electric parameters degradation in pMOSFETs[3,4]. The influence of the secondary impact ionization on the hot hole degradation is believed to be enhanced for scaled down devices[4,5].

Drain avalanche hot carrier degradation occurring around a maximum substrate condition (about $V_g = V_d/2$) is serious in pMOSFETs, where interface state generation reduces the drain current[2]. In addition, the mode is projected to be the worst-case stress bias condition for pMOSFETs in deep submicron technologies[3]. A simple and physical lifetime prediction model in good agreement with the data is needed both for reliability evaluation of fabrication processes and for circuit level reliability simulation.

A simple relationship to describe the substrate current as a function of effective channel length is developed as a function of drain voltage and effective channel length[6]. The relation is then put into the lifetime prediction model and the device lifetime has a power law relationship with effective length. However, the relationship of substrate current and drain voltage has not been widely accepted in the model and the power law relationship with channel length is overestimated in comparison with other models[7,8].

In this paper, the gate components are analyzed and the device degradation under $V_g = V_d/2$ stress mode is discussed. A new lifetime prediction model is proposed on the basis. The commonly accepted substrate current equation[4] is then put into the new lifetime prediction model including explicitly the channel length and applied voltage dependencies.

2 Model

Because gate current, I_g, is a sensitive measure of the high energy tail of the hot carrier distribution function, understanding their origin is essential for understanding the hot carrier effects in MOSFETs. To this end, the gate current of pMOSFETs will be investigated in theory. The device degradation mechanism will be analyzed accordingly.

Figure 1 shows the gate current mechanism for pMOSFETs. Electrons at the poly-gate can be accelerated by high electric field between gate and substrate and then injected into the oxide with the assistance of tunneling (Mechanism (i)). Direct tunneling itself does not cause charge trapping in the gate oxide[8]. If the stress voltage is comparatively high, the channel holes can gain sufficient energy from channel acceleration to surmount Si-SiO_2 barrier with the help of tunneling to overcome an unfavorable gate to drain potential difference and be injected into the gate oxide to form gate current (Mechanism (ii))[9]. In the case of extremely short channel devices with ultra-thin gate oxides, more holes are enough to become highly energetic. Carriers can only contribute to gate current if their energies are above the effective Si/SiO_2. Clearly, in this case, channel carriers cannot contribute a finite gate current for pMOSFETs.

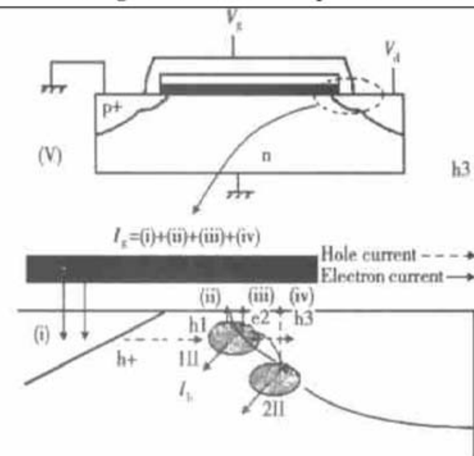

Fig. 1 Gate current mechanism for pMOSFETs
(i) electron tunneling from gate to substrate by direct tunneling, (ii) channel hot hole injection, (iii) electron injection by primary impact ionization, and (iv) hole injection by secondary impact ionization

In the region of the channel close to the drain of a device biased into the saturation region, the gate potential (relative to the channel) appears positive for a pMOSFET and the internal electric field distributions then favor electron injection the gate oxide[10,11]. The gate current of pMOSFETs

results from electrons(e2) rather than hole injection into the oxide because electrons have a longer mean free path[10] (Mechanism (iii)). Also, the Si-SiO_2 barrier height is lower for electrons and the vertical field at a low gate voltage favors electron injection[12]. Even under a low stress voltage, the component still exists. For the gate current under a high drain voltage it always lies below that under low drain voltage in Fig. 3. The existence of electron current has been widely accepted and demonstrated to be related to the device degradation[4] of pMOSFETs.

The secondary holes(h2) leaves through the drain while the secondary electrons (e2) diffuse through the drain to the junction between substrate and drain. The generated energetic electrons by primary impact ionization are accelerated by the electric field between substrate and drain and ionize deep in the substrate and generate secondary pairs of electron-holes. The hot holes by secondary impact ionization (h3) will fall back through the potential drop of drain-substrate junction and are injected into the drain where they can diffuse to the oxide surface[12,13]. The hot holes can also fall through the vertical potential drop beneath the channel to the oxide interface just to the left of the drain. It has been demonstrated that the high energies of hole current by the secondary impact ionization are at the origin of interface states creation and of electrical parameter degradation in MOS transistors[2~5,12,13]. The generated holes will flow toward the Si-SiO_2 interface by the acceleration of lateral and vertical electric field and be injected into the gate oxide, which will form positive gate current (Process (iv)).

With the decrease of device dimensions and corresponding decrease of the drain voltage ($|V_d|$), channel electric field acceleration is unable to provide enough energy for holes to be injected into the gate oxide. However, the primary impact ionization under low stress voltages still exists and results in high energetic holes by secondary impact ionization. The mechanisms (iii) and (iv) will become dominant in the components of gate current with the decreasing dimensions and corresponding decrease of stress voltage.

$V_g = V_d/2$ stress mode basically corresponds to the maximum impact ionization rate and the number of energetic electrons is maximum[6]. Generally, the injected amount of hot holes and hot electrons is not equal under $V_g = V_d/2$ stress mode. The amount of injected holes by secondary is generally smaller than that of injected electrons for two reasons. First, the Si-SiO_2 barrier for holes is much larger than that of electrons[11]. In addition, tertiary holes are generated by secondary electrons. So the device degradation should be decided by the holes for the efficiency for creating interface traps per electron is much smaller than per recombination event[2]. Furthermore, hole trapping efficiency and electron capture cross section of trapped holes are very high[2].

The proposed model assumes that the device lifetime is inversely proportional to the amount of holes by secondary impact ionization that can be able to surmount Si-SiO_2 barrier. The device lifetime can be written as

$$\frac{1}{\tau} \propto I_{gh3}/W \tag{1}$$

where I_{gh3} is the hot holes by secondary impact ionization, which is able to surmount Si-SiO_2 barrier and be injected into the gate oxide. W represents channel width.

$$I_{gh3} \propto I_b(E_{/\!/})[M_n(E_\perp) - 1]T_B(E_\perp) \tag{2}$$

$$I_b \propto I_d \exp(-\Phi_i/q\lambda_h E_m) \tag{3}$$

$$E_m = \frac{V_d - V_{dsat}}{l_d} \tag{4}$$

where I_b is the substrate current, E_m is the maximum channel electric field; I_{gh3} is decided by the secondary electron multiplication coefficient (M_n) and the fraction of tertiary holes injected back to the gate(T_B), which is proportional to I_b at certain bias. These two parameters are mostly sensitive to the vertical field ($E_\perp$) in proximity of the drain junction. E_m is the maximum channel electric field; I_d is drain current, V_{dsat} is pinch-off point potential

and l_d is characteristic length of velocity saturation region, and V_d is drain voltage. V_{dsat} can be determined by experiment[13].

Holes by secondary impact ionization are generated by secondary electrons. The maximum electric field between the drain and substrate junction can be approximately expressed as $\sqrt{\frac{2qN_A}{\epsilon_{Si}}(V_d+V_{bi})}$ for a specific value of the substrate doping concentration N_A near the junction in the full depletion approximation. V_{bi} is junction built-in potential between substrate and drain. q represents the electron charge and ϵ_{Si} is the dielectric permittivity of silicon.

Based on lucky electron model[4], M_n can be expressed as

$$M_n - 1 \propto \exp\left(-\frac{\Phi_i}{q\lambda_e\sqrt{\frac{2qN_A}{\epsilon_{Si}}(V_d+V_{bi})}}\right) \quad (5)$$

where λ_e = 9.2nm is the electron free paths[2] and Φ_i = 1.3eV[4] is the critical energy for impact ionization.

The holes, h3, which come back through DBJ (drain-substrate junction) into the drain, dominate the high energy DF (distribution function) and can lead to significant gate current. This occurs for two reasons. First, the high field DBJ potential drop, which includes the junction built-in potential, is larger than channel potential drop V_{CH}. For reasonable junction dopings, the field in the DBJ will be high enough for significant feedback. Second, each successive II generate secondaries with non-zero energy. Therefore, the holes reaching the drain have energies greater than the DBJ potential drop[13]. So T_B can be written as

$$T_B \propto \exp\left(-\frac{\Phi_h}{q\lambda_n\sqrt{\frac{2qN_A}{\epsilon_{Si}}(V_d+V_{bi})}}\right) \quad (6)$$

where λ_h = 4.3nm is hole free paths[2] and Φ_h = 4.5eV[2] is the critical hole energy for creating damage. $\exp\left(-\frac{\Phi_h}{q\lambda_h\sqrt{\frac{2qN_A}{\epsilon_{Si}}(V_d+V_{bi})}}\right)$ of Eq.(6) is the rate of supply of hot holes by secondary possessing energies greater than Φ_h.

Take Eqs.(5) and (6) into Eq.(1), the lifetime model can be expressed as

$$\ln(\tau I_d/W) \propto \left(\frac{\Phi_i l_d}{q\lambda_h}\right)\left(\frac{1}{V_d - V_{dsat}} + \left(\frac{\lambda_h}{\lambda_e} + \frac{\Phi_h}{\Phi_i}\right)\frac{1}{k\sqrt{(V_d+V_{bi})}}\right) \quad (7)$$

$$k = l_d \times \sqrt{\frac{2qN_A}{\epsilon_{Si}}} = 2l_d/\sqrt{2\epsilon_{Si}/qN_A} \quad (8)$$

l_d can be derived from the unified relationship of I_b/I_d vs $V_d - V_{dsat}$ and then k can be extracted. Plotting τI_d versus $\left(\frac{1}{V_d - V_{dsat}} + \left(\frac{\lambda_h}{\lambda_e} + \frac{\Phi_h}{\Phi_i}\right) \times \frac{1}{k\sqrt{(V_d+V_{bi})}}\right)$, $\frac{\Phi_i l_d}{q\lambda_h}$ can be derived, which should be identical to the values extracted from Eq.(2).

3 Experiment

The pMOSFETs with 2.5nm gate oxide used for the study had 0.165, 0.15, and 0.135μm effective channel length and 10 and 0.3μm channel width, which contain a shallow source/drain extension junction and a counter-doped halo to suppress short channel effects. The devices were stressed at various drain voltage under $V_g = V_d/2$ stress mode. The degradation of saturated current dI_{dsat} (= $(I_{dsat} - I_{dsat}(0)/I_{dsat}(0))$) was monitored for evaluating the hot carrier lifetime and 10% dI_{dsat} is taken as the device lifetime. The thickness of oxide was measured by high-frequency C-V method. All the devices were fabricated through the same standard CMOS processes. The stresses and normal I-V measurements were performed by means of precision semiconductor parameter analyzer HP4156B. All experiments were done at room temperature, i.e. 300K, and all the instruments were controlled by a PC using GPIB interface.

4 Model validation

To verify the model, $\frac{\Phi_i l_d}{q\lambda_h}$ extracted by Eq.(2)

can be effectively used to fit Eq. (7). Figure 2 shows the relationship of impact ionization rate I_b/I_d versus $1/(V_d - V_{dsat})$. A straight line is obtained under different bias conditions and device dimen-

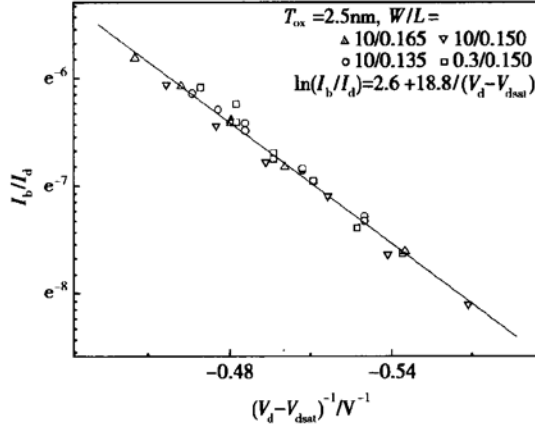

Fig. 2 Relationship of the ratio of I_b/I_d versus $1/(V_d - V_{dsat})$

sions. V_{dsat} is extracted from the experiments[14]. For pMOSFETs with different gate oxide, the relationship of I_b/I_d versus $1/(V_d - V_{dsat})$ can be written as

$$\ln(I_b/I_d) = -2.6 + 18.8/(V_d - V_{dsat}) \quad (9)$$

l_d can be calculated from Eq. (10) for pMOSFETs with 2.5nm gate oxide:

$$l_d = 18.8/(\Phi_i/q\lambda_h) = 18.8/(3.7 \times 10^6) = 5.7 \times 10^{-6}\text{cm} \quad (10)$$

For our samples, the doping concentration of substrate is about 10^{-17}cm^{-3} for pMOSFETs. So k can be calculated:

$$k = 2l_d/\sqrt{2\epsilon_{Si}/qN_A} \approx 1.1$$

Data have been plotted τI_d vs $\frac{1}{V_d - V_{dsat}} + (\frac{\lambda_h + \Phi_h}{\lambda_e + \Phi_i})\frac{1}{k\sqrt{(V_d + V_{bi})}}$ in Fig. 3 for pMOSFETs with different channel length and width. Very good agreement is found between the model and the experimental data, and the results indicate that the present model can accurately predict the lifetimes of MOS devices beyond those being measured.

5 Conclusion

Gate current for PMOSFETs is composed of

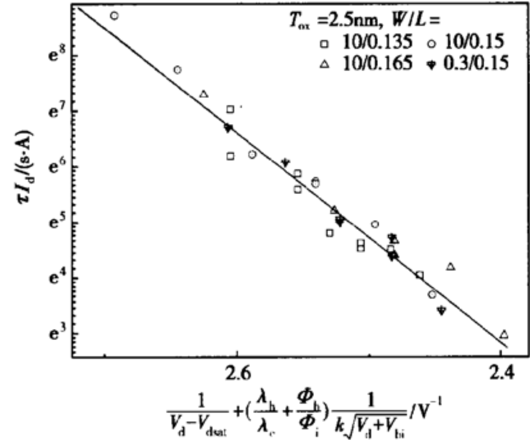

Fig. 3 τI_d vs $\frac{1}{V_d - V_{dsat}} + (\frac{\lambda_h + \Phi_h}{\lambda_e + \Phi_i})\frac{1}{k\sqrt{(V_d + V_{bi})}}$ for pMOSFETs with different channel length and width under $V_g = V_d/2$ stress mode.

four parts, which are direct tunneling current, channel hot hole, electron injection current, and highly energetic hot holes by secondary impact ionization. The device degradation under $V_g = V_d/2$ stress mode is caused by the recombination of electrons and hot holes by secondary impact ionization, and the device lifetime is assumed to be inversely proportional to the amount of holes by secondary. A new lifetime prediction model τI_d versus $\frac{1}{V_d - V_{dsat}} + (\frac{\lambda_h}{\lambda_e} + \frac{\Phi_h}{\Phi_i})\frac{1}{k\sqrt{(V_d + V_{bi})}}$ has been proposed on the basis and validated to agree well with the theory. This model is extremely useful in the estimate of the MOS applied voltage range needed for ensuring a long device lifetime with the presence of hot-carrier induced degradation.

References

[1] Yang Z J, Guarin F J, Rauch S E. The interaction of hot electrons and hot holes on the degradation of p-channel metal oxide semiconductor field effect transistors. IEEE International Caracas Conferences on Devices, Circuits and Systems, 2002: 17

[2] Koike N, Tatsuunma K. A drain avalance hot carrier lifetime mode for n- and p-channel MOSFET's. IEEE International Reliabilty Physics Symposium, 2002: 86

[3] Li E, Rosenbaum E, Tao J, et al. Projecting lifetime of deep

submicron MOSFETs. IEEE Trans Electron Devices, 2001, 48: 671

[4] Hu C, Tam S C, Hsu F C, et al. Hot-electron induced MOSFET degradation-model, monitior and improvement. IEEE Trans Electron Devices, 1985, 32: 375

[5] Doyle B S, Mistry K D. A lifetime prediction for hot-carrier degradation in surface-channel p-MOS devices. IEEE Trans Electron Devices, 1990, 37: 1301

[6] Wong W, Ice A, Liou J J. An empirical model for the characterization of hot-carrier induced MOS device degradation. Solid State Electron, 1997: 173

[7] Weber W, Thewes R. Hot-carrier-related device reliability for digital and analogue CMOS circuits. Semicond Sci Technol, 1995, 10: 1432

[8] Thewes R, Bredelow R, Schlunder C, et al. Device reliability in analog CMOS applications. IEEE International Electron Device Meeting, 1998: 81

[9] Min B W, Zia O, Celik M, et al. Hot carrier enhanced gate current and its impact on short channel nMOSFET reliabilty with ultra-thin gate oxides. IEEE International Electron Device Meeting, 2001: 873

[10] Brassington M P, Razouk R R. The relationship between gate bias and hot-carrier-induced instabilities in buried- and surface-channel PMOSFET′s. IEEE Trans Electron Device, 1988, 35: 320

[11] Ong T C, Ko P K, Hu C. Hot-carrier current and device degradation in surface-channel pMOSFE′s. IEEE Trans Electron Device, 1990, 37: 1658

[12] Driussi F, Esseni D, Selmi L, et al. Hot hole gate current in surface channel PMOSFETs. IEEE Electron Device Lett, 2001, 22: 29

[13] Bude J D. Gate current by impact ionization feedback in submicron MOSFET technologies. Symposium on VLST Technology Digest of Technical Paper, 1995: 101

[14] Chan T Y, Ko P K, Hu C. Dependence of channel electric field on device scaling. IEEE Electron Device Lett, 1985, 6: 551

在 $V_g = V_d/2$ 应力模式下 2.5nm 氧化层 pMOSFETs 的新寿命预测模型*

胡 靖 赵 要 许铭真 谭长华

(北京大学微电子学研究所, 北京 100871)

摘要: 研究了 2.5nm 超薄栅短沟 pMOSFETs 在 $V_g = V_d/2$ 应力模式下的热载流子退化机制及寿命预测模型. 栅电流由四部分组成: 直接隧穿电流、沟道热空穴、一次碰撞电离产生的电子注入、二次碰撞电离产生的空穴注入. 器件退化主要是由一次碰撞产生的电子和二次碰撞产生的空穴复合引起. 假设器件寿命反比于能够越过 Si-SiO_2 界面势垒的二次碰撞产生的二次空穴数目, 在此基础上提出了一个新的模型并在实验中得到验证.

关键词: 热载流子; 复合; 电子注入; 二次碰撞电离

EEACC: 0170N; 2560R

中图分类号: TN386 **文献标识码**: A **文章编号**: 0253-4177(2004)02-0152-06

* 国家重点基础研究发展计划(No. G2000036503)及 Motorola Digital DNA Laboratory 资助项目

胡 靖 男, 1976 年出生, 博士研究生, 从事小尺寸器件的可靠性研究.

赵 要 男, 1980 年出生, 博士研究生, 从事小尺寸器件的可靠性研究.

许铭真 女, 1939 年出生, 教授, 从事小尺寸器件的特性和物理以及半导体材料的可靠性研究.

2003-05-23 收到, 2003-08-22 定稿

©2004 中国电子学会