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Novel General-Purpose Sense Amplifier-Based Flip-Flop and Its Further Speed Improvement by Pseudo-PMOS Dynamic Technique*

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Abstract: A novel general-purpose sense amplifier-based flip-flop is proposed. Compared to other flip-flops, the proposed flip-flop has faster operating speed under the approximately same power consumption, and needs fewer transistors and consumes smaller area. Moreover, it eliminates the glitch problem. By using pseudo-PMOS dynamic technique, its performance is further improved.

Key words: flip-flop; pseudo-PMOS; dynamic technique
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1 Introduction

Many kinds of flip-flop circuit are proposed in the References[1~6]. Among them, sense amplifier-based flip-flops draw much attention. In References[1~5], five kinds of sense amplifier-based flip-flop were presented. The comparison of their performance was done in Reference[5].

In this paper, a new kind of sense amplifier-based flip-flop is proposed. Its performance is compared to the best performance of flip-flop in Reference[5]. The results show that the newly proposed flip-flop has faster operating speed under the approximately same power consumption, and it needs fewer transistors and consumes smaller area. Moreover, the proposed flip-flop eliminates the glitch problem existing in other kinds of flip-flop and could be used as a general-purpose flip-flop. By using pseudo-PMOS dynamic technique, its speed is further improved, the power and the chip area is further reduced.

2 Circuit implementation

Figure 1 shows the schematic diagram of the proposed general-purpose flip-flop. It consists of a modified sense amplifier at the first (input) stage and modified N-C^{2}MOS latches at the second (output) stage. The cross-coupled pairs (M5~M8) are in parallel with the differential pair (M1~M2). Compared to the conventional sense amplifier, the proposed circuit will improve the speed and sensitivity of the sense amplifier. The circuit also benefits from the body effect of NMOS transistors M1~M2 and M7~M8. Their bulk nodes are connected to ground. When the clock signal CK is 0, the source node, COM, of M1~M2 and M7~M8 is

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pre-charged along with nodes S, R. Source-to-bulk bias voltages will appear. These bias voltages will increase the threshold voltages of these transistors. This will decrease the voltage level and reduce the charge storage in node COM when M1~ M2

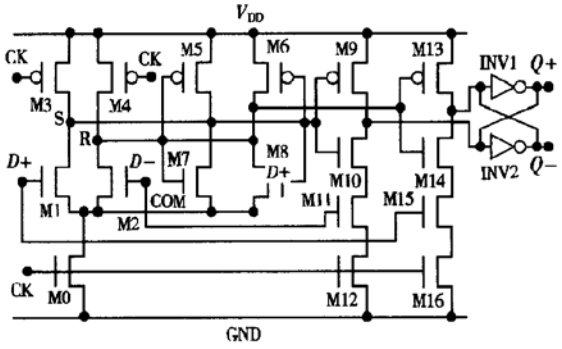

Fig. 1 Schematic diagram of proposed flip-flop

and M7~ M8 are turned off. So the transition speed of the sense amplifier will be improved at the rise edge of the clock signal CK. The clock-controlled transistors next to output nodes in the standard N-C^{2}MOS latches are placed immediately next to the ground. This will improve the speed, since floating transistors present less load[7], and more load transistors can be made floating by exchanging of position of the clock-controlled transistors. One more NMOS transistor M11 (M15) is added to N-C^{2}MOS latch. Its role is to avoid the glitch. If this transistor is omitted, the glitch problem might appear. The sequence of logic transitions that leads to the glitch is listed in the following statements. If $Q+$ and $D+$ are logic 1 and $Q-$ and $D-$ are logic 0 for CK= 0, the nodes, S and R, are pre-charged to logic 1 and $Q+$ ($Q-$) remains constant. During evaluation phase, CK= 1, which turns off M3~ M4 and turns on M12 (M16) and M0. Node S cannot be discharged instantly to logic low by the sense amplifier and remains high for a short time, which can be long enough to cause $Q+$ to discharge. Node S will eventually become lower than the threshold of the inverter formed by M9 and M10, causing $Q+$ to move up again to the correct output of logic 1. Depending on the transistor dimensions, the hazardous glitch can become very serious. If the transistor M11 is added, $Q+$ could not be discharged at the rise edge of CK since the transistor M11 controlled by $D-$ (which is logic 0) is turned off. So the glitch problem is eliminated. The cross-coupled inverters INV1~ INV2 shorten the transition time of the output nodes ($Q+$, $Q-$) during the evaluation phase. They prevent the output nodes ($Q+$, $Q-$) from being dynamic nodes and hold the output values until the next rise edge of CK during the pre-charge phase. They are all made up of minimum size transistors, so the additional capacitive loads to the output nodes due to the cross-coupled inverters are negligible.

The principle of the proposed flip-flop is described as follows. When the clock signal CK is logic 0, the nodes S~ R are pre-charged to logic 1. If $D+$ is logic 1 at the rise edge of CK, S changes from logic 1 to logic 0 while R remains logic 1. Thus, $Q+$ is pulled up to logic 1 and $Q-$ is pulled down to logic 0. Conversely, if $D+$ is logic 0 at the rise edge of CK, the similar operation happens. While CK remains logic 0, S and R are pre-charged to logic 1, M9~ M12 and M13~ M16 are turned off, so $Q+$ and $Q-$ are all kept latched.

To further improve the speed of the proposed flip-flop, pseudo-PMOS dynamic technique is used. The schematic diagram of the improved high-speed flip-flop is shown in Fig. 2. The output latch is a modified pseudo-PMOS inverter. The load of the

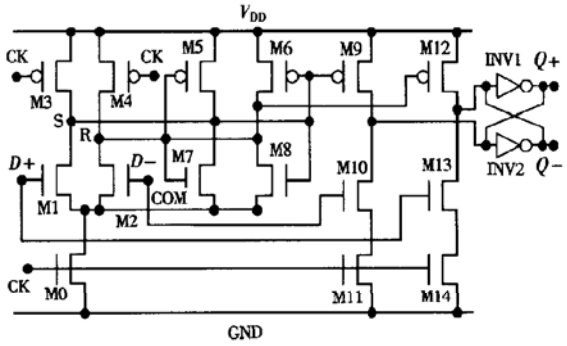

Fig. 2 Schematic diagram of improved high-speed flip-flop

sense amplifier is lowered, so the speed could be improved. M10 (M13) is added to turn off the dis-

charge path when $Q+$ ($Q-$) changes from logic 0 to logic 1. Although the output logic 1 decreases from V_{DD}, and a static current path exists if the input data changes in the evaluation phase (CK= 1), the proper logic operation could be ensured by carefully selecting the dimensions of the transistors. Moreover, in the high-speed applications, due to the continuous switching at high frequencies, the dynamic power dissipation dominates and the added static power dissipation is not significant. So the improved high-speed flip-flop is very attractive for RF (radio frequency) applications.

3 Comparison of performances and discussion

To compare the proposed flip-flops with Kim's[5], HSPICE simulations using BSIM3.1 (Level 49) transistor models for a standard digital process —0.25μm logic 2.5V process were done for the flip-flops under the same condition. The power supply voltage we used is 2.5V and the load capacitances at the output nodes are 0.1pF. Table 1 shows the comparison of the performances of the flips-flops. The clock-to-output delays are the time that the outputs rise up to 2.0V and the outputs fall down to 0.5V after CK becomes logic 1. The speed-up factor is calculated from the worst-case of clock-to-output delay time, which is the larger value of 1→0 and 0→1 transition times. The power consumption, the power-delay product (PDP) and the normalized PDP (NPDP) are measured when the clock frequency is 500MHz and the input data frequency is 250MHz. With respect to the Kim's flip-flop, the proposed flip-flop has a speed-up factor of 1.10. Its power consumption is approximately the same as Kim's, and its PDP is reduced by 8%. The improved high-speed flip-flop has a speed-up factor of 29%. Its power consumption and PDP are reduced by 17% and 35% respectively. The proposed flip-flop needs 21 MOS transistors and the improved high-speed flip-flop only needs 19 transistors while the Kim's needs 24 ones. According to Reference[5], the Kim's flip-flop has the best performance among the flip-flops in References[1~5], now our proposed flip-flop and the improved high-speed flip-flop are better than kim's.

Table 1　Comparison of performances of three kinds of flip-flop's

	Clock-to-output delay/ps			power /μW	PDP /fJ	NPDP
	0→1	1→0	Speed-up			
Kim's FF	243	228	1.00(243)	862	209	1.00
Proposed FF	222	217	1.10(222)	867	192	0.92
Improved FF	186	189	1.29(189)	713	135	0.65

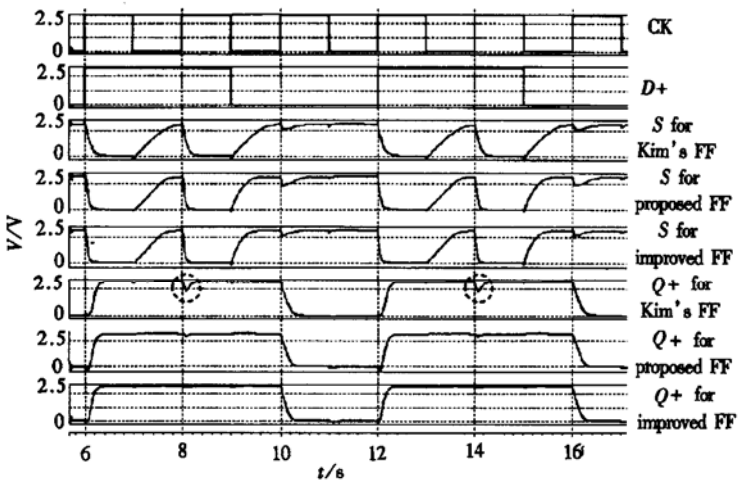

Fig. 3　Transient simulation waveforms

Figure 3 shows the transient simulation waveforms for three kinds of flip-flop when the clock frequency is 500MHz and the input data frequency is one-third clock frequency. From the figure, it could be seen that the Kim's flip-flop produces the glitches (which could result in serious logic error in general applications) while the proposed flip-flop and the improved high-speed flip-flop are all glitch-free at the expense of the increase of capacitance at input nodes.

4 Conclusions

This paper presents a new kind of sense amplifier-based flip-flop and its further speed improvement. The results show that the new proposed flip-flops have faster operating speed under the approximately same power consumption compared to Reference[5], and it needs fewer transistors and consumes smaller area. Moreover, the proposed flip-flop eliminates the glitch problem existing in other kinds of flip-flop and could be used as a general-purpose flip-flop.

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一种基于灵敏放大器的新型触发器及其通过伪 PMOS 动态技术的速度改进*

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摘要: 提出了一种基于灵敏放大器的新型触发器. 和其它触发器相比, 该触发器在近似相等的功耗下能以更快的速度工作, 并且其所需要的 MOS 管少, 芯片占用的面积也少. 这种触发器消除了"假信号"问题, 通过使用伪 PMOS 动态技术, 它的速度可以得到进一步的提高.

关键词: 触发器; 伪 PMOS; 动态技术

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