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# A 1.25Gb/s InP-Based Vertical Monolithic Integration of an MQW Laser Diode and an HBT Driver with a Lateral Buffer Mesa Structure*

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**Abstract**: A novel fabrication process related to a smoothly wet chemical etching profile of InP-based epitaxial layers in the crystal direction of [01$\bar{1}$] for an InP-based monolithic vertically integrated transmitter with an MQW laser diode and a heterojunction bipolar transistors driver circuit is described. A clear eye output diagram via an O/E converter is demonstrated under a 1.25Gb/s non-return-zero pseudorandom code with a pattern length of $2^{23}-1$. The integrated transmitter has a power dissipation of about 120mW with an optical output of 2dBm.

**Key words**: integrated optoelectronics; optoelectronic integrated circuits; transmitter
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## 1 Introduction

InP-based monolithic opto-electronic integrated circuits (OEICs), such as metal-semiconductor-metal (MSM) photodetector integrated with high electronic mobility transistors (HEMTs) or PIN photodetector with heterojunction bipolar transistors (HBTs) and laser diode (LD) with HBTs or HEMTs, are most desirable OEICs for the front-ends of lightwave receiver and transmitter. Unlike the rapid progress made in the field of receiver OEICs which have reached such a high bit rate for more than 40Gb/s[1,2], the research results of transmitter OEICs still remain in lower Gigabits[3]. One of the most important reasons is that the DFB or MQW laser is not so much compatible with HBTs and HEMTs for transmitter OEICs in either epitaxial structure or fabricating process as the MSM or PIN photodetector with electronic circuits of HEMTs or HBTs for receiver ones. As a vertically integrated transmitter, the simple stack of the layers of optical and electronic devices resulted in higher mesas on the topography of the chip, which makes too difficult or complicated for making a good connection between mesas at different layers of the device fabrication. In this paper, we present an improved fabrication process related to a novel buffer mesa structure for a vertical monolithically integrated transmitter with a 1.55μm MQW laser and an InP/InGaAs HBT driver circuit on a semi-insulating Fe-doped (100) InP

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substrate. The mentioned disadvantage of the fabrication of vertically integrated transmitter could be greatly avoided in the process that we present.

## 2 Epitaxial structure and circuit schematic

The epitaxial structure for the OEIC wafer is shown in Table 1. It was grown by a low pressure metal organic chemistry deposit system on a substrate of commercial 50mm semi-insulating Fe-doped (100) InP. The structure consists of a nearly conventional structure of InP/InGaAs HBT and that of an InGaAsP MQW laser diode (LD), between which is an undoped 100-nm-thick buffer layer of InP. The buffer layer here acts as an insulating layer between the $N^+$-sub-collector of HBT and the $P^+$-contact layer of LD as well as an etch-stop layer.

Table 1 Epitaxial structure of the integrated transmitter

| Layer | Material | Doping /$cm^{-3}$ | Thickness /nm |
|---|---|---|---|
| HBT | $n^+$ InGaAs | $5\times10^{18}$ | 100 |
| | $n^+$-InP | $1\times10^{19}$ | 70 |
| | n-InP | $5\times10^{17}$ | 100 |
| | i-InGaAs | i | 10 |
| | $p^+$-InGaAs | $1\times10^{19}$ | 120 |
| | $n^-$-InGaAs | $2\times10^{16}$ | 450 |
| | $n^+$ InGaAs | $5\times10^{18}$ | 500 |
| Buffer | InP | i | 100 |
| LD | $p^+$-InGaAs | $5\times10^{18}$ | 500 |
| | p-InP | $2\times10^{17}$ | 1700 |
| | MQW | i | 300 |
| | n-InP | $2\times10^{17}$ | 1700 |
| | $n^+$ InGaAs | $2\times10^{19}$ | 500 |
| Substrate | (100) SI-InP | | |

Figure 1 is the schematic of the transmitter circuit. The circuit includes a laser diode (LD) and a driver circuit which consists of 4 HBTs. $Q_1$ and $Q_2$ make up an emitter coupled differential pair switch and $Q_3$ is designed to set the peak modulating current. The DC operating point of LD is provided by $Q_4$ with a off-chip inductor between the cathode of LD and the collector of $Q_4$.

Limited by our process, a simple single-base structure for HBT was used. The contact area of the emitter with base of $Q_1$ was $6\mu m\times15\mu m$ with the distance between emitter and base contacts of $3\mu m$. So was $Q_2$ and $Q_3$. But for $Q_4$, it was $6\mu m\times20\mu m$ with the same distance between emitter and base contacts.

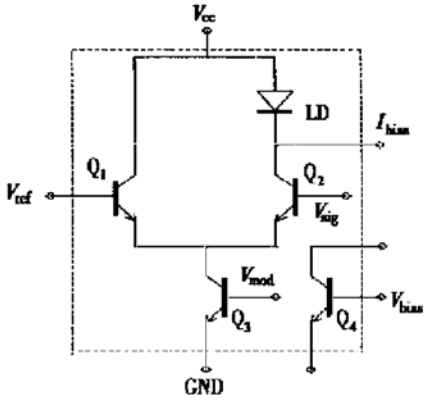


Fig. 1 Schematic circuit of the integrated transmitter

## 3 Device structure and fabrication process

Figure 2 shows the profile diagram of the improved vertical integration of LD and HBT. The single-base structure of HBT is just similar to that employed in our previously reported $n^+$-substrate transmitter OEICs[4] except the difference with the thickness and contact metal for the base region. The base contact was self-aligned to the emitter mesa by the under-cut chemical wet etching process with photoresist mask. The ridge waveguide of the LD is formed by a double-groove process which self-aligned to the 3-$\mu$m-width anode contact strip. An in-house $SiO_2$-assisted lift-off metalization process[5] was used for the fabrication of ohmic contact of HBT and LD, and the contact of the LD and that of the emitter and collector of HBT was evaporated with Ti/Pt/Au (40nm/40nm/100nm). $H_3PO_4$ : $H_2O_2$ : $H_2O$ solution and HCl; $H_2O$ acted as selective wet chemical etchant for InGaAs and InP respectively, while HBr : $HNO_3$ : $H_2O$ as unselective one for InGaAs, InP and InGaAsP epitaxial layers.

Polyimide was spinned as planarization of the chip surface, and 2-μm-thick Au was electro-plated as the interconnection.

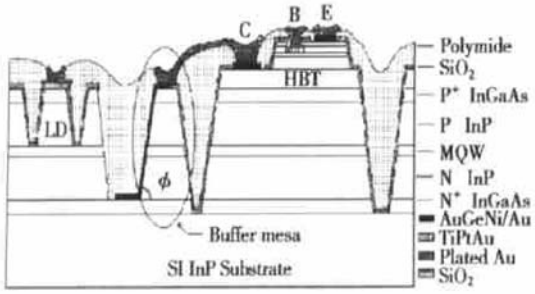


Fig. 2 Profile diagram of the vertical integration of LD and HBT

As illustrated in Fig. 1, the cathode of LD was connected with the collector contact of $Q_2$, which is usually achieved by electrical plate through a hole via polyimide. Connection with a hole that is nearly 4~ 5μm in depth by electrical plating is very difficult for the side-wall of the hole which is nearly vertical. To avoid this disadvantage, we developed an improved process related to a relatively smoothly wet chemical etching profile of InP-based epitaxial layers in the crystal direction of $[01\bar{1}]$. Figure 3 is the etching profile of the epitaxial layers under scan electronic microscope (SEM), from which we can see that the slope $\Phi$ of the sidewall is as small as about 30°. Depending on this advantage, we arranged a mesa as a lateral buffer in the same height of the anode contact of LD between the cathode of

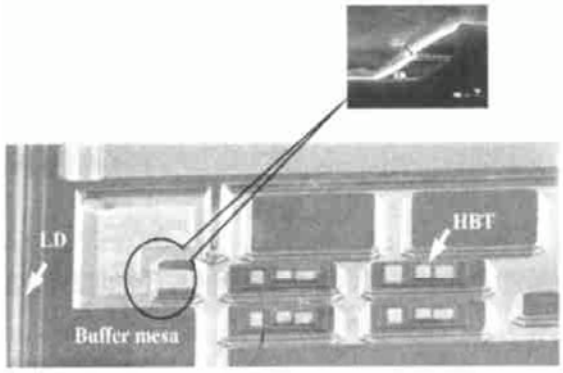


Fig. 3 SEM photograph of the integrated transmitter chip before planarization and interconnection Inset: photograph of the buffer mesa with a smooth chemical wet etching profile in the crystal direction of $[01\bar{1}]$

LD and the collector of $Q_2$. When the contacted metal of the cathode was deposited, the lower contacted metal for LD cathode was extended up to the surface of the buffer mesa along the smooth sidewall automatically. As a result, the vertical electrical connection between the cathode and the collector was shortened dramatically to almost only 1μm. Not only the electrical connection was shortened from 5μm to 1μm, but also it became much easier and more reliable.

The wafer was thinned to about 100μm by both of mechanical grinding and chemical wet etching following with metalization on the backside. The dies on chip were cleaved into about 970μm × 350μm and the length of cavity with the cleaved facets for LD was 350μm.

## 4 Experiment result

The current-voltage ($I$-$V$) characteristics of a typical HBT on the chip reveals that HBT can provide a current gain of about 50 with a current of 40mA. The unity current gain cutoff frequency ($f_t$) of a typical HBT is 11GHz resulted from an un-optimized simple base structure in lateral layout and vertical epitaxial structure. The average threshold current $I_{thav}$ for the integrated LD without antireflective film at a pulsed operation is as low as about 10mA, while the threshold current $I_{th}$ at continuously operation is about 20~ 25mA. Figure 4 is the spectrum plot of emission intensity versus wavelength and pulsed output power versus average current (inset) for the integrated LD.

We demonstrated a current modulation experiment with a packaged transmitter chip, which was bonded on a copper heat sink. The integrated transmitter was operated under a NRZ (nonreturn-to-zero) pseudorandom pulsed data with a pattern length of $2^{23}-1$, which were generated by a HP7084A Pattern Generator. A 1.5Gb/s O/E converter was employed to detect the light output of laser via a lensed single mode fiber, and then change it into the electronic signal, which was ob-

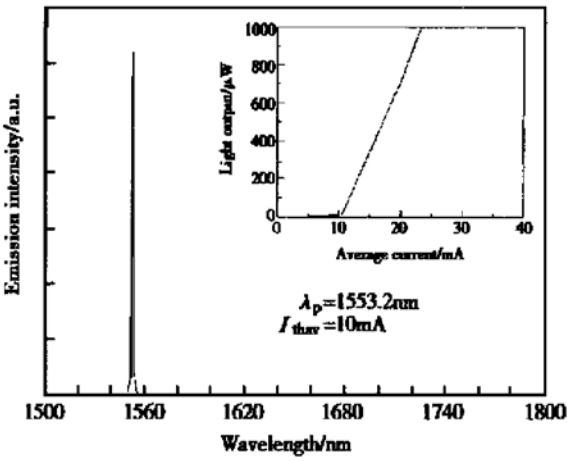


Fig. 4 Spectrum plot characteristics of an integrated LD Inset: pulsed output power versus average current

served by a HP54120B digitizing oscilloscope. Figure 5 is the output eye diagram at 1.25Gb/s of the integrated transmitter.

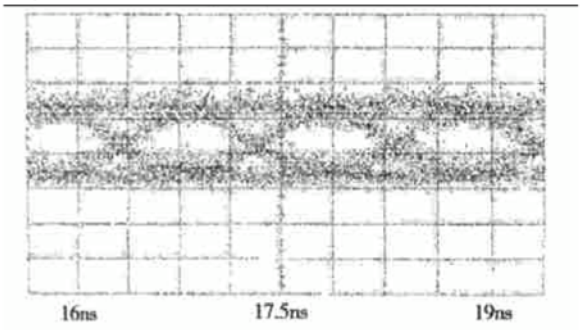


Fig. 5 Output eye diagram operated under 1.25Gb/s NRZ code for the integrated transmitter (300ps/div, 100mV/div)

## 5 Conclusion

We have developed a simple interconnecting process with a novel lateral buffer mesa structure depending on a smoothly wet chemical etching profile of InP and InGaAs in the crystal direction of [01$\bar{1}$] for an InP-based vertical monolithically integrated transmitter OEICs. A monolithically integrated transmitter with 1.55μm in wavelength at a modulation rate of 1.25Gb/s was achieved with an output of an opening eye diagram.

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# 1.25Gb/s InP 基多量子阱激光器与 HBT 驱动电路的单片集成*

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**摘要**: 描述了一种基于 InP 材料沿[01$\bar{1}$]晶向湿法化学腐蚀形成平滑侧壁实现的 InP 基多量子阱激光器和异质结双极晶体管驱动电路单片集成. 通过一个横向缓冲台面结构, 降低了激光器阳极和晶体管集电极互连工艺的难度, 改善了光发射单片光电集成电路的可制造性. 采用该方法制作的光发射单片直流功耗为 120mW, 在码长 $2^{23}-1$ 传输速率 1.5Gb/s 伪随机码信号调制下有清晰的眼图, 光输出功率为 2dBm.

**关键词**: 光发射; 单片集成; 光电集成电路
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