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A Reduced-Order Modeling of Multi-Port RC Networks by Means of Graph Partitioning *

Yang Huazhong, Mao Xiaojian, Yan Zhaoran and Wang Hui

(Department of Electronic Engineering, Tsinghua University, Beijing 100084, China)

Abstract: A modified reduced-order method for RC networks which takes a division-and-conquest strategy is presented. The whole network is partitioned into a set of sub-networks at first, then each of them is reduced by Krylov subspace techniques, and finally all the reduced sub-networks are incorporated together. With some accuracy, this method can reduce the number of both nodes and components of the circuit comparing to the traditional methods which usually only offer a reduced net with less nodes. This can markedly accelerate the sparse-matrix-based simulators whose performance is dominated by the entity of the matrix or the number of components of the circuits.

Key words: interconnect; reduced-order modeling; graph partitioning; Krylov subspace
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1 Introduction

With the trend in microelectronic industry to the deep sub-micron era, the effects of the interconnection become more important than any time before. In order to get the precise information of these interconnects, a popular method is to simulate the equivalent RC networks extracted from the physical layout. But these RC networks are so big that it is time consuming and memory prone to simulate them directly.

For the feasibility of simulation, the reduced-order modeling of linear passive networks is an efficient way. A lot of related work has been presented in recent 5 years, such as PACT (pole analysis via congruence transformations)[1], AWE (asymptotic waveform evaluation)[2] and MPVL (matrix-Padé via Lanczos) based on Krylov subspaces[3,4], etc. Especially MPVL works accurately and stably. In the case of a net with large scale ports (clock nets or power nets are in this case), these methods can only reduce the number of nodes of the network, but could not reduce the number of components significantly because the result matrix of transfer function are dense and the actual components are not reduced. For the sparse-matrix based simulation tools, these node-reduced but component-unreduced networks gain a very limited benefit. For

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Yang Huazhong　male, was born in 1967, professor. His research field covers speech/audio signal processing chips, CMOS analog and RF integrated circuits, system-on-a-chip architectures, and their design automation techniques.

Mao Xiaojian　male, was born in 1978, PhD candidate. His research interests are in CMOS RF IC design and design automation.

Yan Zhaoran　male, was born in 1978, MS candidate. He mainly focuses on static timing analysis and reduced modeling.

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example ,a network with 100 ports ,500 internal nodes and 10000 components should not be reduced to a circuitry with less than 100 nodes. As the result matrix G_n and C_n in $H_n(s)$ are dense ,the reduced network still has about 100 ×100 components.

To vanquish this grief , we present an amended method. It takes 3 steps shown in Fig. 1 to reduce the network. Step one is to divide the original multi-port network in some smaller sub-networks with a moderate number of ports. Step two is to reduce the sub-networks one by one by means of MPVL. Step three is to link the reduced sub-networks into a result network in which both the nodes and components are greatly reduced .

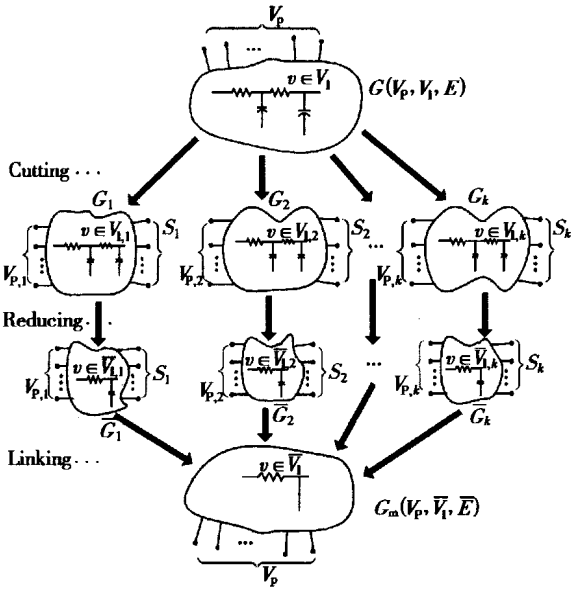

Fig. 1 Algorithm flowchart of partitioning-based RC network reduction.

2 Partitioning-based reduced-order modeling

Let $G(V_P, V_I, E)$ be the graph representing the multi-port RC network to be reduced ,where V_P and V_I represent sets of the ports (or external nodes) and internal nodes ,respectively. $|E| = L$,$|V_P| = N_P$,and $|V_I| = N_I$ represent the number of components , ports and internal nodes of the network ,respectively. Suppose any port could be an input or output port , then the transfer function of $G(V_P, V_I, E)$ can be expressed as[3] :

$$H(s) = B^T(G + sC)^{-1}B \tag{1}$$

where G and C represent $N \times N$ real sparse matrices , $N = N_P + N_I$,and B represents an $N \times N_P$ real matrix. The transfer function of the reduced network would be as

$$H_n(s) = B_n^T(G_n + sC_n)^{-1}B_n \tag{2}$$

where G_n and C_n represent $n \times n$ real dense matrices , $n \geq N_P$,and B_n represents an $n \times N_P$ real matrix. The traditional techniques of reduced-order modeling can only make n much smaller than N but could not guarantee the sparsity of G_n and C_n. Thus the number of components of the reduced network is very close to N_P^2 which exposes the fact that traditional reduced-order modeling will lose efficiency if $L \approx N_P^2$.

To overcome this difficulty ,we partition $G(V_P, V_I, E)$ into k sub-graphs , $G_j(V_{P,j} \cup S_j, V_{I,j}, E_j)$, $j = 1, 2, \cdots, k$, where $S_j \subset V_I$ represents the separator of $G(V_P, V_I, E)$, $\bigcup_j (V_{I,j} \cup S_j) = V_I, (\bigcup_j V_{I,j}) \cap (\bigcup_j S_j) = \varnothing, V_{I,j} \cap V_{I,i} = \varnothing$ for $\forall i \neq j$, $\bigcup_j V_{P,j} = V_P, V_{P,j} \cap V_{P,i} = \varnothing$ for $\forall i \neq j$, $E_j = \{(u, v) \mid u, v \in V_{P,j} \cup S_j \cup V_{I,j}, (u, v) \in E\}$ and $\bigcup_j E_j = E$. And the partitioning process can be realized by taking the vertex cut algorithm[5] recursively. If the network is a tree ,the partitioning process can be performed simply and efficiently.

After partitioning ,each sub-network is reduced individually , and nodes in S_j and $V_{P,j}$ are regarded as the ports of the jth sub-network. By MPVL ,the reduced transfer function of the jth sub-network is derived as

$$H_{n,j}(s) = B_{n,j}^T(G_{n,j} + sC_{n,j})^{-1}B_{n,j}, \quad j = 1, 2, \cdots, k \tag{3}$$

where $G_{n,j}$ and $C_{n,j}$ represent $n_j \times n_j$ real dense matrices , $B_{n,j}$ represents an $n_j \times N_{P,j}$ matrix , $N_{P,j} = |V_{P,j}| + |S_j|$,and $n_j \geq N_{P,j}$. Thus $G_j(V_{P,j} \cup S_j, V_{I,j}, E_j)$ is reduced to $\overline{G}_j(V_{P,j} \cup S_j, \overline{V}_{I,j}, \overline{E}_j)$,where $|\overline{V}_{I,j}| = n_j - N_{P,j}$,and in general $|\overline{E}_j|$,the number of the com-

ponents of the *j*th reduced sub-network, is at the scale of n_j^2.

Finally, all the k reduced sub-networks are incorporated into $G_m(V_P, \overline{V_I}, \overline{E})$ which is the reduced model of $G(V_P, V_I, E)$, where $\overline{V_I} = \bigcup_j (S_j \cup \overline{V_{I,j}})$, $\overline{E} = \bigcup_j \overline{E_j}$, and the number of the components in the reduced network is proportional to $\sum_{j=1}^{k} n_j^2$ which is much smaller than N_P^2, the number of components of the reduced network by MPVL without partitioning.

In order to reduce the number of components drastically, $G(V_P, V_I, E)$ should be partitioned as homogeneous as possible and all the node cut sets S_j should be minimized. For a general graph, these partitioning constraints are quite hard to be satisfied. Fortunately, the mostly actual RC nets are of very limited loops and in most cases they are in tree structures with no loops, thus the partitioning process consumes an extremely limited time of CPU.

3 Numerical results

As MPVL is the most effective model-reduction algorithm and becomes popular in recent years, it has been embedded into our three-step partitioning-based RC network reduction flow. In fact, any other traditional reduced-order modeling techniques can be embedded into our flow too. To compare the efficiency and accuracy, some actual RC nets are reduced by MPVL with and without partitioning, respectively. All the reduced RC nets by our method are equivalent to their original nets because their electrical performance differences, measured by circuit simulator HSPICE[6], are less than 1 %. The HSPICE simulation time of original nets and the reduced ones is listed in Table 1, which shows there is a significant speed improvement in sparse-matrix based simulators.

Table 1 Comparison of MPVL with and without partitioning

Index	Port #	Reduction time/s		Component #			Simulation time by HSPICE/s		
		Reduction w/o Part.	Reduction w/ Part.	Original	Reduced w/o Part.	Reduced w/ Part.	Original	Reduced w/o Part.	Reduced w/ Part.
1	50	5.25	1.75	3390	819	428	266.5	110.2	27.0
2	100	55.80	6.45	10120	2408	1080	1111.7	469.4	93.3
3	150	540.9	21.53	25500	12060	1455	4738.7	3638.8	130.6
4	240	2743.88	163.23	50000	25124	6024	15477.9	12399.3	692.4
5	500	—	824.30	150000	—	14412	124031.4	—	2511.2

According to the experimental results shown in Table 1, we can see that the results of partitioning-based reduction method show better performance. The simulation time of the reduced network by our method listed in column 10 is much less than those of the original and the reduced networks without partitioning, listed in column 8 and column 9, respectively. Comparing the run time shown in column 8 and column 9, we can see that the speed improvement of the reduction algorithm without partitioning drops from 141.8 % to 24.8 % when the number of ports increases from 50 to 500. Of particular note that shown in columns 3 and 4 when the partitioning method is carried out, the reduction process will save more time because the computational cost grows drastically with the increasing dimension of matrix G and C in $H(s)$. And MPVL even failed in the 5th experiment because it is run out of memory. So in this aspect, the partitioning is not only an efficient way to reduce the number of components but also a necessary way for any interconnect with very large scale ports.

4 Conclusion

The modified reduced-order method presented in this

paper takes partitioning and MPVL to reduce the numbers of both nodes and components of multiport RC networks. This actually accelerates not only the sparse-matrix-based circuit simulators whose computational cost is dominated by the entity of the matrix or the components of the network but also the reduction process itself. Other reduced-order modeling techniques can also be embedded in our three-step partitioning-based flow, and the partitioning strategy should be applied to RCL networks.

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采用图划分技术的多端口 RC 网络约减方法*

杨华中 冒小建 燕昭然 汪 蕙

(清华大学电子工程系, 北京 100084)

摘要: 提出了一种采用分而治之的改进型 RC 网络约减方法. 该方法首先将被约减的网络划分成若干子网络,然后用 Krylov 子空间算法逐个约减这些子网络,最后将所有被约减后的子网络链接起来就获得了原网络的约减网络. 传统的 Krylov 子空间算法只能约减电路的节点数目,而该方法在保证精度的条件下不仅可以约减电路的节点数目,而且能够约减其元件数目. 这可以极大地提高采用稀疏矩阵技术的电路模拟工具处理互连线的效率,因为这类电路模拟工具的计算成本主要取决于电路矩阵中非零元的个数,即电路中的元件数目.

关键词: 互连线; 模型约减; 图划分; Krylov 子空间

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杨华中 男,1967 年出生,博士生导师,目前的研究方向主要包括语音/音频信号处理芯片、与数字 CMOS 工艺兼容的模拟与射频集成电路、微系统芯片(SoC)的体系结构与设计自动化技术等.

冒小建 男,1978 年出生,博士研究生,主要研究方向 CMOS 模拟电路设计及设计自动化.

燕昭然 男,1978 年出生,硕士研究生,主要研究方向静态时序估计和网络压缩算法研究.

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