A Novel Technique of Parameter Extraction for Short Channel Length LDD MOSFETs

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Abstract: A novel parameter extraction technique suitable for short channel length lightly-doped-drain (LDD) MOSFET’s is proposed which segments the total gate bias range, and executes the linear regression in every subsections, yielding the gate bias dependent parameters, such as effective channel length, parasitic resistance, and mobility, etc. This method avoids the gate bias range optimization, and retains the accuracy and simplicity of linear regression. The extracted gate bias dependent parameters are implemented in the compact I-V model which has been proposed for deep submicron LDD MOSFET’s. The good agreements between simulations and measurements of the devices on 0.18μm CMOS technology indicate the effectivity of this technique.

Key words: LDD MOSFET; parameter extraction; parasitic series resistance; mobility
PACC: 7220H; 7230 EACC: 2560B; 2560R

1 Introduction

The device parameter extraction is important for describing the device electrical characteristics in CMOS technology. The linear regression extraction is one of the most effective methods. However, it is not easy for very short channel devices because the fundamental assumption of the linear $R_{n+}V_{ss}^{-1}$ derived from the measured $I_n-V_{pp}$ curves causes significant errors, particularly for the lightly-doped-drain (LDD) devices. Many improved extraction methods, such as “S&R” method, “single device” method, etc., have been published for this purpose[1-5]. As a matter of fact, some of parameters, including electrical effective channel length, parasitic series resistance, mobility, etc., are gate bias dependent, although artificially constant $L_e$ and $R_s$ are more desirable for compact model. Thus an optimized gate overdrive ($V_{gs} - V_{th}$) range has to be determined for linear regression operations in order to minimize the bias dependence of the parameters, which is usually technology specific. This is why most extraction techniques require a similar gate bias range optimization[1-5]. With the decreases of channel length and gate oxide thickness, the obvious nonlinearity that is caused by the effect of the gate voltage on the channel electric field through very thin gate oxide increases the difficulties of this work.

This paper presents a new extraction method in which the total gate bias range is segmented into many small bias subsections, and then the linear regression is executed in every bias subsection, which results in the bias independent parameters. The different values of the parameters are obtained at different gate bias subsections. In other words, the
gate bias dependent parameters are derived. This simple method avoids the complicated optimization of the gate bias range and retains the accuracy of linear regression extraction. As validity, the measured data from LDD NMOSFETs of different channel lengths fabricated on 0.18µm LDD CMOS technology are used to extract the gate bias dependent \( L_{\text{off}}, R_{\text{on}}, \) and \( \mu_c \) with the new method, and then these parameters are implemented in the compact model which has been proposed for short channel LDD MOSFETs.

2 Parameter extraction technique

In the theory of linear regression extraction, at a very small drain bias (approximately \( V_{\text{ds}} = 50\text{mV} \)), the total drain to source resistance is expressed by\(^{[3]}\):

\[
R_{\text{total}} = \frac{V_{\text{ds}}}{I_{\text{ds}}} = R_{\text{on}} + \frac{L_{\text{on}} - \Delta L}{\mu_c C_{\text{ox}} W} \times (\frac{1}{V_{\phi}} + \Theta)
\]

(1)

where \( R_{\text{on}} \) is parasitic series resistance outside the channel, \( L_{\text{off}} = L_{\text{on}} - \Delta L \) equals electrical effective channel length and \( \Delta L \) is defined as the channel reduction, the gate overdrive \( V_{\phi} = V_{\text{ds}} - V_{\text{th}} \) and \( V_{\text{th}} \) is the threshold voltage, \( C_{\text{ox}} \) and \( W \) are the gate oxide capacitance and the gate length, respectively, \( \mu_c \) and \( \Theta \) are the low electric field mobility and the mobility degradation factor, respectively. The linearity between \( R_{\text{total}} \) and \( V_{\phi}^{-1} \) must be guaranteed in linear regression operation, therefore the gate bias independent parameters \( \mu_c, \Theta \) and \( \Delta L \) must be assumed. It is also shown from Eq. (1) that the relation between \( R_{\text{total}} \) and \( L_{\text{on}} \) is linear at a constant gate bias, thereby for \( R_{\text{on}} \) and \( \Theta \) extraction of devices with different channel lengths. In fact, the nonlinearity between \( R_{\text{total}} \) and \( V_{\phi}^{-1} \) is clearly shown in short channel length and very thin gate oxide devices, even in a small gate bias range. In our work, the LDD NMOSFETs with 3.2nm gate oxide thickness and different gate lengths on 0.18µm CMOS technology give the \( R_{\text{total}} - V_{\phi}^{-1} \) curves shown in Fig. 1. These curves demonstrate the serious nonlinearity at the range of total bias \( V_{\text{ds}} \) that should be just used for extraction. This phenomenon indicates that some of the extracted parameters are closely gate bias dependent\(^{[3]}\) particularly for LDD devices. This in turn causes a problem of accuracy of linear regression.

![Fig. 1 Drain-source resistance versus \( V_{\phi}^{-1} \) nonlinear curves derived from the \( I_{\text{ds}}-V_{\phi} \) characteristics of different gate length LDD NMOSFETs with thin gate oxide (3.2nm) and 20µm gate width fabricated on 0.18µm CMOS technology](image)

However, the simplicity of the linear regression extraction is an attractive issue in device modeling. It is hence proposed in this paper that the related parameters are treated as gate bias independent in a very small gate bias range, such as 0.1V range, therefore guaranteeing the effectiveness of linear regression. The total \( V_{\phi} \) range is segmented by 0.1V step and the linear regression extraction is repeated in different subsections to obtain the parameter array at different gate biases. It is noted that the subsection range which is average of 0.1V in this paper is determined in terms of the nonlinearity of \( R_{\text{total}} - V_{\phi}^{-1} \) characteristic, that is, the large range for weakly nonlinearity, and the small range for strong nonlinearity, usually a factor lower than the total \( V_{\phi} \) range. The smaller range will improve the description of the bias dependence, and yet increase the calculations. Consequently, the extracted \( R_{\text{on}}(V_{\phi}) \) and the \( \Delta L(V_{\phi}) \) are modeled by curve fit-
ting in order to implement in the device model. Simultaneously, the extracted $\mu_0$ and $\Theta$ give the effective mobility $\mu_{eff}(V_g)$ array by $\mu_{eff} = \mu_0/(1 + \theta V_g)$. In our work, the LDD NMOSFETs with 0.18~2.0 $\mu m$ gate mask lengths are used to extract the parameters by linear regression. In details, the threshold voltages $V_{th}$ of different $L_{mask}$ devices are first extracted by "peak $g_m$" technique from the measured $I_{ds}-V_{gs}$ characteristics and then the gate overdrive $V_{gs}$ is obtained for next extraction operation. For every device of different gate length $L_{mask}$, at each 0.1 $V$ step of $V_{gs}$, the slope of $R_{total}-V_{gs}^{-1}$ straight line, i.e., $slope = (L_{mask} - \Delta L)/\mu_0 C_{ox} W$, is obtained and then is used to plot the slopes-$L_{mask}$ curve which should be straight line under the assumption of gate bias independent parameters. By linear regression, the slope of the straight line (it equals $1/\mu_0 C_{ox} W$) is used to extract $\mu_0$ and the intercept of the line gives $\Delta L$. Simultaneously, a family of $R_{total}-L_{mask}$ straight lines at different $V_{gs}^{-1}$ biases is drawn, and then be used to extract $R_\Theta$ by intercept with the vertical line of $\Delta L$ while the $\Delta L$ has been determined. Different from the $R_\Theta$ extraction and interpretation in Ref. [5], the well linearized family of $R_{total}-L_{mask}$ lines must intersect at one point with a coordinate $(\Delta L, R_\Theta)$, which is easily understood from Eq. (1). This point gives the $R_\Theta$ independent with $V_{gs}$. Furthermore, the $\Theta$ is extracted by slope of the $R_{total}-L_{mask}$ straight line at extrapolated $V_{gs}^{-1} = 0$, i.e., $slope = \Theta/\mu_0 C_{ox} W$. The $\mu_0$ and $\Theta$ are then used to derive the effective mobility $\mu_{eff}$. Finally, the linear regression operations step by step yield the $R_\Theta-V_{gs}$, the $\Delta L-V_{gs}$, and the $\mu_{eff}-V_{gs}$ curves. These accurate extraction parameters are then embedded in the compact model of the devices. In the device model, a constant low electric field mobility $\mu_0$ and a constant mobility degradation factor $\Theta$ are more desired. To this end, the $\mu_{eff}-V_{gs}$ curve is used to optimize the two constants by least square algorithm at the total bias range, shown as $^{[6]}$

$$\mu_{eff} = \frac{\mu_0}{1 + \theta V_g}$$  \hspace{1cm} (2) 

where the factor $r$ indicates the nonlinearity of the curve. To obtain the physically reasonable constant $\mu_0$ and $\Theta$, the factor $r$ is not unity and related with process for short channel length LDD devices, which has been experimentally proved in Refs. [6, 7]. The optimized results in our work will be illustrated in next section.

3 Experiment and extraction results

The extraction is operated on an array of LDD NMOSFETs with 20 $\mu m$ gate width and 0.18, 0.26, 0.36, 0.5, 0.7, 1.0, 1.5, and 2.0 $\mu m$ gate lengths, on 0.18 $\mu m$ CMOS technology and the gate oxide thickness is 3.2 $\mu m$. By "peak $g_m$" technique, the extracted threshold voltages of different gate lengths are shown in Fig. 2(a), in which the $V_{th}$ reduction is observed in very short channel length devices. By continuous linear regression, the extracted $R_\Theta$, $\Delta L$, and $\mu_{eff}$ curves at 0.2~2.5 $V$ gate overdrive $V_{gs}$ range are demonstrated in Fig. 2(b)~(d). The results indicate that it would cause big errors if the gate bias independent parameters were assumed in compact device model. It is also found in the figures that $R_\Theta$ and $\Delta L$ decrease from maximum and tend to be constants with the $V_{gs}$ increasing to high value. This indicates that the bias independent parameter's assumption is practical when the $V_{gs}$ is high enough. This is why the constant parameters are usually assumed in large dimensional devices with high bias voltage operations. But this is limited by the low bias applications in deep submicron devices, increasing the difficulties of the parameter extractions. In Fig. 2(d), the well optimized curve gives the results: $\mu_0 = 307 cm^2/(V \cdot s)$, $\Theta = 0.16$, and $r = 1.65$. They are in reasonable range. The low $\mu_0$ value is caused by the $t_{ox}$ very small gate oxide thickness. It has been illustrated experimentally in Ref. [4] that the reduced $t_{ox}$ yields the decreased mobility.
Fig. 2  Extracted parameters by new method, where (a) is the extracted threshold voltages of different gate length LDD N MOSFETs by "peak transconductance and extrapolation" method, (b) is the gate bias dependent parastic series resistance, (c) is the gate bias dependent channel reduction, and (d) is the gate bias dependent effective mobility. The solid line in (d) is the optimized result which gives the constant $\mu_0$ and $\theta$ for device model.

4 Validity in the LDD nMOSFET's $I-V$ model

The extracted parameters are implemented in the LDD nMOSFET's compact $I-V$ model which has been proposed and detailed in Ref. [8], briefly given as follows.

The nonlinear current $I_{\text{th}}(V_{gs}, V_{db})$ with hyperbolic-tangent description is given by

$$I_{\text{th}}(V_{gs}, V_{db}) = I_{\text{sat}} (1 + \lambda V_{db}) \tanh(\alpha V_{db})$$  \hspace{1cm} (3)

where the critical saturated drain current $I_{\text{sat}}$, the channel length modulation parameter $\lambda$, and the saturation voltage parameter $\alpha$ are given respectively as

$$I_{\text{sat}} = W v_{sat} C_{ox} (V_{gs} - V_{th} - \gamma V_{db})$$  \hspace{1cm} (4)

$$\lambda = \left. \frac{\partial I_{\text{th}}}{\partial V_{db}} \right|_{V_{db} = V_{\text{sat}}} = \frac{1}{V_{db}} \times \frac{I_{d} E_{c}}{(L_{eff} - L_{d}) E_{c} + V_{db}}$$  \hspace{1cm} (5)

$$\alpha = \left. \frac{\partial I_{\text{th}}}{\partial V_{db}} \right|_{V_{db} = 0} = \frac{1}{I_{\text{sat}}} \times \frac{\mu_s C_{ox} W}{L_{eff}}$$  \hspace{1cm} (6)

The process well matched substrate current model for submicron and deep submicron LDD MOSFETs is shown as

$$I_{\text{sub}} = I_{db} \times \frac{A_{d}}{B_{d}} \times (V_{ds} - \eta V_{db}) \times \exp(- \frac{IB_{d}}{V_{db} - \eta V_{db}})$$  \hspace{1cm} (7)

In this model, $R_h$ (i.e. $R_s + R_c$) is defined as external parameter, and the relation between external
and intrinsic biases yields an iterated calculation for the model. So the extracted $R_s$ and $\Delta L$ fitting models are easily embedded to the $I-V$ characteristics. It is clear that the gate bias dependent parasitic series resistance and channel reduction are more reasonable for describing the reality of device. The simulated and experimental characteristics families of 20μm/0.18μm LDD NMOSFETs, including $I_{ds-V_{ds}}$, $I_{ds-V_{gs}}$, $g_{ds-V_{gs}}$, and $I_{ds-V_{gs}}$, are given.
in Fig. 3(a) ~ (c). The excellent agreements between simulations and measurements show the accuracy of the extracted parameters and the effectiveness of the compact I-V model for deep submicron devices. Furthermore, Figure 4(a) ~ (c) also give the comparison between measurements and simulations of 0.26, 0.36, and 0.35 μm gate lengths LDD devices. The results indicate the robustness of the extraction technique and the device model.

5 Conclusion

We propose a novel parameter extraction technique suitable for short channel length LDD MOSFET’s. It avoids the gate bias range optimization of the linear regression extraction by segmenting the total gate bias region. In a very small gate bias range, the extracted parameters are nearly gate bias independent, therefore maintaining the effectiveness of linear regression. The repeat extraction operations accurately obtain the gate bias dependent parameters and well be modeled. The extracted parameters are then implemented in the proposed I-V model for LDD MOSFET’s. The agreements between simulations and measurements of different gate lengths devices indicate the effectiveness and the robustness of this technique.

References


一种适用于短沟道 LDD MOSFET 参数提取的改进方法

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摘要：提出了一种适用于短沟道 LDD MOSFET 的改进型参数提取方法。通过对电荷分布和结电容采用线性回归方法，提取参数相关性，保证了线性回归方法的精度和有效性。避免了对电荷分布的优化和误差考虑。提出的参数适用于已建立的深亚微米 LDD MOSFET 的 I-V 特性模型中，模拟与测试数据的吻合表明了该方法的实用性。

关键词：轻掺杂漏 MOSFET；参数提取；寄生串联电阻；迁移率
PACC: 7220H；7230 EACC: 2560B；2560R

* 国家自然科学基金资助项目（批准号：60206006）
于春利，女，博士研究生，从事深亚微米 CMOS 器件建模及可靠性应用的研究。
2003-12-22 收到，2004-03-29 收稿 ©2004 中国电子学会