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Energy Recovery Threshold Logic and Power Clock Generation Circuits*

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Abstract: Energy recovery threshold logic (ERTL) is proposed, which combines threshold logic with adiabatic approach. ERTL achieves low energy as well as low gate complexity. A high efficiency power clock generator is also proposed, which can adjust duty cycle of MOS switch in power clock generator depending on logic complexity and operating frequency to achieve optimum energy efficiency. Closed-form results are derived, which facilitate efficiency-optimized design of the power clock generator. An ERTL PLA and a conventional PLA are designed and simulated on 0.35μm process. The energy efficiency of the proposed power clock generator can reach 77%~85% operating between 20~100MHz. Simulation results indicate that ERTL is a low energy logic. Including power loss of power clock circuits, ERTL PLA still shows 65%~77% power savings compared to conventional PLA.

Key words: energy recovery; low power; power clock; threshold logic; CMOS circuits

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1 Introduction

Low energy is of utmost importance in, for example, a hand held computer, where its performance is not critical, but a battery life is of primary concern. Adiabatic computing is an attractive approach in this viewpoint[1,2]. Energy recovery threshold logic (ERTL) is proposed, which combines threshold logic with adiabatic methods. Threshold logic has been attractive for the reasons of reduced logic depth and gate count compared to traditional AND-OR-NOT logic gate based design[3]. ERTL uses capacitor coupling technique to realize the threshold logic. ERTL reduces energy dissipation as well as gate complexity.

Energy recovery logic is clocked and supplied by power clock. Power clock generator usually consumes large fraction of the total loss of the adiabatic system and degrades the energy savings of the adiabatic logic[4]. The design of power clock generator, therefore, is an important part of the adiabatic system design. A high-efficiency power clock generator which generates four phase power clock required by ERTL is also presented. The power clock circuit generates synchronized power clock which makes it possible to integrate the adiabatic module into a VLSI system. The duty cycle of MOS switch in power clock generator can be optimized according to logic complexity and operating frequency to achieve higher energy efficiency. A closed-form results that facilitate efficiency-optimized design of the power clock generator are derived.

A 5×8×4 PLA is designed and simulated us-

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ing ERTL. Results are compared with a conventional PLA which adopts domino logic.

2 Energy recovery threshold logic

Figure 1 shows base ERTL gate structure. The ideal four phase overlapping power clock Φ_i and the corresponding auxiliary clock CK_i are shown in Fig. 2. Φ_i has four phases, i. e. evaluate, hold, (energy) recovery, wait. CK_i is high during the wait phase of Φ_i and low during the other phases.

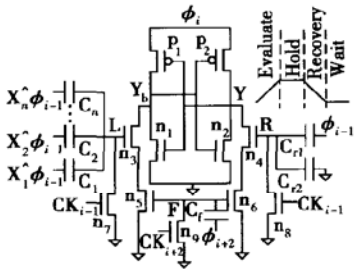

Fig. 1 ERTL gate structure

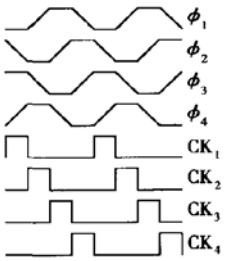

Fig. 2 ERTL ideal power clock and auxiliary clock

During the wait phase of Φ_i, nodes L and R are floating, and the voltage difference of nodes L and R are generated through capacitor coupling as Φ_{i-1} ramps high. $V_L = V_{dd}(\sum_{i=1}^{n} C_i X_i)/C_L$, $V_R = V_{dd}C_{r1}/C_R$, where C_L and C_R are the total parasitic capacitance at nodes L and R respectively. During the evaluate phase of Φ_i, the voltage difference at nodes L and R generates a current difference at the differential pair. The differential output at nodes Y and Y_b can be evaluated by the sense amplifier consisting of p_1, p_2, n_1, n_2. If $V_L > V_R$, Y_b is low and Y is high, and vice versa. During the hold phase of Φ_i, the outputs hold the value, and the voltage of nodes L and R ramp to low as Φ_{i-1} ramps down. During the recovery phase of Φ_i, charge of outputs is recovered, and nodes L and R are clamped to low through n_7 and n_8.

The transistors n_5 and n_6 switch on during the evaluate phase of Φ_i for evaluation, switch off during the other phases for power saving, and are controlled by coupling capacitor C_f and power clock Φ_{i+2}. The clamping transistors n_7, n_8 and n_9 switch on only during the wait phase of Φ_{i-1} and Φ_{i+2} respectively for avoiding nodes L, R and F floating all the time, and they are controlled by CK_{i-1} and CK_{i+2} respectively.

Ideally, ERTL operates with four phase trapezoid power clock. However, generating trapezoid power clock is difficult and energy-inefficient. Sinusoidal-like power clock circuit based on LC resonant technique is simple and energy-efficient. ERTL circuit can also operate with sinusoidal-like power clock, but it dissipates slightly more power than that with ideal trapezoid power clock. A simple high-efficiency power clock generator for ERTL circuits which generates sinusoidal-like power clock is proposed in the next section.

3 Power clock generation circuit and design

Various power clock circuit topologies for resonant energy recovery have been proposed[4~7]. The power clock generation circuit based on synchronous 2N2P topology[7] is proposed, as shown in Fig. 3. It contains two parts: switch signal generation circuit and DC/AC converters.

3.1 Power clock generation circuit

The DC/AC converter is based on the resonant, zero-voltage and zero-current switching techniques. The clock nodes of ERTL circuits are represented by lumped model C_i and R_i. For each phase, an approximate lumped-element model of the logic is built including an equivalent capacitor

C to model the energy storage, in series with a resistor R to model the losses. The capacitors C_{Ei} are external balancing capacitors to achieve more energy efficiency. Since the Q of the on-chip inductors is low, the external high Q inductor is used. NMOS and PMOS of DC/AC converters operate as switches to DC supply and ground to sustain a steady-state oscillation by supplying loss of energy, which are turned on and off in an alternating, periodic manner. The DC/AC converter produces two power clocks which have 180° phase difference. But ERTL needs four-phase clocking, so two DC/AC converters which have 90° phase difference are needed. The DC/AC converters are initiated and synchronized by switch signals fi_1 ~ fi_4, which are produced by switch signal generation circuit. The timing of fi_1 ~ fi_4 are shown in Fig. 3(c). For achieving high energy efficiency, the duty cycle of the switches is chosen so that in the steady state, the total energy dissipated exactly balances the energy added during the turn-on of MOS switches.

The frequency of external main clock is two times that of the internal oscillation frequency, which is a 50% duty cycle square wave. The 25% duty cycle negative pulse clk_1 ~ clk_4 (in Fig. 3(a)) is generated by a circuit similar to a Johnson counter using two D-latches and four NAND gates, and they are used to synchronize and generate switch signals fi_1 ~ fi_4. The pulse width of the switch signals is controlled to tune the duty cycle of the switches by adjusting the delay of buffer chain in pulse generator circuits as shown in Fig. 3 (d).

The auxiliary clocks CK_1 ~ CK_4 needed in ERTL circuits are obtained easily from the switch signals fi_1 ~ fi_4 in the power clock generator with an inverter.

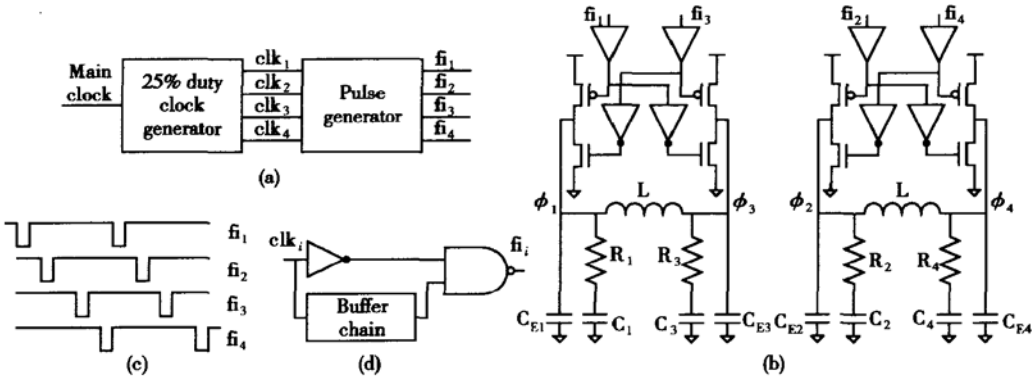

Fig. 3 (a) Switch signal generation circuit; (b) DC/AC converters; (c) Switch signal timing; (d) Pulse generator circuit

3.2 Power clock design

In section 3.1, the proposed power clock generation circuit is described. In this section, how to optimize and determine the device parameters of power clock generator is derived. Firstly the adiabatic circuit for which the power clock generator is designed should be modeled. The values of the model parameters, R and C, can be extracted from the simulation tests where an external ideal sinusoidal voltage source is applied as the power clock. For a given clock frequency f and a logic activity, for each phase, the power loss P_L in the logic, and the rms current I_L supplied to the logic by the power clock can be measured from the test. For the purpose of power clock design, the test should be performed for the logic activity that corresponds to the worst-case losses. Given P_L and I_L, the model parameters can be determined as[7]:

$$R = \frac{P_L}{I_L^2} \tag{1}$$

$$C = \frac{\sqrt{2} I_L}{\pi V_{DD} f} \tag{2}$$

where V_{DD} is the peak value of the applied power clock.

The inductor value of L_r is determined by the required frequency and the sum of the extracted capacitance C and the balance capacitance C_E. The oscillating frequency for the 2N2P power clock generators is determined by:

$$f = \frac{1}{2\pi \sqrt{L_r \times \frac{C + C_E}{2}}} \tag{3}$$

Finally, the device size W of MOS switches in DC/AC converters is optimized. The total power loss P of one MOS switch in power clock generator consists of the gate-drive switching loss and the device conduction loss:

$$P = WLC_{ox}V_{DD}^2 f + \frac{I_s^2}{K_p \times \frac{W}{L} \times (V_{DD} - V_t)} \tag{4}$$

I_s is the conducting rms current of MOS switches. Minimization of the power loss with respect to the device size W yields the optimum value:

$$W_{opt} = \frac{I_s}{V_{DD} \sqrt{K_p C_{ox}(V_{DD} - V_t) f}} \tag{5}$$

To determine the switch rms current I_s, we observe that the switch current during the turn-on interval is increasing from zero approximately as a linear function of time. Assumed that the switch duty cycle D is chosen so that the total energy dissipated in the system per cycle exactly balances the energy added per cycle. The required energy balance given approximately by[6]:

$$\frac{1}{2} L_r i_{on}^2 = \frac{P_L}{f} \tag{6}$$

i_{on} is the switch current at the end of the switch on-time.

$$i_{on} = \frac{V_{DD}}{L_r} \times D \tag{7}$$

The switch rms current I_s is then given by[5]:

$$I_s = i_{on} \sqrt{D/3} \tag{8}$$

Once the switch rms current I_s is determined by Eqs. (6), (7), and (8), Eq. (5) can be used to determine the optimum device size. The optimum switch duty cycle D can be determined by Eqs. (6), (7). Power clock generator designed with the optimum device size W and the optimum switch duty cycle D achieves the optimum MOS switch power loss given by Eq. (4).

4 Simulation results

Simulation have been performed on one ERTL PLA supplied by the power clock circuits shown in Fig. 3. The power clock is designed following the derived results in section 3. 2. One conventional PLA implemented in domino logic[8] is also designed. The logic equations implemented in the PLA are as follows:

$$\begin{aligned} z_1 &= a\bar{b}\bar{d}\bar{e} + \bar{a}\bar{b}\bar{c}\bar{d}\bar{e} + bc + de \\ z_2 &= \bar{a}\bar{c}e \\ z_3 &= bd + \bar{c}\bar{d}\bar{e} + bc + de \\ z_4 &= \bar{a}\bar{c}e + ce \end{aligned} \tag{9}$$

where z_n are the outputs and a, b, c, d, and e are the inputs. Table 1 shows the power dissipation of conventional PLA and ERTL PLA with the optimized power clock. The circuits are simulated with 5V power supply and 100fF output loading and designed base on TSMC 0.35μm process.

Table 1 Power dissipation of ERTL PLA and conventional PLA operating on various frequency

Frequency/MHz	20	50	100
Power loss of ERTL core/μW	106	197	527
Power loss of DC/AC converter/μW	18.6	47	154
Power loss of auxiliary clocks/μW	6.7	16.7	34
Total power loss of ERTL PLA/μW	131.3	260.7	715
Energy efficiency/%	85	81	77
Power loss of conventional PLA/μW	408	1010	2020
Power ratio of ERTL PLA and conventional PLA/%	32	26	35

The loss of switch signal generation circuit (Fig. 3(a)) does not depend on either the operating frequency or complexity of ERTL circuit. If the complexity of ERTL circuit is higher, the loss of switch generation circuit becomes a negligible portion. As such, in Table 1, only the power dissipation of the DC/AC converter which comprises the MOS switches and the driver is considered as the

loss of power clock generation. The energy efficiency is defined as: $P_L/(P_L+P_C)$, P_L is the power loss in ERTL core, P_C is the power loss in DC/AC converter. For frequency varying between 20 ~ 100MHz, energy efficiency is 85% ~ 77%, indicating that the proposed power clock generator is a high efficiency generator. ERTL is a low-energy, adiabatic logic. Including the power clock loss, ERTL still shows 74% ~ 65% energy saving compared with conventional PLA.

5 Conclusion

In this paper, ERTL, a low-energy energy recovery logic, is proposed, which uses capacitor coupling technique to realize the threshold logic. A high efficiency power clock generator is also presented which generates four-phase sinusoidal power clocks for ERTL circuits. The power clock design is to integrate all power-clock switching transistors and associated control circuitry on the same CMOS chip with ERTL logic, which is well suited for low-power power conversion. Only high Q inductors and small balance capacitors are added as external components. The duty cycle of MOS switch in power clock generator can be adjusted depending on logic complexity and operating frequency to achieve optimum energy efficiency. Closed-form results are derived to facilitate efficiency-optimized design of power clock generator.

A ERTL PLA and a conventional PLA are designed and simulated on TSMC 0.35μm process. The simulation results indicate that the proposed power clock generator is high-efficiency and ERTL is a low-power logic. Between 20~ 100MHz, energy efficiency of the proposed power clock generator is 85% ~ 77%, and energy savings of ERTL PLA over conventional PLA is 74% ~ 65%.

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能量回收阈值逻辑及其功率时钟产生电路*

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摘要: 提出了能量回收阈值逻辑电路(ERTL). 该电路把阈值逻辑应用到绝热电路中, 降低能耗的同时也降低了电路的门复杂度. 并且提出了一种高效率的功率时钟产生电路. 该功率时钟电路能够根据逻辑的复杂度和工作频率, 调整电路中 MOS 开关的开启时间, 以取得最优的能量效率. 为了便于功率时钟的优化设计, 推导出了闭式结果. 基于 0.35μm 的工艺参数, 设计并且仿真了 ERTL 可编程逻辑阵列(PLA) 和普通结构 PLA. 在 20~ 100MHz 的工作频率范围内, 提出的功率时钟电路的能量效率可以达到 77% ~ 85%. 仿真结果还显示, ERTL 是一个低能耗的逻辑. ERTL PLA 与普通结构的 PLA 相比, 包括功率时钟电路的功耗在内, ERTL PLA 仍节省 65% ~ 77% 的功耗.

关键词: 能量回收; 低功耗; 功率时钟; 阈值逻辑; CMOS 电路

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