第25卷第12期 半 导 体 学 报 Vol. 25, No. 12
2004年12月 CHINESE JOURNAL OF SEMICONDUCTORS Dec., 2004

Fabrication of 4H-SiC Buried-Channel nMOSFETs

Gao Jinxia, Zhang Yimen and Zhang Yuming

(Microelectronics Institute, Xidian University, Xi'an 710071, China)

Abstract: The buried channel (BC) nMOSFETs with gate oxide grown thermally on 4H-SiC are fabricated. The BC region and source/drain region are formed by nitrogen implantation at room temperature followed by annealing at 1600℃. The channel depth is about 0.2μm. The peak field-effect mobility of 18.1cm^2/(V·s) for 5μm device is achieved. Thickly dotted pits found in the surface through microscope may be one of the important factors of the cause low field-effect mobility. The threshold voltages are 1.73V and 1.72V for the gate lengths of 3μm and 5μm respectively. The transconductance at V_G= 20V and V_D= 10V is 102μS for the gate length of 3μm.

Key words: 4H-SiC; buried-channel; MOSFET; field-effect mobility

PACC: 7340Q; 6170T

CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2004)12-1561-06

1 Introduction

4H- and 6H-SiC are attractive semiconductor materials for high-power and high temperature electron devices because they have excellent physical properties such as wide bandgap, high breakdown voltage, high thermal conductivity, and high saturation electron drift velocity. In addition, SiC has the advantage of a thermally grown native oxide, which provides the opportunity for its application in metal-oxide-semiconductor (MOS) devices.

With the improvement of SiC material quality and device process, the device research is expanding to analog and digital integrated circuits. Some monolithic nMOS and CMOS digital and analog integrated circuits have been demonstrated[1~3]. All SiC-based integrated circuits have been demonstrated to operate successfully at the temperature range from 573 to 673K. But, low channel mobility caused by SiO_2/SiC interface traps becomes one of the obstacles in the development of SiC MOSFET integrated circuits.

The bulk mobility of 4H-SiC is approximately twofold higher than that of 6H-SiC. Therefore, the 4H-SiC MOSFET is a promising candidate for a high-power switch device at high speed and low loss. However, the surface channel mobility of 4H-SiC MOSFET reported is extremely low[4]. It is believed that the high density traps at 2.9eV above the valence band edge at the SiO_2/4H-SiC interface lower the surface channel mobility[5]. One possible solution to raise the channel mobility is to keep electrons away from the SiO_2/4H-SiC interface. Some research groups reported that a buried channel structure can improve the channel mobility in 4H-SiC MOSFETs[6~8]. The highest reported channel field-effect mobility in a normally-off BC MOSFET of 140cm^2/(V·s) has been achieved. These results show that this structure of BC-MOSFET has important potential in high speed circuits. But there is no report about this kind of device to be

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Gao Jinxia female, was born in 1977, PhD candidate. Her current research interests are SiC MOS devices and circuits.

Zhang Yimen male, was born in 1941, professor, advisor of PhD candidate. He focuses on the research of device modeling and simulation in VLSI, VLSI CAD, quantum well devices and IC and high temperature microelectronics in wide band gap semiconductors.

Received 9 March 2004, revised manuscript received 21 June 2004 ©2004 The Chinese Institute of Electronics

achieved in our country so far.

The critical factors of affecting the characteristics of BC-MOSFET are channel doping concentration, channel depth, SiO_2/SiC interface quality, and the characteristics of metal-SiC ohmic contact. In this study, we have designed this kind of device and fabricated BC-MOSFETs with different channel length for the first time in our country. Some measurement results give us some important information for further studies.

2 Operation modes of BC-MOSFET

The SiC buried-channel n MOSFET is realized by implanting nitrogen into the surface of p-SiC. This implantation not only adjusts the threshold voltage, but significantly changes the operational characteristics of the device. Figure 1 shows a structural cross section of buried-channel MOSFETs. Depending on the bias conditions, the device can be worked in surface channel, buried-channel, surface-buried combined channel, and pinch-off modes.

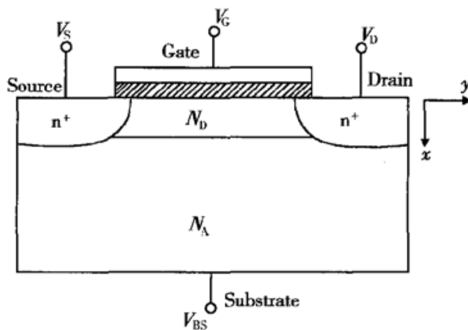

Fig. 1 Cross section of a typical buried-channel MOSFET device

With $V_{GS}-V_{FB}>V_{DS}$, where V_{GS}, V_{DS}, and V_{FB} are gate/source voltage, drain/source voltage, and flat-band voltage, respectively, the surface of the buried-channel MOSFET is in accumulation from source to drain, and in this case the buried-channel MOSFET operates in surface channel mode (as shown in Fig. 2(a)).

When V_{GS} is reduced such that $0<V_{GS}-V_{FB}<V_{DS}$, the surface is in partial accumulation/partial depletion (source is in accumulation and drain is in depletion), and the buried-channel MOSFET operates in surface-buried combined channel mode (as shown in Fig. 2(b)).

As V_G is reduced further, the surface depletion region will extend over the entire channel length. Under the condition, a true buried channel from the source to drain is formed, which is called buried-channel mode(as shown in Fig. 2(c)).

Further reduction in the gate voltage can lead to punch through between surface depletion layer and the depletion region of the metallurgical junction. Under such circumstances the buried channel becomes pinched off, which is called channel pinch-off mode (as shown in Fig. 2(d)).

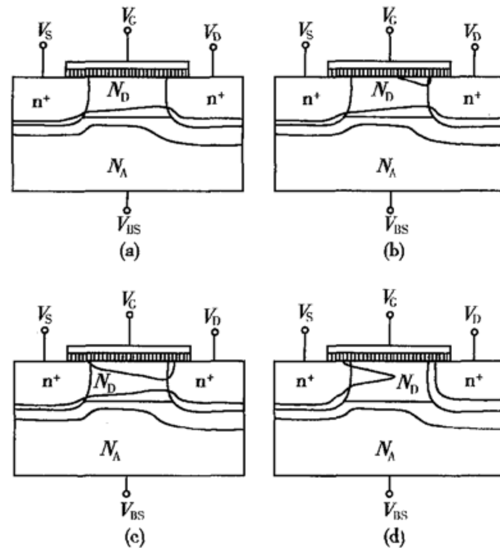

Fig. 2 Modes of operation for BC-MOSFET (a) Surface-channel mode: $V_{GS}-V_{FB}>V_{DS}$; (b) Surface-buried combined channel mode: $0<V_{GS}-V_{FB}<V_{DS}$; (c) Buried-channel mode: $V_{GS}-V_{FB}<0$; (d) Pinch-off mode

When a sufficiently negative gate voltage is applied, the density of the holes at the surface will exceed the doping density in implanted channel region and the surface region of the device can become inverted. The device cannot be turned off at a gate bias if surface inversion occurs before pinch-off. So the concentration and the depth of the chan-

nel must be designed carefully in experiment.

3 Device fabrication

BC-MOSFETs are fabricated on a 2μm thick, lightly doped p-type 4H-SiC epilayer with doping of $2.3\times10^{16}cm^{-3}$ grown on a heavily doped n^+ substrate. The channel width is 100μm. Source/drain regions and BC region are formed by multiple energy nitrogen ion implantations at room temperature, and the doses, energies, and simulated concentration profiles with Tsuprem 4 are shown in Fig. 3. Some parameters taken from Ref. [9] are referred to this simulation. We can see from Fig. 3 that the uniform impurity concentration of about $10^{17}cm^{-3}$ is obtained in the channel. The designed channel depth is about 0.2μm, but the actual channel depth should be less than 0.2μm after implant activation annealing, sacrifice oxidation, and gate oxidation. The implanted ions in the BC region and the source and drain regions have been activated simultaneously at 1600℃ for 30min.

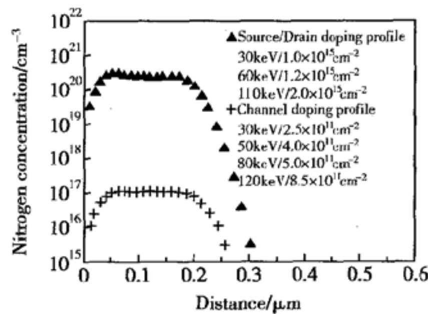

Fig. 3 Simulated ion implantation profiles for S/D regions and buried-channel region

Gate oxide layer growth has been done by thermal oxidation in dry O_2 atmosphere at 1200℃ for 140min. The thickness of the gate oxide is about 40nm. Ni metal layer with the thickness of 0.3μm has been deposited as the gate and the source/drain contacts and then annealed at 900℃ in vacuum for 30min. Finally, Ni/Pt/Au is formed. The total thickness of metal layers is about 1.5μm. A specific contact resistance of 1.7×10^{-4} $\Omega\cdot cm^2$ is obtained by the measurement with transfer length method structures.

4 Results and discussion

Figure 4 shows typical drain current-voltage (I_D-V_D) characteristics of the BC MOSFETs with channel length of 3μm and 5μm. Drain current in saturation region for 3μm and 5μm device increase obviously with drain bias, which may be caused by surface leakage current and channel length modulation effect. The threshold voltage of MOSFETs is determined by extrapolating the point of maximum slope on the I_D-V_G characteristics to the gate-voltage axis (the inset in Fig. 6). The threshold voltages are 1.73V and 1.72V for the gate lengths of 3μm and 5μm respectively. Positive threshold voltage indicates that the devices are operated in enhancement mode.

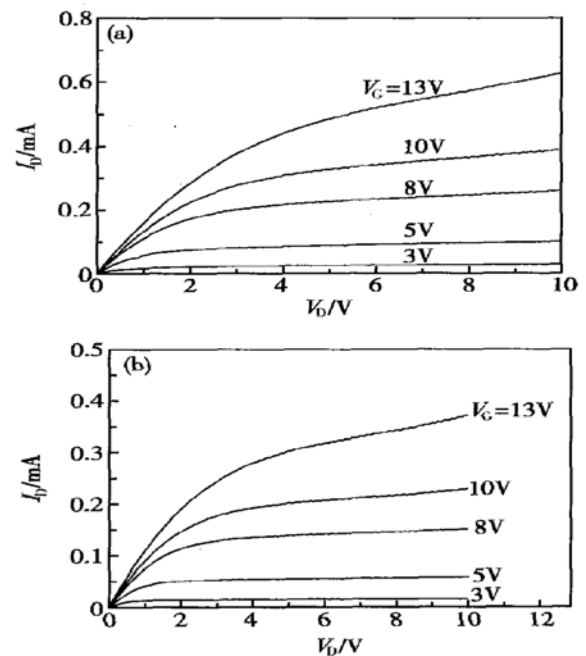

Fig. 4 I_D-V_D characteristics of the BC MOSFETs with channel length of 3μm (a) and 5μm (b)

Figure 5 shows the transfer characteristics and transconductance g_m at V_D= 10V in the saturation region for various gate lengths. For the gate lengths of 3μm and 5μm, the transconductances at V_G= 20V are 102 and 60μS, respectively.

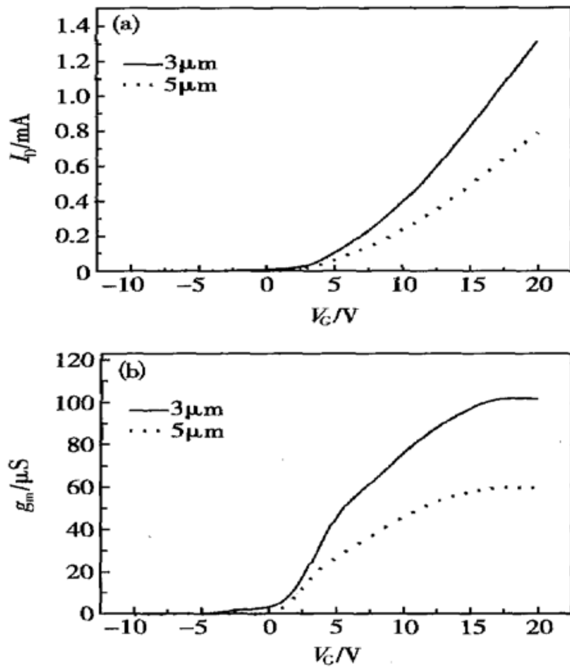

Fig. 5 (a) Transfer characteristics; (b) Transconductance g_m at $V_D = 10V$ in the saturation region for various gate length

A field-effect mobility (μ_{FE}) is usually calculated from the drain I_D-V_G curves at linear region with the following formula:

$$\mu_{FE} = \frac{\partial I_D}{\partial V_G} \times \frac{1}{C_{ox} V_D} \times \frac{L}{W} \quad (1)$$

But equation(1) is not suitable for BC MOSFET because the surface of device can enter into a number of states, such as inversion, depletion, and accumulation, and the calculations of drain current are different in each state. For obtaining a unitized expression, some simplification must be maken. The drain current in linear region is caculated from the following expression:

$$I_D = \frac{W}{L} \times \bar{\mu}_n V_{DS} \left[qN_D^+ x_i + \bar{C}(V_{GS} - V_{FB}) - \sqrt{\frac{2q\epsilon_s\epsilon_0 N_A^- N_D^+}{N_A^- + N_D^+} \times V_{bi}} \right] \quad (2)$$

where W and L are the channel width and length respectively, x_i is the channel depth, N_D^+ and N_A^- are ionized donor and acceptor impurity concentration. V_{bi} is built-in potential of the channel-substrate junction. $\bar{C}$ is the average capacitance, which can not be measured. When $V_{GS} - V_{FB} > 0$, the surface is in complete surface accumulation and $\bar{C} = C_{ox}$, C_{ox} is oxide capacitance. When $V_{GS} - V_{FB} < 0$, the surface is in complete surface depletion, and the capacitance is calculated from the following expression:

$$\bar{C} = \frac{C_{ox}}{\left[1 - \frac{2C_{ox}^2(V_{GS} - V_{FB})}{q\epsilon_s\epsilon_0 n_{n0}}\right]^{1/2}}$$

From Eq. (2), we can obtain the field-effect mobility:

$$\mu_{FE} = \frac{\partial I_D}{\partial V_G} \times \frac{1}{\bar{C} V_{DS}} \times \frac{L}{W} \quad (3)$$

The subthreshold and transfer characteristics at $V_D = 0.1V$ for 5μm device are shown in Fig. 6. The subthreshold slopes of 629mV/decade are obtained. We believe that the trapping of interface states plays an important role in the poor subthreshold characteristics. Figure 7 shows the field-effect mobility μ_{FE} as a function of gate voltage at $V_D = 0.1V$. The peak field-effect mobility is about 18.1cm^2/(V·s).

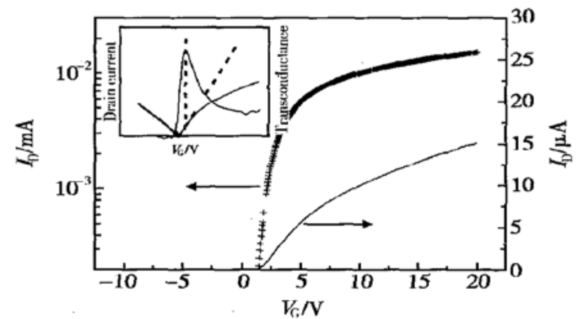

Fig. 6 Transfer characteristics at $V_D = 0.1V$ with a gate length of 5μm

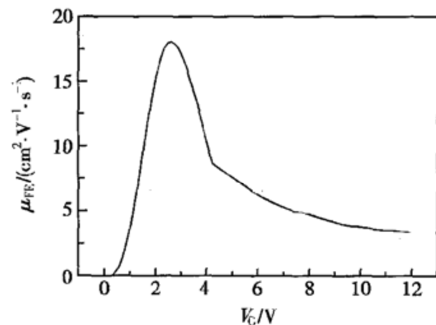

Fig. 7 Field-effect mobility μ_{FE} as a function of gate voltage at $V_D = 0.1V$ with a gate length of 5μm

Generally, for SiC inverted MOSFET, the field-effect mobility at low electric field is affected by the Coulomb scattering from the ionized impurities and the charges at interface states, and the field-effect mobility at high electric field is affected by the roughness scattering from the surface. But it is different for BC-MOSFET.

When a BC-MOSFET is biased into surface depletion, the channel is buried in the bulk between the surface depletion layer and the depletion region of the metallurgical junction, and the bulk constitutes the dominant conduction path. In this case, the Coulomb scattering from the ionized impurities has most important effect on field effect mobility. As the gate bias is increased, the edge of the channel moves to SiC/SiO_2 and the channel becomes thicker, which leads to the increase of carriers taking part in conduction and field-effect mobility.

As the surface is driven into accumulation, the conduction of electrons occurs both through the bulk portion of the channel and a surface accumulation-layer. The transport of electrons in the bulk is still dominated by Coulomb scattering from the ionized impurities. But in accumulation layer, the field effect mobility is also affected by following factors.

Firstly, in accumulation layer, the carrier concentration is always higher than the density of ionized impurities. As the gate bias is increased, the ionized dopants are quickly screened by the accumulated carriers allowing the carrier mobility to increase quickly before surface scattering effects begin to dominate.

Secondly, a large density of interface states exist on the SiC/SiO_2 interface, which increases rapidly with energy near the band edges. When the surface of the device is in accumulation, the Fermi level is located closer to the conduction band edge, where the density of interface states is very high. Under this condition, the effect of interface states should not be neglected. Interface states within the bandgap affect the transport of electrons in two distinct ways: on the one hand, some electrons in accumulation-layer will be trapped by interface states and become immobilized and only a fraction of electrons takes part in conduction; on the other hand, the drift of electrons in accumulation-layer will be affected by additional Coulomb scattering from the charged interface states.

Thirdly, the effect of carrier-carrier interactions becomes important as the carrier concentration increases to high level. The carrier concentration can be quite high even before the surface field becomes strong enough for surface roughness to become dominant.

Finally, as the gate electric field is increased to high values, surface roughness scattering becomes dominant. But it will have a very serious effect even in low or moderate field if the surface is very rough.

In our experiment, the sample is annealed at temperature of 1600℃ after drain/source implantation without any protection. At such temperature, silicon atoms evaporate preferentially from the SiC surface lattice and this severely roughens the surface. We have found that the surface is thickly dotted with little pit through magnification with microscope. The decrease of mobility caused by surface scattering will quickly offset the increase of mobility caused by the growing of carrier concentration in accumulation layer. So surface roughness scattering may be one of the most important factors of lowering the field effect mobility.

Moreover the field-effect mobility also is a function of source/drain parasitic series resistance, which is relative large due to larger specific contact resistance, lower activation of implantation dopant, and lower ionization rate at room temperature. Large source/drain parasitic series resistance also is one of the factors of causing low field-effect mobility.

5 Concolusion

It is believed that the low mobility in the 4H-SiC surface channel MOSFET is caused by the high

density traps near the band edge at the SiO_2/4H-SiC interface. For reducing the effects of interface states, buried channel MOSFETs with a thermally grown gate oxide on 4H-SiC is firstly reported in our country. The obtained peak field-effect mobility is about $18.1cm^2/(V \cdot s)$. The low field effect mobility may be caused by interface state near band edge, surface roughness, and S/D series resistance. The improvement of the field-effect mobility can be obtained by reducing the density of interface states, protecting the surface during implantion annealing, and improving the source/drain contact quality.

Acknowledgment The authors would like to thank Zhang Changjun and Prof. Feng Xianfeng in Xi′an University of Technology for high-temperature implantation activation annealing. And we also would like to thank Cui Zhandong in No. 13 Research Institute, China Electronics Technology Group Corporation for the experiment.

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4H-SiC 埋沟 MOSFET 的研制

郜锦侠　张义门　张玉明

(西安电子科技大学微电子研究所, 西安　710071)

摘要: 研制了 4H-SiC 热氧化生长氧化层埋沟 nMOSFET. 用室温下 N 离子注入的方法形成埋沟区和源漏区, 然后在 1600℃进行激活退火. 离子注入所得到的埋沟区深度大约为 0.2μm. 从转移特性提取出来的峰值场效应迁移率约为 $18.1cm^2/(V \cdot s)$. 造成低场效应迁移率的主要因素可能是粗糙的器件表面(器件表面布满密密麻麻的小坑). 3μm 和 5μm 器件的阈值电压分别为 1.73V 和 1.72V. 3μm 器件饱和跨导约为 102μS(V_G= 20V, V_D= 10V).

关键词: 4H-SiC; 埋沟; MOSFET; 场效应迁移率

PACC: 7340Q; 6170T

中图分类号: TN386　　**文献标识码**: A　　**文章编号**: 0253-4177(2004)12-1561-06

郜锦侠　女, 1977 年出生, 博士研究生, 现从事 SiC MOS 器件及电路研究. Email: jinxiag@mei.xidian.edu.cn

张义门　男, 教授, 博士生导师, 从事器件模型、VLSI 计算机辅助设计的教学和研究工作.

2004-03-09 收到, 2004-06-21 定稿

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