A Novel Barrier to Copper Metallization by Implanting Nitrogen into SiO_2*

ZHANG Guo-hai[1], XIA Yang[1], QIAN He[1], GAO Wen-fang[1], YU Guang-hua[2] and LONG Shi-bing[2]

(1 *Microelectronic R&D Center, The Chinese Academy of Sciences, Beijing 100029, China*)
(2 *Beijing University of Science and Technology, Beijing 100083, China*)

Abstract: The barrier to the copper diffusion is one of the key technologies in copper metallization. A novel barrier has been presented, which is a thin film of silicon oxynitride formed by implanting nitrogen into PECVD silicon dioxide. The method proved highly effective to block the copper diffusion after high frequency *C-V* measurements at different BTS (Bias Thermal Stress) conditions and the XPS (X-ray Photoelectron Spectroscopy) analysis. Furthermore, this method has the advantage of simplifying the damascene process of copper metallization, which has also been analyzed and discussed in detail.

Key words: ULSI; interconnection; copper; barrier
EEACC: 2220; 2550F
CLC number: TN405.97　　**Document code**: A　　**Article ID**: 0253-4177(2001)03-0271-04

1 Introduction

As the devices are continuously reduced in size, the RC delay of the ULSI interconnection system becomes one of the crucial limitations on IC performance. As a result, a more reliable metallization scheme is badly in need. Copper interconnect is a promising replacement for the conventional Al and its alloys[1]. However, owing to the importance of the interconnection of copper with contacting materials in multilevel metallization schemes, it should be demonstrated before its being utilized in certain applications. Typical dielectric materials such as silicon dioxide (SiO_2) are not effective barriers to copper diffusion[2]. Furthermore, any movement of copper into the substrate via drift or diffusion could degrade the leakage current of devices. Copper, a deep level dopant in silicon, can form several acceptor and donor levels within the forbidden band gap, which act as generation-recombination centers and can induce the leakage currents. So, the barriers to copper diffusion is a key technology in copper interconnection in ULSI.

In recent researches, the barriers to copper metallization can be divided into two categories, electric barriers and dielectric barriers. Some refractory metals and their nitrides as electric barriers, including Ta, W, TaN and TiN, have been extensively investigated[3,4]. Among these, Ta, having been reported to seed the growth of (111) Cu, has proved to provide an enhanced electromigration resistance as well as the improved adhesion and diffusion barrier properties. In addition, Ta is also found not easy to be removed by CMP (Chem-

* Project Supported by National Natural Science Foundation of China Under Grant No. 69936020.

ZHANG Guo-hai was born in 1975. He is currently a Ph. D candidate of Microelectronic R&D Center, The Chinese Academy of Sciences. His research interests are in the interconnections technology of ULSI.

Received 5 October 2000, revised manuscript received 29 November 2000
©2001 The Chinese Institute of Electronics

ical Mechanical Planarization). The overall IC-technology can be simplified if sufficient dielectric barriers are available[5]. PECVD silicon nitride has been reported to be an effective dielectric barrier to copper diffusion[6], though it is not very useful due to the high dielectric constant.

By implanting nitrogen into silicon dioxide, a thin film of silicon oxynitride is formed, which is the novel dielectric barrier to copper metallization we presented in this paper.

2 Experiment

Cu-gate MIS capacitors samples were fabricated on P-type silicon substrate (100) with ρ of 30 $\Omega \cdot$cm, as was illustrated in Fig. 1. First, 50nm SiO_2 was grown by PECVD at 280℃ to meet the requirements of low-temperature process in ULSI interconnections. Then, the samples were divided into two groups: A and B. With low implant energy of 10 keV and dose level of $3\times10^{15}cm^{-2}$, nitrogen was implanted into the 50nm SiO_2 film of samples A, which had been annealed at 400℃ in nitrogen for 30min to activate the implanted ions. For the sake of contrast, no nitrogen implantation nor thermal annealing were performed on samples B. Finally, 50nm Cu-dots with diameter of 1mm were formed by DC sputtering Cu onto all the samples in group A and B, with the DC sputtering power of 60W and at the Ar gas flow rate of 18.1sccm. At last, the fabrication of Cu-gate MIS capacitors was finished.

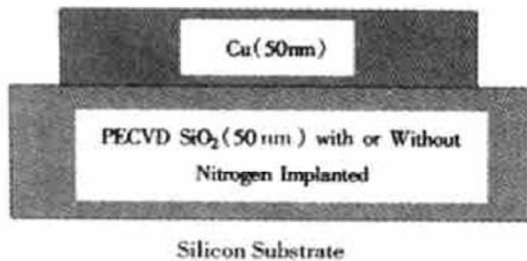

FIG. 1 Cross-Section of Samples

To investigate copper diffusion in PECVD SiO_2 with or without nitrogen implantation, the samples were characterized by high frequency C-V measurements at different BTS (Bias Thermal Stress) conditions. Besides, XPS (X-ray Photoelectron Spectroscopy) was carried out to analyze the thermal reliability of the dielectric barriers to copper diffusion.

3 Results and Discussion

3.1 C-V Measurements

The C-V measurements can quantify the dielectric charges in MIS (Metal-Insulator-Semiconductor) systems with high sensitivity. The dielectric bulk and interface charges can affect the surface inversion in the semiconductor substrate and thus the C-V characteristic is modified. Cu^+ drift in PECVD SiO_2 film with and without the nitrogen implanted will be evaluated by using BTS and C-V analysis, respectively.

The C-V shifts can be quantified by changing the flatband voltage, ΔV_{FB}. Uncompensated positive charge in the dielectric, Cu^+ as an example, makes V_{FB} more negative because it induces a negative image charge in the Si surface. To remove this image charge and restore the flatband condition, negative charges must be added on the gate. Hence, V_{FB} becomes increasingly negative as more positive charges are introduced into the dielectric. The amount of Cu^+ charges drifted into the dielectric can be estimated by measuring the flatband voltage shifts, ΔV_{FB}. Assuming that the Cu ions have drifted to the SiO_2/Si interface, the Cu^+ concentration per unit area, $[Cu^+]$, is[7]

$$[Cu^+] = -\frac{C_{OX}}{q}\Delta V_{FB}$$

where C_{ox} is the dielectric capacitance per unit area and q is the eletronic charge.

Table 1 shows a comparison of flatband shifts between the samples under different BTS conditions. It can be seen that under BTS of 10V, 200℃ and 5min, ΔV_{FB} of Cu/SiO_2/Si is much higher than the others, which demonstrates the pene-

tration of Cu^+ ions into PECVD SiO_2. When the bias voltage is − 10V, ΔV_{FB} becomes − 0.9V, which is much smaller than − 5.6V but higher than the others. This indicates that less Cu^+ ions are penetrated into PECVD SiO_2 due to the positve charge of Cu^+. When the PECVD SiO_2 film has been implanted with nitrogen, ΔV_{FB} becomes very low at BTS of ± 10V, 200℃ and 5min, which demonstrates that almost no Cu^+ ions have drifted to the insulator/Si interface. The PECVD SiO_2 film with nitrogen implanted is very effective to block the copper diffusion.

Table 1 ΔV_{FB} of Samples Under Different BTS Conditions

BTS (Bias Thermal Stress) Condition	10V, 200℃, 5min	− 10V, 200℃, 5min
Cu/SiO_2/Si ΔV_{FB}	− 5.6V	− 0.9V
Cu/SiO_2 (Nitrogen Implanted)/Si ΔV_{FB}	− 0.4V	− 0.2V

3.2 XPS Analysis Results

Special samples with 20nm copper film thicker than 50nm copper-dots have been fabricated, for the sake of convenience of XPS analysis. Figure 2 gives the results of XPS analysis on the samples with and without nitrogen implanted, which have been thermally stressed at 300℃ for 30 min. As for the samples without nitrogen implanted, copper ions can penetrate through the dielectric layer and some of them arrive at the silicon substrate, while no copper ions will drift to the insulator/Si interface if the PECVD SiO_2 film is implanted with nitrogen. The XPS analysis results are consistent with the results of *C-V* measurements above.

3.3 Discussion

Damascene process[8] is the conventional method in copper metallization because it can not only overcome the poor dry-etchability of Cu, but also achieve the global planarization, in which, interlevel dielectric is deposited; the trenches and pads are patterned by Reactive Ion Etching(RIE); and diffusion barriers (which are electric barriers conventionally) and Cu are deposited sequentially.

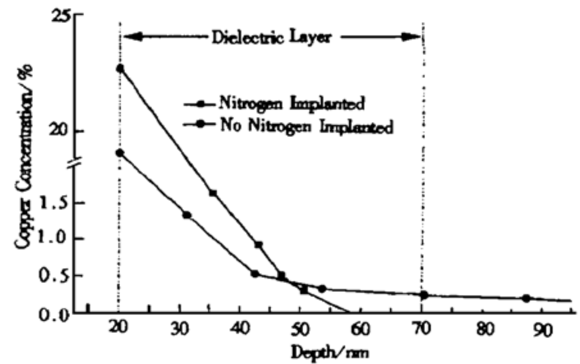

FIG. 2 XPS Analysis Curves of Copper Concentration Versus Depth After Stress of 300℃ for 30min

Then the excess Cu and barrier layers in the filled region are removed by CMP, as is no longer necessary if we use the dielectric barriers instead of electric barriers. If the silicon nitride or silicon oxynitride is deposited by PECVD to remove the excess dielectric layer at the bottom of the via and the dielectric layer of silicon oxynitride is formed by implanting nitrogen into SiO_2, only one mask is needed, so the process will be simplified greatly. The layer of silicon oxynitride will be formed selectively at the point where SiO_2 deposites (shown in Fig. 3). No silicon oxynitride exists at the bottom of the via, nor no more mask is needed, so the process can be simplified.

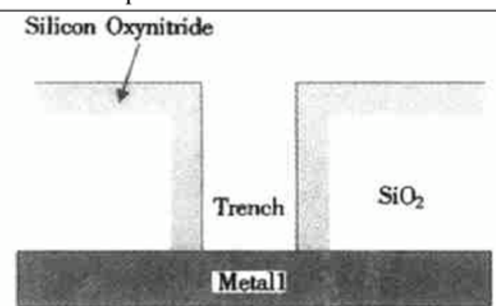

FIG. 3 Silicon Oxynitride Formed Selectively in Damascence Process

4 Conclusion

Copper interconnect is a promising replacement for the conventional Al and its alloys with the development of deep sub-micron integrated circuits. The fabrication of barrier to copper diffusion

is one of the key technologies in copper interconnection. A novel barrier was presented in this paper by implanting nitrogen into PECVD silicon dioxide and forming a thin film of silicon oxynitride. It has proved highly effective to block the copper diffusion after high frequency *C-V* measurements at different BTS conditions and the XPS analysis. If the novel barrier is adopted in the Damascene process, the process will be simplified by forming dielectric barrier layer selectively.

References

[1] Mehdi Moussavi, IEDM, IEEE 1999, 611—614.

[2] Y. Shacham-Diamond, A. Redhia, D. Hoffstetter *et al.*, J. Electrochem. Soc., 1993, **140**(8): 2427—2432.

[3] Changsup Ryu, Haehum Lee, Kee-Won Kwon *et al.*, Solid State Technology, April, 1999, 53—56.

[4] J. Baumann, T. Werner, A. Ehrlich *et al.*, Microelectronic Engineering, 1997, **37/38**: 221—228.

[5] M. Vogt, M. Kachel, M. Plotner *et al.*, Microelectronic Engineering, 1997, **37/38**: 181—187.

[6] M. Vogt, K. Drescher, Applied Surface Science, 1995, **91**: 303—307.

[7] Alvin L. S. Loke, Changsup Ryu, Patrick Yue *et al.*, IEEE Electron Device Letters, 1996, **17**(12): 549—551.

[8] Robert L. Jackson *et al.*, Solid State Technology, March, 1998, 49—59.

以注氮 SiO_2 作为铜互连技术中的新型阻挡层*

张国海[1] 夏 洋[1] 钱 鹤[1] 高文芳[1] 于广华[2] 龙世兵[2]

(1 中国科学院微电子中心, 北京 100029)

(2 北京科技大学, 北京 100083)

摘要: 采用给 PECVD SiO_2 中注入氮的方法, 形成一薄层氮氧化硅, 以此作为一种新型的扩散阻挡层. 不同热偏压条件下的 *C-V* 测试结果和 XPS 分析结果表明, 该方法能起到对铜扩散的有效阻挡作用.

关键词: 超大规模集成电路; 互连; 铜; 阻挡层

EEACC: 2220; 2550F

中图分类号: TN405.97 **文献标识码**: A **文章编号**: 0253-4177(2001)03-0271-04

* 国家自然科学基金资助项目(批准号: 69936020).

张国海 1975 年出生, 博士研究生, 主要从事 ULSI 互连技术研究.

2000-10-05 收到, 2000-11-29 定稿

©2001 中国电子学会