A Precise Model for Simulation of Temperature Distribution in Power Modules

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Abstract: The interaction between the active chips mounted and the same base plate is considered as a thermoelectrical coupling effect. An approach to coupling effect analysis of a multi-chip system is presented with IGBT as a sample. Finite element method is used to evaluate the temperature distribution in power modules. The precise electrothermal model is obtained by fitting the curve of transient thermal impedance with a finite series of exponential terms, in which, the thermal-coupling effect among chips is considered as a prediction of the highest transient temperature of the chips. This model can be used in many thermal monitoring systems. Both ANSYS and PSPICE simulation software have been employed, and the simulation results agree with the experimental ones very well.

1 Introduction

With the technology advancing, the characteristic dimension of semiconductor devices becomes smaller and smaller, so the electrical performance of power devices and the power electronic systems are greatly influenced by the temperature's rising inside the semiconductor devices. In order to protect the power devices, the temperature of devices should be monitored during the operation. Should any junction temperature in the device approach the critical value, immediate actions would be taken to reduce the dissipation. Much attention has been paid to the evaluation of increment in the temperature rising and the heat transmission. In previous works[1, 2] a good method has been proposed to monitor the chip temperature, namely on-line temperature measurement technique, which is based on the dynamical electrothermal model of a power device as well as its components. For this purpose, several models have also been established, including the normal model and the transformed one. The former, in the form of distributed RC equivalent network or the so-called "transmission line", has been widely used in some thermal simulators and can well demonstrate the coupling of the electrical and thermal phenomena in power devices, while the latter is with series connection of RC elements[1].

Mounted on a base plate, power devices can build large power modules, such as IGBT modules, as improves the handing capability and compactness of the power conversion system greatly. When the devices operate at the same time, the heat will influence the temperature of each chip. It is rather

complicated because of the interaction between the temperature rise and the heat transmission among the chips on the same base plate, that is to say, it is the most important to understand the interaction between them so as to establish a good electrothermal model.

Thermal coupling effects having been considered, an improved electrothermal model is presented in this paper as an on-line temperature monitor to calculate the chip temperatures of IGBT power modules. 3D finite element method is also used to calculate the temperature distribution. The curve of transient thermal impedance has been fitted with a finite series of exponential terms to obtain the precise electrothermal model, which applies to the circuit simulation software such as PSPICE, etc. Results from both the finite element numerical solution and the PSPICE simulation are in agreement with the measured ones. IGBT module (SKM 75 GB 123D) is the sample in the simulation and tests. An infrared camera has been used to measure the temperature.

2　Thermal Impedance and RC Parameters in Electrothermal Model

The transient thermal impedance curve of a power device is usually obtained by measuring the chip temperature under a constant power dissipation[2], which, however, may result in some uncertainty under different measuring conditions. In this work, by using the thermal simulation software ANSYS, the thermal distribution in a chip was obtained. The thermal impedance was then found as a function of time. In comparison with the experimental method, it is more convenient and relatively accurate. In this method, only the thermal behavior of the hottest spot at the chip center needs considering, because it can be regarded as the junction of the device[3].

With a constant power dissipation P, the time resolved temperature $T_{hot}(t)$ of the hottest spot in one chip can be obtained via a transient simulation.

The thermal impedance from junction to heatsink $Z_{th_{j-h}}(t)$ is then defined as

$$Z_{th_{j-h}}(t) = (T_{hot}(t) - T_{heatsink})/P \qquad (1)$$

With the transformed model with series connection of RC elements, we substitute $Z_{th_{j-h}}(t)$ into the equation

$$Z_{th_{j-h}}(t) = \sum_{i=1}^{n} R_i (1 - e^{\frac{-t}{R_i C_i}}) \qquad (2)$$

by using a curve fitting program to get the RC parameters[2]. Where R_i and $C_i (i = 1, \cdots n)$ are the elements in the transformed model. Number of the RC elements is decided according to the required accuracy of the model. The thermal resistance of one chip can be expressed as

$$R_{th_{j-h}} = \sum_{i=1}^{n} R_i \qquad (3)$$

It can also be obtained from $R_{th_{j-h}} = (T_{hot} - T_{heatsink})/P$ in a static simulation by using ANSYS.

3　Structure of IGBT Module

Three-dimensional structure model used in ANSYS simulation is based on the actual device layout. Figure1 shows the schematic structure of the concerned IGBT power module with two IGBT chips and two diode chips mounted on the same base plate. Because the length of each layer in any chip concerned is much bigger than its thickness, a carefully-made finite element mesh is necessary to get an optimum mesh size, with the aim of trading off the calculation precision, calculation time and storage space.

Two kinds of loads are used in the ANSYS simulation. One is the heat generation H, i. e. the density of power dissipation, which is defined as the power dissipation per unit volume of a chip heated actively; the other is the heat sink temperature at the bottom of the grease.

Static simulation was performed for IGBT and the diode in the module, respectively. The thermal resistance calculated from equation (3) is 0.49℃/W for IGBT and 0.78℃/W for diode.
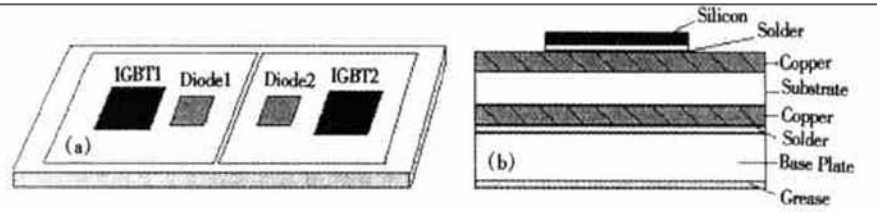
FIG. 1 Structure of IGBT Module (a) Schematic Structure of the IGBT Module; (b) Cross Sectional View of One Chip

Figure 2 shows a static temperature distribution in the power module when the constant power of 100W is dissipated by both IGBT 1 and diode 2 simultaneously. When the heat sink temperature keeps 0℃, the temperature of the hottest point in either IGBT 1 or diode 2 is higher than that when the same power is dissipated by only one of them. It demonstrates the thermal coupling effect among the chips. As the temperature rise can not be characterized by the normal electrothermal model, a new thermal model, considering the thermal-coupling effect, should be established to monitor the chip temperature.
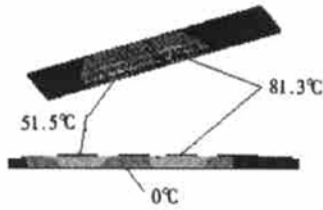

FIG. 2 Simulated Temperature Distribution in an IGBT Module

4 New Model

4.1 Calculation of Thermal-Coupling Effect Among Chips

Neglecting the convection and radiation, we can obtain a transition formula from the general heat conduction equation as follows:

$$\rho(x)c(x)\frac{\partial T(x,t)}{\partial t} - \mathrm{div}(K(x) \cdot \mathrm{grad}T(x,t))$$
$$= H(x,t) \qquad (4)$$

where x denotes the position vector (x,y,z). Normally, errors due to the non-linearity properties of

silicon are relatively small, thus specific heat $c(x)$, mass density $\rho(x)$, thermal conductivity $K(x)$ are regarded as independent on the temperature. Heat generation, $H(x,t)$, that depends on both the position and time, will change its overall strength with time instead of its spatial distribution. Therefore, equation (4) is linear.

Equation (5) is the solution of equation (4) when an arbitrary power dissipation $P(t)$ is applied on a chip[3].

$$T_{\mathrm{hot}}(t) = T_0 + \int_0^t P(\tau)Z_{\mathrm{th_{hot}}}(t-\tau)\,\mathrm{d}\tau \qquad (5)$$

where $T_{\mathrm{hot}}(t)$ is the hottest spot temperature of the concerned chip, T_0 is the heatsink temperature, $Z_{\mathrm{th_{hot}}}(t)$ is the time derivation of thermal impedance $Z_{\mathrm{th_{hot}}}(t)$.

If n independent power dissipation $P_i(t)$ ($i=1, 2, \cdots, n$) are applied on n chips of one power module, respectively, the hottest spot temperature of the j-th chip $T_{j\mathrm{hot}}(t)$ ($j=1, 2, \cdots, n$) can be written as below, because of the linear thermal system.

$$T_{j\mathrm{hot}}(t) - T_0 = \sum_{i=1}^n \Delta T_{j\mathrm{hot},i}(t) \qquad (6)$$

where $\Delta T_{j\mathrm{hot},i}(t)$ represents the hottest spot temperature rising on the j-th chip when the only power load $P_i(t)$ is applied on the i-th chip. According to equation (5), $T_{j\mathrm{hot},i}(t)$ is obtained from

$$T_{j\mathrm{hot},i}(t) = T_0 + \int_0^t P_i(\tau)Z_{\mathrm{th_{j\mathrm{hot},i}}}(t-\tau)\,\mathrm{d}\tau \quad (7)$$

where $Z_{\mathrm{th_{j\mathrm{hot},i}}}(t)$ is the time derivation of $Z_{\mathrm{th_{j\mathrm{hot},i}}}(t)$. $Z_{\mathrm{th_{j\mathrm{hot},i}}}(t)$ is defined as the thermal-coupling impedance from the i-th chip to the j-th chip. It is determined by $Z_{\mathrm{th_{j\mathrm{hot},i}}}(t) = (T_{j\mathrm{hot},i}(t) - T_0)/P_i$, where P_i is the constant power dissipated on the i-th chip.

For the module with n chips, there are $n \times n$ thermal-coupling impedances. When $i = j$, $Z_{th_{i}hot,i}(t)$ represents the thermal impedance of the i-th chip.

Therefore, equation (8) is obtained from (6) and (7)：

$$T_{jhot}(t) = T_0 + \sum_{i=1}^{n} \int_0^t P_i(\tau) Z_{th_{jhot,i}}(t - \tau) \mathrm{d}\tau \quad (8)$$

In the case of steady-state, there is no difference in the time domain. Equation (8) can be simplified to

$$T_{jhot} = T_0 + \sum_{i=1}^{n} R_{th_{jhot,i}} P_i \quad (9)$$

where $R_{th_{jhot,i}}$ expresses the thermal-coupling resistance from the i-th chip to the j-th one. Equation (9) can be also written as

$$
\begin{bmatrix}
\Delta T_{1hot} \\
M \\
\Delta T_{jhot} \\
M \\
\Delta T_{nhot}
\end{bmatrix}
=
\begin{bmatrix}
R_{th_{1hot,1}} & K & R_{th_{1hot,i}} & \Lambda & R_{th_{1hot,n}} \\
M & M & M & M & M \\
R_{th_{jhot,1}} & K & R_{th_{jhot,i}} & \Lambda & R_{th_{jhot,n}} \\
M & M & M & M & M \\
R_{th_{nhot,1}} & \Lambda & R_{th_{nhot,i}} & \Lambda & R_{th_{nhot,n}}
\end{bmatrix}
\cdot
\begin{bmatrix}
P_1 \\
M \\
P_i \\
M \\
P_n
\end{bmatrix}
$$

$$(10)$$

4.2 New Electrothermal Model

Transformed equivalent circuit with series connection of RC elements is used in the new electrothermal model with thermal-coupling effects considered. The equivalent circuit structure obtained from equation (8) is shown in Fig. 3. The voltage of node 1 represents the temperature of the hottest spot in the j-th ($j = 1, 2, \cdots, n$) chip. Current source represents the power dissipation in each chip. Voltage source represents the temperature of heatsink. There are n equivalent circuits having the similar structures to that shown in Fig. 3, presenting the thermal features of n concerned chips, respectively.

In our case, four chips are mounted on the IGBT power module. Due to the symmetric effect, two equivalent circuits are enough to present the thermal features of IGBT and diode. The new electrothermal model of IGBT1 is shown in Fig. 4. Seven pairs of RC elements are applied to fit the thermal impedance of IGBT1 and thermal-coupling
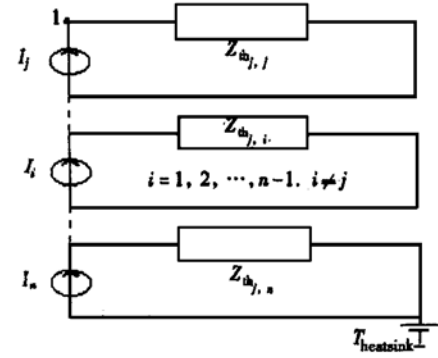

FIG. 3   Equivalent with Thermal.

impedance from diode1 to IGBT1, as well as 3 pairs of parameters to fit other thermal coupling effects.
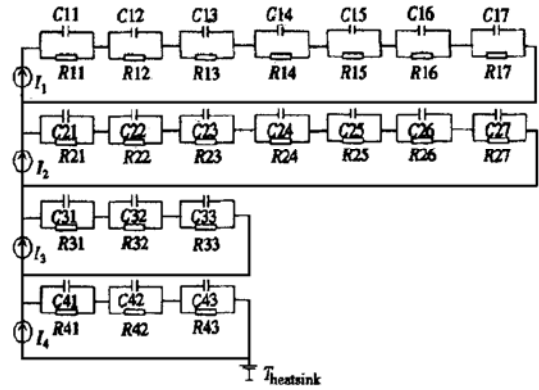

FIG. 4   Electrothermal Model of IGBT1

4.3 Simulation and Results

Based on the structure model with the grease thickness of $70\mu m$, 16 thermal coupling resistors are obtained from the static simulation on the IGBT power module, as is shown in Table 1. According to the symmetric effect, there are eight different coupling resistor values. Equation (10) and the parameters in Table 1 are used to calculate the hottest temperature of each chip. For example, the power dissipations of 27W and 23W are applied in IGBT1 and diode2, respectively. The heatsink temperature T_0 keeps $24℃$. Simulation results show that the hottest temperatures of IGBT1 and diode2 are $37.893℃$ and $42.584℃$, respectively, while the calculation results are $37.90℃$ and $42.58℃$. They coincide with each other well. It is easy to evaluate the static thermal-coupling effects with equation

(9) or (10).

Table 1 Thermal-Coupling Resistance of IGBT Module

$R_{1,hot1}$/(℃·W⁻¹)	0.4936	$R_{1hot,2}$/(℃·W⁻¹)	0.077	$R_{1hot,3}$/(℃·W⁻¹)	0.0252	$R_{1hot,4}$/(℃·W⁻¹)	0.0071
$R_{2hot,1}$/(℃·W⁻¹)	0.0681	$R_{2hot,2}$/(℃·W⁻¹)	0.7814	$R_{2hot,3}$/(℃·W⁻¹)	0.0886	$R_{2hot,4}$/(℃·W⁻¹)	0.0225
$R_{3hot,1}$/(℃·W⁻¹)	0.0225	$R_{3hot,2}$/(℃·W⁻¹)	0.0886	$R_{3hot,3}$/(℃·W⁻¹)	0.7814	$R_{3hot,4}$/(℃·W⁻¹)	0.0681
$R_{4hot,1}$/(℃·W⁻¹)	0.0071	$R_{4hot,2}$/(℃·W⁻¹)	0.0252	$R_{4hot,3}$/(℃·W⁻¹)	0.077	$R_{4hot,4}$/(℃·W⁻¹)	0.4936

An infrared camera is used to monitor the hottest temperature of each chip mounted on the open IGBT module. Different constant power losses are applied on IGBT 1. The temperature rises of each chip with power losses are shown in Fig. 5. The curves are proximately linear. The slope of curve T-IGBT 1 is the thermal resistance of IGBT 1 and the slopes of other curves represent the thermal-coupling resistance from IGBT 1 to their respective devices. Table 2 shows the comparison between the simulation results and the tested ones when the power losses of 100W and 70W are dissipated on IGBT 1 and diode1, respectively. The simulation results in Table 2 are based on the structure model with grease thickness of $200\mu m$.
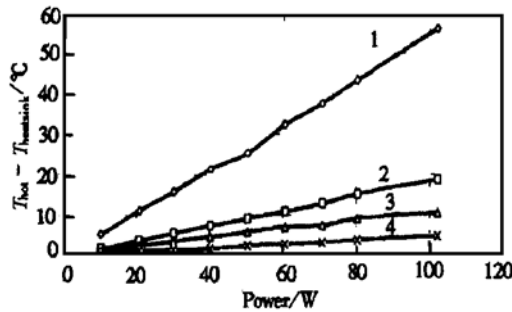

FIG. 5 Measurement Results of Middle Point in Every Chip with Different Power Losses Applied on IGBT 1

Table 2 Comparison Between Simulation and Test Results

	IGBT 1		Diode1		Diode2		IGBT 2	
	Simu	Meas	Simu	Meas	Simu	Meas	Simu	Meas
Power Losses/W	100	102.3	0	0	0	0	0	0
ΔT/℃	60.1	58.2	16.8	18.7	8.59	10.5	4.5	4.8
Power Losses/W	0	0	70	72	0	0	0	0
ΔT/℃	13.1	13.2	62.6	63.5	14.5	14.6	6.8	6.5

The errors are mainly due to the non-uniform grease thickness between the case and the heatsink. In practice, it is difficult to evaluate the grease thickness and the grease can not be pasted as evenly as that applied in simulation. During the simulation, the hottest point is in the middle of the chip and the temperature distribution is only decided by the thermal effect. However, in practical operation, the chip temperature is also influenced by the device structure, existing defects in silicon, and electric field, etc. Besides, some errors are caused by the different boundary and the ambient conditions between the simulation and measurement.

Transient analyses are also done on the IGBT module. By using the methods above, the electrothermal models of both IGBT and diode with thermal-coupling effects considered have been established. The RC parameters are also obtained by fitting the coupling impedance curves. The fitting correlation coefficient ρ is bigger than 0.997. Then electrothermal model can be implemented in PSPICE to simulate the junction temperature waveform at a given power.

For example, the rectangular power pulse with the amplitude of 100W and duty cycle of 1s is alternately applied on IGBT 1 and diode1, i. e. IGBT 1 turns on but diode1 turns off during one cycle. The heatsink temperature is 0℃. Figure 6 shows the variation in temperature of the hottest point on IGBT 1 that are obtained from ANSYS and PSPICE simulation, respectively. Curve 1 represents the results of PSPICE using normal thermal model without considering the thermal-coupling effect, while curve 3 is that using a new thermal model. Curve 2 is the results of ANSYS. The values from curve 3 and curve 2 agree with each other very well and are both higher than that from curve 1. The electrothermal model with thermal coupling effect considered is much accurate compared with those mul-

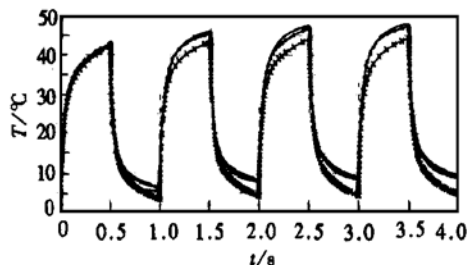ti-chip module applications. A rising trend is observed in the curve after each cycle to get its static state.

FIG. 6   Transient Simulation results

5   Conclusion

Finite element method is used to discuss the thermal-coupling effects in a multi-chip system. A precise electrothermal model has been obtained with the thermal-coupling effect having been considered among the chips, which applies to kinds of thermal monitoring systems. For example, it can be easily transferred in micro-controller by means of the delay element model[4], therefore, the junction temperature of the device can be determined on-line.

Because of the limitation of data storage space and long time needed in the calculation, it is difficult to get the solutions with long time evolution by using ANSYS. It is expected to use the numerical method to set up a good thermal model and then use PSPICE to get the dynamic results.

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一种用于功率模块热分布特性研究的精确模型

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摘要: 应用有限元法, 对一个 IGBT 功率模块的三维热分布进行了仿真研究, 提出了通过 ANSYS 仿真建立热模型的基本方法, 进而探讨了功率模块上各芯片之间的热耦合关系, 提出了考虑热耦合效应在内的功率模块热模型的统一结构, 基于对瞬态热阻抗曲线的拟合, 获得了热模型的相关参数, 从而建立了热耦合模型. 该模型可方便地应用于电路仿真软件如 PSPICE 中, 仿真结果与有限元计算结果一致, 并与实际测量值相符.

关键词: 功率电子; IGBT 模块; 热仿真; 热耦合

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