Characteristics of Refractory Metal Gate MOS Capacitor with Improved Sputtering Process for Gate Electrode

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Abstract: The technique to improve the performance of W/TiN stacked gate MOS capacitor with 3nm gate oxide is reported by optimizing the sputtering process of a refractory metal gate electrode and adopting a proper anneal temperature to eliminate the damages. Specific methods involved in the optimization of sputtering process include: selecting a proper TiN thickness to reduce stresses; using a smaller sputtering rate to suppress the damages to gate dielectric and adopting a higher N_2/Ar ratio during the TiN sputtering process to further nitride the gate dielectric. With these measures, excellent *C-V* curves are obtained and surface state density (N_{ss}) is successfully reduced to below $8\times10^{10}cm^{-2}$, which is comparable to the polysilicon gate MOS capacitor.

Key words: sub-0.1μm regime; refractory metal gate; sputtering process; surface states

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1 Introduction

Continued scaling of MOSFET gate lengths to sub-0.1μm regime and gate oxide thickness to 3nm below has encountered a series of problems such as high gate resistance, boron penetration, polysilicon gate depletion and increasing gate tunnel leakage[1]. The refractory metals, especially W/TiN, become the preferred candidates for gate electrode to solve these problems[2]. Sputtering deposition of the metal gate electrode is more favorable than CVD for the conventional CMOS process, because the impurity contained in the CVD metal degrades the gate dielectric reliability during a high temperature annealing process[3]. The surface damage of the gate dielectric during the sputtering deposition, however, is one of the major problems[4—5]. Therefore, to reduce the N_{ss} becomes the key to improve the performance of metal gate MOS. In this work, investigations are made into the W/TiN stacked gate MOS capacitors with 3nm gate oxide under various sputtering conditions. Since TiN affects the gate dielectric most, TiN sputtering conditions are therefore mainly optimized in the experimental process, where the comparisons are made between different sputtering rates and different TiN thickness. Besides, comparison is also made between different anneal temperatures to reveal its effect on the recovery of the damage in the thin gate oxide.

2 Experiments

W/TiN stacked gate electrode MOS capacitors on both p-type and n-type silicon substrates are fabricated. The TiN is deposited by the reactive sputtering with the mixture of N_2 and Ar on the

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3nm oxynitride gate dielectric in a DC magnetron sputtering system. The thickness of TiN varies from 20nm to 50nm and the sputtering rate varies from 2.2nm/min to 8.6nm/min. The next 100nm-thick W is deposited by the normal sputtering, which is in the same DC magnetron sputtering system. When the stacked gate is etched, a furnace anneal is performed with the anneal temperature varying from 380℃ to 450℃. N^+ polysilicon gate MOS capacitors are also prepared to compare with the metal gate MOS capacitors.

3 Results and Discussion

The high frequency C-V curves in Fig. 1 show the different characteristics of p-substrate W/TiN gate MOS capacitors with W thickness keeping

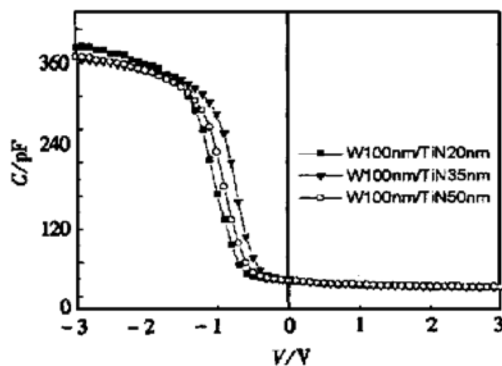

FIG. 1 C-V Characteristics of p-Substrate W/TiN Gate MOS Capacitors with W Thickness Keeping 100nm and TiN Thickness Varying from 20nm to 50nm

100nm and TiN thickness varying from 20nm to 50nm. It can be seen that the C-V characteristics of the MOS capacitors are improved when the TiN thickness is 35nm, as can be explained as follows: When the double layer of the metal combination is 100nm W + 35nm TiN, the stacked gate structure will undertake the smallest stress, the gate dielectric receive the lightest effect and N_{ss} decline to a satisfactory low value. The relationship between TiN thickness, N_{ss} and stress is illustrated in Fig. 2, as confirms the fact seen in Fig. 1 that TiN thickness of 35nm combining 100nm-thick W is the best choice. Figure 3 explains the effect of different TiN sputtering rates on the C-V curves. This experiment is conducted under the condition of a smaller RF power and a higher N_2/Ar ratio that

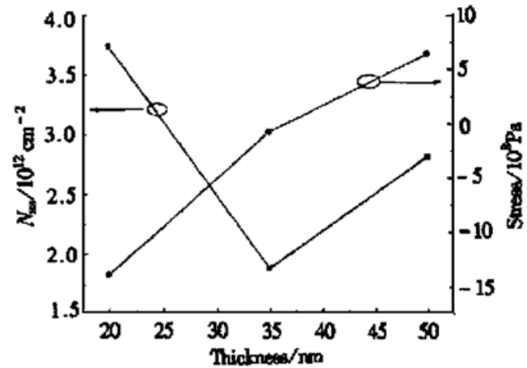

FIG. 2 Relationship Between TiN Thickness, N_{ss} and Stress, in which the Stacked Gate Structure being 100nm W + 35nm TiN

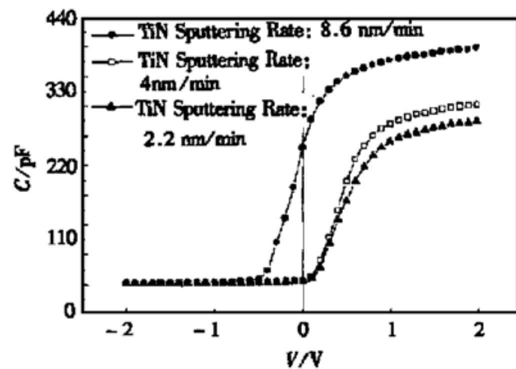

FIG. 3 Tendency of n-Substrate MOS Capacitor C-V Curves Changing at Different TiN Sputtering Rate

leads to a smaller sputtering rate. TiN is deposited slowly so as to reduce the damage to the gate dielectric. With the sputtering rate decreasing from 8.6nm/min to 4nm/min, the C-V curve of the capacitor moves in the positive direction. The decrease in N_{ss} is the main cause of this result, which has less damage to the gate dielectric. When the sputtering rate is reduced to 2.2nm/min, a better result is got. Dangling bonds are generated in the gate dielectric during the sputtering deposition of the metal gate[6]. But with the increase of N_2/Ar ratio, they will be terminated because of the nitri-

dation on the dielectric surface during the sputtering deposition[7]. At the same time, a higher N_2/Ar ratio helps to reduce the resistivity of TiN[8]. Figure 4 represents the relationship between the furnace anneal temperature and C-V curve. During the

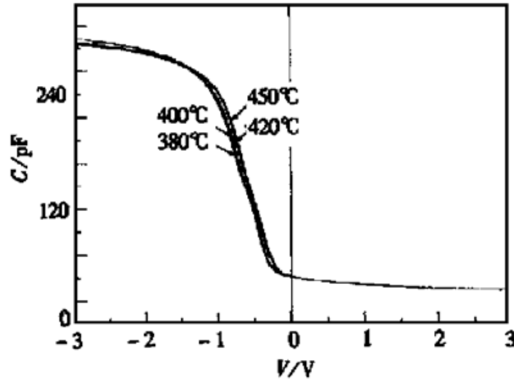

FIG. 4 Effect of Different Furnace Anneal Temperature on C-V Curves of p-Substrate W/TiN Stacked Gate MOS Capacitors

reactive sputtering, the electron and X-ray will induce some surface states[9], most of which can be recovered after a furnace anneal at 380℃ for 30min in the forming gas. When the anneal temperature is increased to 420℃, the N_{ss} value is the same as that of the polysilicon gate MOS capacitors. And inspiringly, as shown in Fig. 5, 450℃ 30min furnace anneal can reduce N_{ss} value to below $8\times10^{10}\text{cm}^{-2}$. Figure 5 also indicates the relationship between the furnace anneal temperature and V_{fb}. With the rising of anneal temperature, N_{ss} value will decline and hence, the V_{fb} value will move in the positive direc-

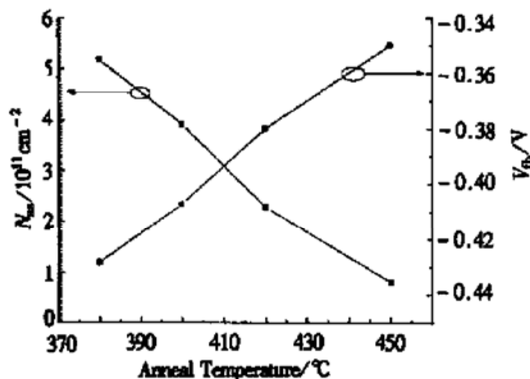

FIG. 5 Tendency of N_{ss} and V_{fb} with the Increase of Furnace Anneal Temperature

tion. In Fig. 6, the C-V curve of W/TiN stacked gate MOS capacitors is compared with that of polysilicon gate MOS capacitors. Through comprehensive optimization of the sputtering process and properly increasing furnace annealing temperature, the C-V characteristics of W/TiN stacked gate MOS capacitors are good and even better than that of the polysilicon gate.

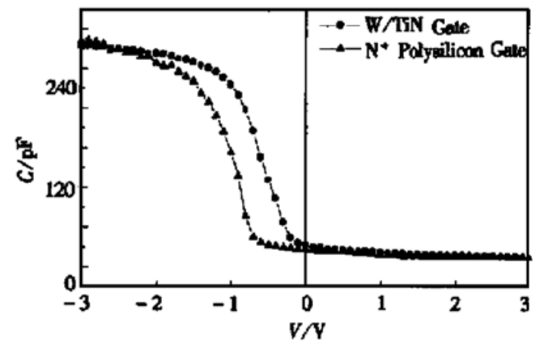

FIG. 6 Comparison of C-V Curves Between W/TiN Stacked Gate MOS Capacitor and n^+ Polysilicon Gate MOS Capacitor

4 Conclusion

This experiment demonstrates the process of improving the performance of deep sub-micron W/TiN gate MOS in detail. Firstly, it is necessary to select a bi-layer metal gate in proper thickness to reduce the stress of the stacked gate structure. Then, a smaller sputtering rate is adopted to deposit TiN that is directly connected with the gate dielectric. Besides, to select a relatively high N_2 percentage in N_2/Ar gas mixture is helpful to the further nitridation of gate dielectric during TiN sputtering deposition to terminate the dangling bonds. At last, the surface states should be recovered at a proper furnace anneal temperature. In this experiment, N_{ss} value is successfully reduced to 8×10^{10} cm^{-2} below, which is even better than that of the polysilicon gate. As a result, the problems, such as high surface state density and serious gate leakage in the deposition of metal gate electrode by PVD, can be solved, as paves the way for the fabrication of deep sub-micron metal gate CMOS devices.

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优化了栅电极溅射工艺的难熔金属栅MOS电容的性能

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摘要: 论述了通过优化难熔金属栅电极的溅射工艺及采用适当的退火温度修复损伤来提高3nm栅氧W/TiN叠层栅MOS电容的性能. 实验选取了合适的TiN厚度来减小应力, 以较小的TiN溅射率避免溅射过程对栅介质的损伤, 并采用了较高的N_2/Ar比率在TiN溅射过程中进一步氮化了栅介质. 实验得到了高质量的*C*-*V*曲线, 并成功地把N_{ss}(表面态密度)降低到了$8\times10^{10}/cm^2$以下, 达到了与多晶硅栅MOS电容相当的水平.

关键词: 亚0.1μm代; 难熔金属栅; 溅射工艺; 表面态

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