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Fabrication of Enhancement Mode GaN Metal-Insulator-Semiconductor Field Effect Transistor*

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Abstract The enhancement mode GaN metal-insulator-semiconductor field effect transistor (E-MISFET) is successfully fabricated on a GaN/AlGaN/GaN double heterojunction structure with SiO_2 as the insulator layer. The enhancement mode DC characteristics have been first achieved in the device with the gate-length of 6μm, 10μm and gate-width of 100μm. The device with gate-length of 6μm shows the DC transconductance of 0.6 mS/mm and the maximum drain-source current of 0.5mA. The gate leakage current is lower than 10^{-6}A at the bias of −10V while the gate breakdown voltage is higher than 20V. This result proves the presence of a piezoelectric field in the heterojunction, the strongly asymmetric band bending and the carriers distribution caused by the piezoelectric field.

Key Words: GaN, MISFET, Piezoelectric
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Recently, a number of papers on GaN-based field-effect transistors (FETs) have been reported. The metal-insulator-semiconductor technology is widely adopted in many applications since it can provide the high DC input impedance, large gate voltage swings, normally-off operation with high source-drain blocking voltage, and high-temperature operation because of the reduced gate leakage, comparing with that of a conventional metal semiconductor FET (MESFET). Ren *et al.*[1] have demonstrated a GaN MISFET which working under depletion mode with $Ga_2O_3(Gd_2O_3)$ as the gate insulator layer. Analysis on the effect of temperature on the device shows that the gate leakage current is significantly

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reduced at an elevated temperature compared with a conventional MESFET fabricated on the same GaN layer.

Deposited Si_3N_4 has also been used as a gate insulator in GaN MISFET fabrication[2]. Using plasma-enhanced chemical vapor deposition (PECVD) to deposite SiO_2 on a GaN layer, we can obtain a very good MIS capacitor with low interface state density and an excellent high-frequency capacitance-voltage (C-V) characteristic[3], which is same as other reports[4]. However, for a semiconductor with a wide energy gap, the generation of minority carries in the deep depletion region of the MIS capacitor would be extremely slow. In a GaN MIS capacitor it would take about 10^{11} years[4]. Therefore, to obtain an inversion channel is very difficult in a GaN MISFET with conventional device structure, and even can not work under the enhancement mode.

In this paper, we demonstrate an enhancement mode GaN-based MISFET on the GaN/AlGaN/GaN double heterojunction with the PECVD-grown SiO_2 as the gate insulator. The DC measurements show this device is of a good output and pinch-off characteristic with a transconductance of 0.6mS/mm and a maximum drain-source current of 0.5mA. The gate leakage current is lower than 10^{-6}A (the limit of the measurement equipment) as the bias of -10V while the gate breakdown voltage is higher than 20V.

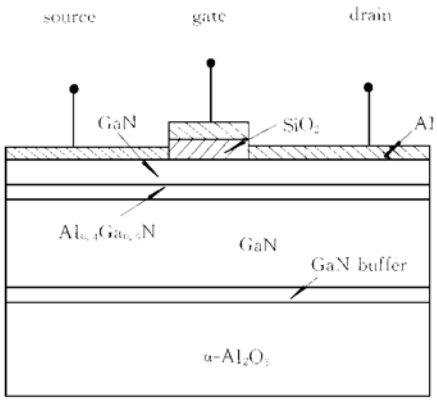

FIG. 1 Schematic Illustration of Device Structure

The GaN and AlGaN were grown on the c-Al_2O_3 substrates in a metalorganic chemical vapor deposition (MOCVD) with a horizontal reactor. The MISFET structure in this study includes, from the bottom, 30nm GaN buffer, 1.4μm GaN, 100nm $Al_{0.4}Ga_{0.6}N$, 100nm GaN. All of the layers were undoped. Finally, a 100nm SiO_2 layer was deposited on the surface of the top GaN by PECVD. The electron concentration of the GaN layers is about 2×10^{17} cm^{-3} from C-V measurement. The devices have the gate lengths of 6μm or 10μm and gate width of 100μm. Al was evaporated on the top GaN layer and annealed at 500℃ for 20 minutes in nitrogen for the ohmic contacts, and on the gate SiO_2 layer for the gate contact. The device structure is illustrated in Fig. 1.

It was known that the piezoelectric effect by lattice-mismatch-induced strain was very important for a III-V nitride heterojunction structure. Bykhovski *et al.*[5] had studied the piezoelectric properties on a GaN/AlN/GaN structure in details, and demonstrated that the strain-induced electric fields could shift the flat band voltage and produce an accumulation region on one side and a depletion region on the other side of AlN. The direction of electric fields depends on the types of atomic plane at the heterointerface (Ga or N). The band bending induced by piezoelectric field is shown in Fig. 2. Later studies[6,7]

have proved that the piezoelectric field produces a sheet electron concentration in the order of 10^{12}~ $10^{13}cm^{-3}$, corresponding the electric field in the order of 10^5~ 10^6V/cm which will strongly affect the band bending.

The DC output characteristic measurements of our devices were performed by some meters. The gate bias is from 0V to − 10V, by step − 1V. The gate leakage current is lower than 10^{-6}A at the bias of − 10V (the limit of the measurement) and the gate breakdown voltage is higher than 20V. The output characteristic is shown in Fig. 3. This figure shows a very good output and pinch-off characteristics of the device with a gate length of 6μm. The transconductance is 0.6mS/mm and the maximum drain source current 0.5mA. Supposing the gate length is 6μm in our device, its transconductance value is approaching 5mS/mm with a gate length of 1μm as reported by Ren[1]. The pinch-off characteristic begins to emerge at the gate bias of − 4V which indicates that a P-channel appears.

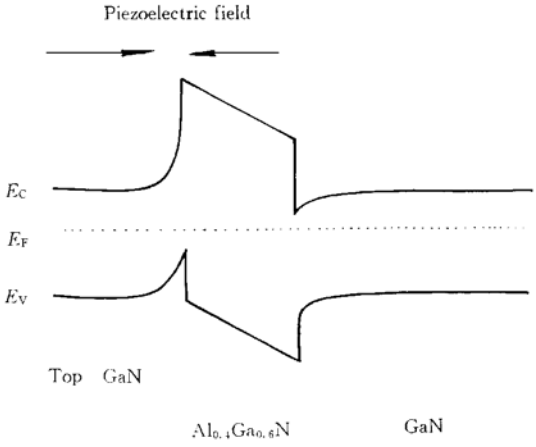

FIG. 2　Schematic Illustration of Band Bending Induced by Piezoelectric Field

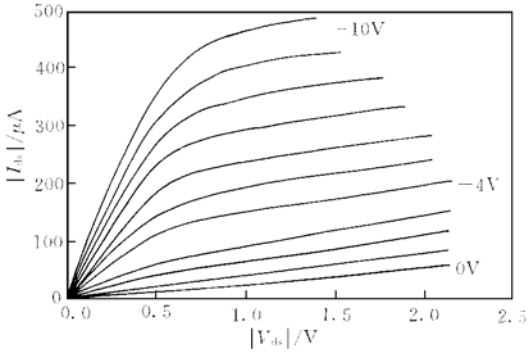

FIG. 3　Output Characteristic of a Device with a Gate Length of 6μm

Ramvall *et al.*[8] have reported the carrier distribution on a MOCVD-grown GaN/$Al_{0.14}Ga_{0.86}N$/GaN double heterojunction structure that is similar to that of our sample. The experimental results reveal the depletion region on the top GaN layer and the directions of electric field (E_P), which prove the existance of a hole well around the interface as that of the Ref. 1 and Fig. 2. These results are in good agreement with our experimental results.

Summary, an enhancement mode GaN-based MISFET on a GaN/AlGaN/GaN double heterojunction with PECVD-grown SiO_2 as the gate insulator was first demonstrated. The DC characteristic show this device has good output, pinch-off characteristic and a transconductance of 0.6mS/mm with the maximum drain-source current of 0.5mA. The gate leakage current is lower than 10^{-6}A (the limit of the measurement) at a bias of − 10V and the gate breakdown voltage is

higher than 20V. The presence of P-channel is the result of the strongly asymmetric band bending and carrier distribution induced by the strain-induced piezoelectric field.

References

[1] F. Ren, M hong, S. N. G. Chu, M. A. Marcus, M. J. Schurman, A. Baca, S. J. Pearton and C. R. Abernathy, Appl. Phys. Lett., 1998, **73**(26): 3893.

[2] S. C. Binari, L. B. Rowland, G. Kelner, W. Kruppar, H. B. Dietrich, K. Doverspike and D. K. Gaskill, in 1994 Int. Sym. Compound Semiconductors Proc., ed. by H. Goronkin, IOP Publishing, Bristol, 1995, p. 459.

[3] P. Chen *et al.*, "The High-frequency Capacitance-voltage Behavior of PECVD Grown SiO_2/n-GaN in Deep Depletion" (unpublished).

[4] H. C. Casey, Jr., G. G. Fountain, R. G. Alley, B. P. Keller and Steven P. DenBarrs, Appl. Phys. Lett., 1996, **68**(13): 1850.

[5] A. Bykhovski, B. Gelmont and M. Shur, J. Appl. Phys., 1993, **74**(11): 6734.

[6] S. C. Binari, J. M. Redwing, G. Kelner and W. Kruppa, Electron. Lett., 1997, **33**: 242.

[7] J. M. Redwing, M. A. Tischler, J. S. Flynn, S. Elhamri, M. Ahoujja, R. S. Newrock and W. C. Mitchel, Appl. Phys. Lett., 1996, **69**(7): 963.

[8] P. Ramvall, Y. Aoyagi, A. Kuramata, P. Hacke and K. Horino, Appl. Phys. Lett., 1999, **74**(25): 3866.