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High-Speed CMOS Sample-and-Hold Amplifier

WU Ge(兀 革) and SHI Yin(石 寅)

(*Institute of Semiconductors, The Chinese Academy of Sciences, Beijing* 100083, *China*)

Abstract: A newly designed sample-and-hold(S/H) integrated circuit based on the 1.5 micron N-well CMOS technology for 8-bit high-speed analog to digital converter is described. It can realize the 40-MHz sampling rate and 8-bit resolution. The good performance of S/H circuit benefits from the use of a newly designed regulated cascode operator amplifier, which has a DC gain of 140-dB, unity-gain bandwidth of 407-MHz, phase margin of 53 degree and power consumption of 90mW. It is superior to the operator amplifier of 60-dB, 107-MHz, 13 degree, and 33mW respectively, which is used in the similar S/H circuit based on the 0.8 micron technology and designed by Michio Yotsuyanagi.

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1 Introduction

The sample-and-hold (S/H) circuit is a key module for many applications[1] to transform a continuous time signal into discrete one. In analog to digital (A/D) converters, the front-end of the S/H amplifier must be of both high speed and high linearity with low dissipation. For the A/D converter we designed, a S/H circuit based on the 1.5μm CMOS technology is needed with 8-bit resolution and 40-MHz sampling rate. No such a design, which meets all the requirements, has been reported only a few circuits meet some of the requirements[2—4], though all of them are designed with advanced technology (0.8μm, 0.5μm and BiCMOS technology). However, there exists a gap between the home technology and abroad one. If S/H circuits are fabricated with home technology (1μm or 1.5μm) without any improvement, the performance will degrade and can not meet our requirement any more.

In this paper, an improvement has been made in the S/H circuit based on the 0.8μm

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WU Ge (兀 革) was born in 1971. She received the Ph. D degree at Institute of Semiconductors, The Chinese Academy of Sciences in 2000. Her research interests are high-speed analog integrated circuits design.

SHI Yin(石 寅) was born in 1950. His current position is professor of microelectronics, tutor of doctoral postgraduate. His research interests include high speed analog integrated design and analog to digital mixed integrated circuits design.

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technology[4] to realize an 8-bit 40-MHz sampling rate based on 1.5μm CMOS technology. The key component op-amp used in the S/H circuit is substituted by a newly designed one. Simulation results from the newly designed op-amp and the S/H circuit based on 1.5μm CMOS technology are discussed.

2 Sample-and-Hold Circuit

According to the required performance of A/D converter, a simple switched-capacitor S/H circuit, shown in figure 1, is improved to realize an 8-bit resolution 40-MHz sampling rate of A/D converter. Based on the 0.8μm CMOS technology, this circuit can realize

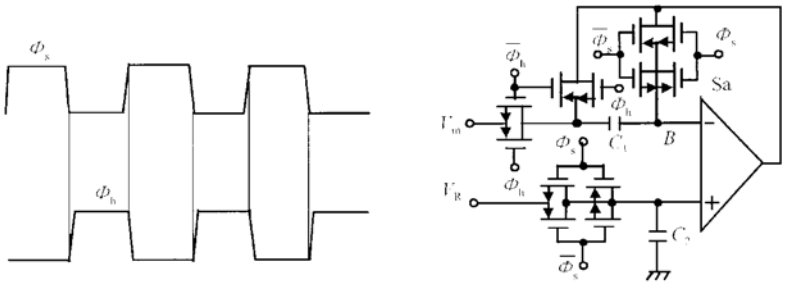

FIG. 1 Switched-Capacitor Sample-and-Hold Circuit

10-bit 50-MHz sampling rate. For this S/H circuit, following equations will be achieved:[4]

$$V_o = V_{in} + V_e \tag{1}$$

$$V_e = K_1 V_{in} + K_2 (V_R - V_{os}) \tag{2}$$

$$K_1 = -\frac{C_1 + C_p}{(1+A)C_1 + C_p} \tag{3}$$

$$K_2 = \frac{A(C_1 + C_p)}{(1+A)[(1+A)C_1 + C_p]} \tag{4}$$

Where V_e is the error voltage of the S/H output, V_{os} is the offset voltage of op-amp and C_p is the parasitic capacitance at node B. Generally, $C_p \ll C_L$ and the second form of V_e is approximately V_{os}/A. If A is 60dB and V_{os} is 30mV, the second term of V_e will be 30μV, which does not affect the signal accuracy, so that it can be neglected. But the error voltage due to the op-amp's finite gain is not cancelled but in inverse proportion to the gain of op-amp. The CMOS switches and dummy switches can eliminate the charge injection effect. Therefore, the gain of op-amp is the most important factor to determine the precision of sample-and-hold circuit.

From the analysis above, DC gain of the op-amp is the only factor determining the resolution of S/H circuit. In fact, parasitic capacitor of the switch is another factor, which decides the speed and accuracy of S/H circuit. If the S/H circuit based on 0.8μm CMOS technology is fabricated with 1.5μm CMOS technology, the parasitic capacitor of MOS

transistor will be largely enhanced, so the effect of signal couple from the input end of the switch to the output end is increased during the hold mode, and the sampling resolution of S/H decreased. In addition, the large capacitor increases the converter time of S/H circuit between sampling mode to hold mode and hold mode to sampling mode. That is to say even if the newly designed op-amp has the same performance with that based on 0.8μm CMOS technology, we could not realized the same performance of S/H circuit. Since the effect of the signal couple is determined by the technology, the only way to improve the resolution is to increase the performance of op-amp. According to the equation (1)—(4), DC gain of 62dB at least and the unity-gain frequency of 250MHz at least are required to be 8-b accuracy and 40-MHz operation. If the op-amp used in Ref. 4 is fabricated based on 1.5μm CMOS technology, the DC gain and unity-gain bandwidth will decrease largely and can not meet the need of 8-b 40-MHz sampling rate, so another op-amp based on 1.5μm CMOS technology must be designed.

3 Operator Amplifier Design

An op-amp with new structure based on 1.5μm CMOS technology is designed to realize the performance of DC gain of 62dB at least and unity-gain frequency of 250MHz at least, because the normal structure is difficult to meet the requirement. A novel regulated cascode op-amp based on the conventional one has been designed, as shown in Figure 2.

As we can see, this op-amp is of a two-stage structure. The first is a differential input stage, including M_1, M_2, M_3, M_4 and M_5. Output stage is the regulated cascode (RGLCDS) architecture (For positive signal path, it includes M_7, M_{c1} and M_{11}, while for negative one, it includes M_6, M_{10} and M_{c2}). Compared with the conventional cascode circuit, a feedback loop-gain stage is added. For positive signal path, in addition to the series feedback through M_{c1} in conventional cascode architecture, there is a second series negative feedback through the common-source amplifier transistor M_{11}. The transconductance of the output stage does not change, while the output impedance is increased by the two-gain product $(g_{mc1}r_{dsc1})(g_{m11}r_{ds11})$ over a single device, and the one-gain product $(g_{m11}r_{ds11})$ over the conventional cascode circuit, which is approximately equivalent to what is derived from a conventional triple-cascode amplifier[5]. But the op-amp has the same voltage range capability as conventional cascode circuits. The gain of this RGLCDS op-amp can be described as follows:

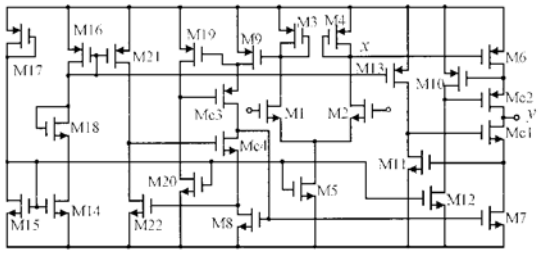

FIG. 2　Regulated Cascode Op-Amp

$$A_v = A_{v1}A_{v2} \tag{5}$$

Where:

$$A_{v1} = g_{m1}R_{I} \tag{6}$$

$$R_{I} = 1/g_{m3} \tag{7}$$

And:

$$A_{v2} = \left[\frac{g_{m6} + g_{m7}}{2}\right] R_{II} \tag{8}$$

$$R_{II} = (r_{ds7}g_{mcl}r_{dsc1}g_{m11}r_{ds11}) \parallel (r_{ds6}g_{mc2}r_{dsc2}g_{m10}r_{ds10}) \tag{9}$$

Where R_{I} and R_{II} are the output impedance of the differential input stage and the regulated cascode output stage, respectively. As it can be seen, since the active load M_3 and M_4 have been used in the differential input stage, R_{I} is very small. And R_{II} is very large because of the RGLCDS output stage, so the large DC gain of op-amp is mainly achieved by large output impedance R_{II}.

In this S/H circuit, sampling accuracy is increased by large DC gain of RGLCDS op-amp, but sampling rate which is another important parameter for S/H, is determined by the unity-gain frequency of op-amp. The larger the unity-gain bandwidth is, the higher of the sampling speed would be. To achieve a higher unity-gain frequency, it is important to move the pole-zero value to a higher frequency. In the RGLCDS amplifier, there exist several pole nodes, most of which have high frequency, do not effect the frequency performance of op-amp. Only those being of low frequency can effect the frequency performance. In this op-amp, there exist two high-impedance nodes, i.e. node x and node y. The pole frequency values at these two nodes are decided by the following equations:

$$f_{1} = -R_{II}^{-1}C_{l}^{-1} \tag{10}$$

$$f_{2} = -R_{I}^{-1}C_{p}^{-1} \tag{11}$$

$$C_{p} = C_{dbm4} + C_{gdm6} + C_{gbm6} + C_{gsm6} + C_{dgm2} + C_{dbm2} \tag{12}$$

where C_{l} is the load capacitor and C_{p} is the parasitic capacitance at node x. C_{l} is larger than C_{p} and R_{II} is larger than R_{I}. Compared with f_2, f_1, the dominant pole is lower, and f_2 is the complex pole. In order to increase the frequency of complex pole, active load M_3 and M_4 are used to reduce the first stage gains. Thus, the AC resistor of M_4 to ground is lowered, and f_2 is increased. In order to increase the frequency of the dominant node, output impedance of the regulated cascode output stage would have to be reduced, as would result in an undesirable lower gain. Because the main gain of the op-amp is generated at the regulated cascade output stage, a compromise between DC gain and the pole value should be considered. Due to the high output impedance of op-amp, large output-stage current is designed to accelerate the large signal slew rate. Moreover, large-sized input transistors are designed to realize the wider bandwidth. PSPICE and HSPICE simulations are used to verify the performance of the designed circuits.

4 Simulation Results and Layout

PSPICE simulation was applied to verify the circuit operation. Level 2 model in PSPICE was adopted, and the 1.5μm n-well CMOS process parameters were used in the

simulation with threshold voltage of 0.7V for all NMOS transistors and − 0.7V for all PMOS transistors. Capacitors in level 2 model are set by 2μm technology shown in Reference [6]. The frequency performance and the small-signal settling time of RGLCDS op-amp are shown in Figure 3 and Figure 4, respectively. A comparation in typical values is shown in Table 1 between the RGLCDS amplifier and the op-amp in the same S/H circuit listed in Reference [4]. Figure 5 shows the simulated results of the sample-and-hold circuit with RGLCDS amplifier, with the input signal frequency being 10-MHz and the sampling rate 40-MHz. Typical values of S/H circuit are shown in Table 2. Figure 6 shows the layout of the sample-and-hold circuit with 1.5μm N-well CMOS technology.

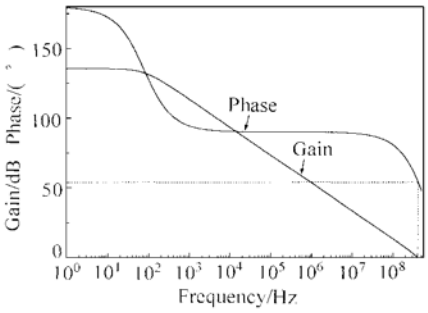

FIG. 3　DC Gain and Unity-Gain Frequency Performance of Regulated Cascode Op-Amp

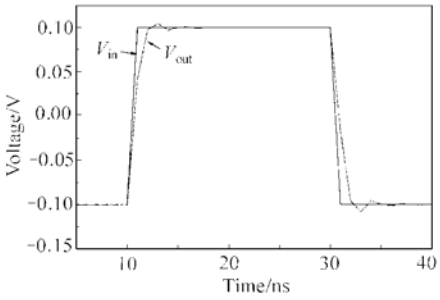

FIG. 4　Small Signal Settling Time of Regulate Cascode Op-Amp

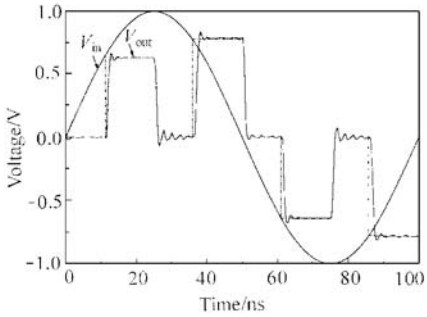

FIG. 5　S/H Output at 40-MHz Sampling Rate with Analog Input at 10-MHz

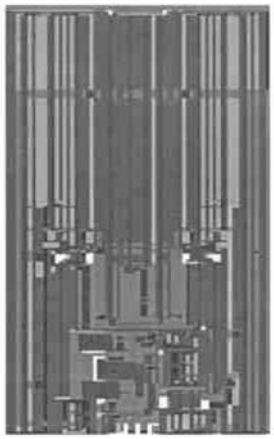

FIG. 6　Layout of Sample-and-Hold Circuit

Simulation results show that the op-amp designed has a DC gain of 140-dB and unity-gain frequency of 407-MHz, which has superiority over that of 60-dB, 107-MHz, 13 degree, and 33mW in Reference [4]. And the S/H circuit can realize an 8-b 40-MHz sampling rate and has been successfully used in an 8-b A/D converter.

Table 1 Comparation in Typical Values Between RGLCDS Amplifies and Op-Amp in Same S/H Circuit Listed in Ref. 4

	Regulated	Reference [4]
DC Gain/dB	140	80
Unity-Gain Frequency/MHz	407	300
Phase Margin/(°)	53	40
Settling Time/ns	8	8
Power Consumption/mW	97	130
Die Area/ mm^2	1.56×0.24	0.55×0.2
Technology	1.5μm n-Well CMOS	0.8μm CMOS
Output Swing/V	2	2

Table 2 Typical Values of S/H Circuit

Sampling Time/ns	Sampling Value/mV	Hold Value/mV	Error/mV
0—25	637.5	637.5	0
25—50	770.0	773.0	-3.0
50—75	-637.0	-637.0	0
75—100	-770.5	-771.5	1.0
100—125	637.5	635.2	2.3
125—150	770.5	773.0	-3
150—175	-637.5	-637.5	0
175—200	-770.5	-771.5	1

5 Conclusion

A switched-capacitor sample-and-hold circuit operating 8-b A/D converter is presented. Especially, a novel RGLCDS op-amp is designed that achieves a very high output impedance equivalent to the conventional triple-cascode circuit and the same output voltage range capability as the conventional double-cascode circuit. The superiority of this RGLCDS op-amp over the op-amp in Reference [4] has been demonstrated. The switched-capacitor S/H circuit using this RGLCDS op-amp can operate at a high frequency with high precision. The RGLCDS configuration may be acceptable for any circuit that needs large output impedance.

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