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VLSI Design Debug Using Focused Ion Beam Technology

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Abstract The use of focused ion beam (FIB) systems to edit prototype integrated circuits (ICs) has been increasingly relied upon by the semiconductor industry. This paper develops methods for very large scale integrated circuit (VLSI) design debug using FIB, including probing pad formation for deep node signal and device modification for prototype ICs. Different modification methods for different VLSI manufacturing processes are described. The electric properties of the deposited material and the reliability of the modification are discussed.

EEACC: 2570, 2560L, 7830

1 Introduction

Urged by the developments in the electronic industry towards miniaturization, the level of integration of integrated circuits (ICs) has steadily increased and the typical dimensions of the constituent devices have steadily decreased. The associated increase in the costs for the development of complex ICs and the demand for a short time-to-market for electronic products have resulted in the need for a submicron tool capable of testing and modifying malfunctioning circuits in very large scale integrated circuit (VLSI) design[1]. For this reason the focused ion beam (FIB) technology is getting increasingly important. During FIB process, a beam of Ga^+ ions is electrostatically focused into a 50nm spot and scanned over the surface of the sample. The interaction of the ion beam with the sample results in the ejection of atoms from sample surface and the production of secondary electrons and ions. The secondary charged particles can be collected, and their signals amplified and displayed to form an image of the surface. The production of ejected neutral atoms is generally referred to as sputtering. If the beam is rastered over a certain area for a length of time, material will be removed from that area. Deposition is possible in the presence of organometallic or TEOS gas. The scanning parameters can be adjusted to decompose the molecules which are introduced in the area of the ion beam and adsorbed onto the surface, forming a metal or insulator layer[2].

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This paper develops methods for mechanical probing pad formation and device modification by using FIB for different VLSI manufacturing processes. The electric properties of the deposited material and the reliability of the modification are discussed. Several points of concern are highlighted.

2 Experiment and Results

The FIB system used in this paper is a FEI model FIB200xP system, with a Ga^+ LMIS operating at a beam energy of 30keV. The system uses organometallic ($C_9H_{16}Pt$) and TEOS as the precursor gases for conductor and insulator deposition. They are delivered to the sample via a stainless steel tube of 0.4mm i.d. placed within 100μm from the surface, the tube making an angle of 45° with the sample normal. The background pressure in the chamber is typically 1.33×10^{-4}Pa. By collecting the ion-induced secondary electrons or the secondary ions generated by the beam, in-situ imaging is achieved. End-point detection is accomplished by monitoring the secondary ions to detect the change in emission at the semiconductor material interface.

VLSI design is a complex process requiring frequent revisions and multiple design iterations. The flow of a typical design debug is as follows: (1) Discover fault through system level test; (2) fault localization through electric test; (3) fault isolation and signal probing; (4) design fix by re-laying out circuit; (5) simulate fix through simulation engine; (6) verify fix by performing on-silicon device modification; (7) implement fix by generating a new mask set and manufacturing fix devices. For testing and modifying, FIB can be used to cut metal lines by sputtering through the metal lines, or to rearrange connections by locally cutting through the passivation on top of two lines and deposition of a Pt interconnect between these lines. Similarly, also probing pads for electric testing can be deposited on devices. With the aid of insulator deposition, the re-insulation of cut IC wiring and FIB deposited conductors is available.

2.1 Device Modification

For devices with design rules exceeding 1μm and two or three layers of interconnects, it is generally possible to find an access point for each track or signal which is not completely covered by other metal layers. Such devices can be repaired by directly FIB-sputtering to cut and uncover tracks in conjunction with FIB-induced conductor deposition for the interconnects. Figure 1(a) is a top view of such modification. The deposited interconnects have high concentrations of impurities. Auger analysis of the surface platinum film gives the composition ratios to be ~50% Pt, ~34% of C, ~15% Ga and ~1% O. The resistivity is determined to be about 300μΩ·cm using four-point probe test, which falls in the range 70~100μΩ·cm that one would expect for pure metals. Nevertheless, even at this resistivity, the modification has been tested as having good effectiveness. The Pt-Al via is then sectioned to give an illustration. Figure 1(b) shows that the aluminum line was cut off about 20 percent and the platinum made good contact with the aluminum track.

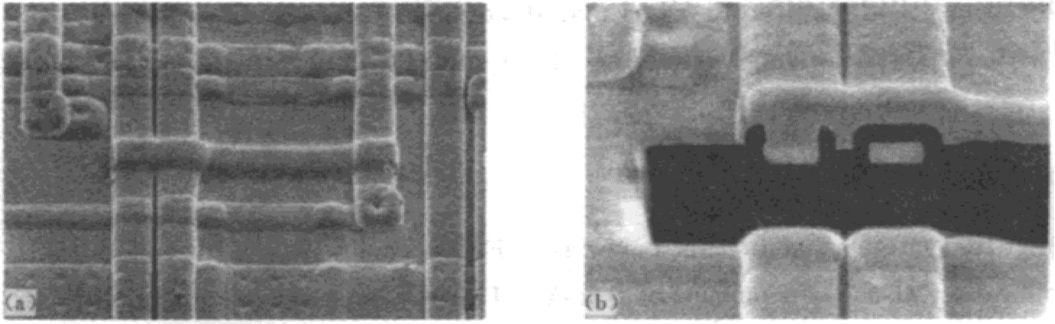

Fig. 1 Rewiring in two-level metal structure using FIB-induced Pt deposition.

The most complex devices have four or more layers of interconnects, with the upper layers often being in wide power or ground buses, or even bond pad covering much of the signal interconnects in the lower levels. The forward modification has much difficulty to route buried tracks without removing large areas of the covering metal plane. With the introduction of FIB-induced local insulator deposition, a new method shown schematically in Fig. 4 is developed to overcome this limitation. First, on each side a via with 3~3.5μm in width is drilled down through the top metal into the dielectric layer below (Fig. 2(a)). Enhanced etching is used for this process to avoid any re-deposition effects that would occur by sputtering alone and to make a higher-aspect-ratio via. This via is then back-filled with the insulator deposition material to a depth of 2~3μm (Fig. 2(b)). Once the insulator deposition is completed, enhanced etching is used to mill a smaller via through the center of the original hole to expose a contact with the metal track below (Fig. 2(c)). Finally, Pt material is deposited into the hole to bring the signal to the surface (Fig. 2(d)). Figure 3 shows a FIB cross-section through a completed via structure. The deposited insulator, which is analyzed by Auger electron spectroscopy (AES), consists of mainly silicon

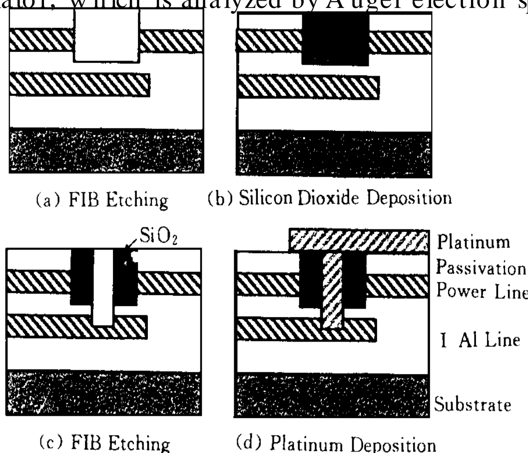

Fig. 2 Rewiring technique using silicon dioxide deposition by FIB.

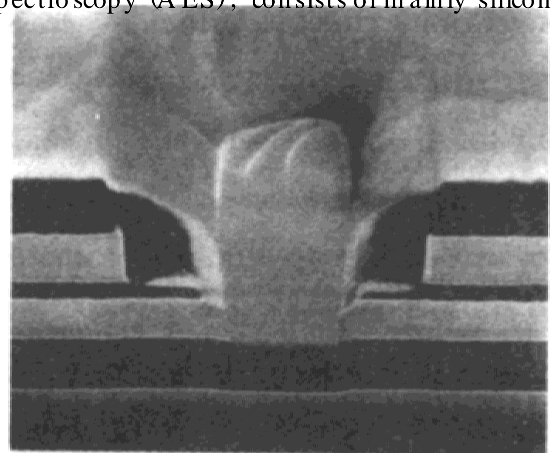

Fig. 3 FIB image of a completed via structure, shown schematically in Fig. 2

and oxygen and also ~ 5% Ga. The leakage between the deposited platinum and the power line is determined to be less than 2nA at 30V, corresponding to an isolation resistance of 15GΩ, more than enough for a successful FIB repair.

2.2 Probing Pad Formation

VLSI simulation modeling cannot always duplicate all of the independent variables found in a system level application. Sometimes monitoring the logic states at multiple internal nodes when operating in the native environment is the only way of debugging a subtle design error. In this situation, FIB technology is used to provide microprobe access points to deeply buried nets, which is achieved by drawing the electrode from the lower level metal layer. Typically, a hole of approximately 1.5×3μm is milled to contact accessible points on the net lines, and filled with platinum to create studs. A 15×15×2μm pad connected to the studs is deposited on the surface for mechanical tip touching. At the same time, the tested devices are electrically isolated using FIB cutting. Figure 4 shows a successful pad formation deposited on the surface of a E^2PROM array, in which the probing pad is just over the studs. The ground line of this array is cut as shown.

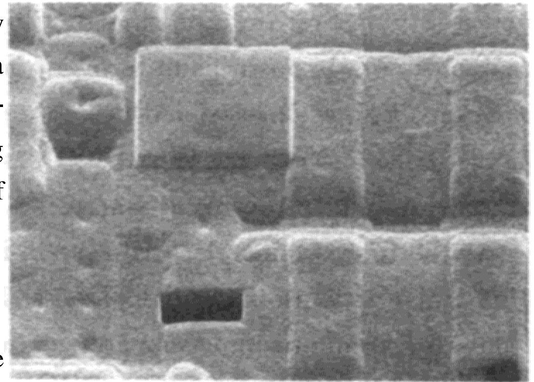

Fig. 4 Mechanical probing pad formation using FIB.

3 Discussion

FIB-induced vias and interconnects are not zero ohm connections and FIB cuts are not perfect open circuits. The resistivity of the FIB interconnects varies considerably depending on the deposition source material, the ion beam parameters used during the deposition, and the precursor gas flux (which, in turn, is dependent on the needle position relative to the sample, needle diameter, crucible temperature and chamber vacuum). If long wiring runs more than 200μm are required, lower resistivity interconnects can be achieved by combining FIB local connections with long laser CVD (LCVD) deposited gold conductors[3]. In this technique, a gold carrier gas is decomposed by a scanning laser beam, leaving a 5~10μm wide gold line on the work surface. The resulting sheet resistance of the LCVD gold lines is on the order of 0.1Ω/□. The capacitance of the interconnects is almost impossible to model, because it depends on a lot of parameters that cannot be controlled like substrate layout, dielectric thickness, dielectric constant, etc. But there definitely is capacitance and it will affect signals in the FIB deposited lines. If we know that a connection is particularly sensitive to resistance and capacitance we should take measures to minimize these effects. Likewise, these properties may be used to slow a signal or cure a race condition. FIB cuts are just trenches milled across a conductor, with gallium implanted into the bottom of the trench[4]. While this is an open circuit for most CMOS processes,

there is a small leakage across the trench that can be a trouble in certain high voltage or analog processes.

It has been traditionally believed that FIB irradiation contributes to the failure of a VLSI device[5]. FIB imaging and circuit modification processes can cause electrostatic discharge (ESD) damage in ICs. In general, the success rate of FIB modifications is increased by reducing the ion dose for imaging and navigation purposes to an absolute minimum. Extreme care must be exercised when performing circuit modifications on certain types of ICs, particularly when the modifications are in close proximity to the active (transistor) regions. Even with these precautions, post-modification electric testing may indicate that the ICs are altered to some extent by FIB exposure.

4 Conclusions

Even the most powerful circuit modeling systems cannot always generate 100% chip functionality on first revision silicon. Chip design layout and logic errors can be extremely damaging to one's business in terms of both increased development costs and delayed time to market. Using FIB-assisted design debug developed in this paper, designers can now minimize time and expense during the design cycle by modifying a prototype device rather than creating a new prototype wafer.

As the first commercial FIB system in China, we welcome customers to our center at Fudan University. Both individual die and packaged parts can be accommodated. The sample must be vacuum compatible and conductive samples are preferred.

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