Photonic AND Gate Based on Hybrid Integration of GaAs VCSEL and GaAs MISS*

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Abstract　The photonic AND gate based on the hybrid integration of GaAs Vertical Cavity Surface Emitting Laser (VCSEL) and Metal-Insulator-Semiconductor-Switch (MISS) is reported. The GaAs VCSEL is fabricated by selective etching and selective oxidation. The Ultra-Thin semi-Insulating layer (UTI) in the GaAs MISS is formed by using oxidation of AlAs, which is grown by Molecular Beam Epitaxy. The accurate control of UTI thickness and the processing compatibility between VCSEL and MISS are solved by this growth procedure. Using one VCSEL and two MISSs, we have fabricated a photonic AND gate. The experiment results are described. This device can be applied in free-space optical interconnection or optical calculation.

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1　Introduction

Vertical-cavity surface-emitting laser (VCSEL)-based photonic switches and photonic logic gates are well suited for applications in parallel optical processing and interconnections because of their compactness, surface-normal format, functional flexibility, low beam divergence, high optical gain and contrast. Recently, with the rapid progress of low threshold surface emitting lasers, several research groups have reported optical logic devices based on the integration of VCSELs and Heterojunction PhotoTransistors, or VCSELs and

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Heterojunction Bipolar Transistors[1,2].

In this letter, we proposed and demonstrated, for the first time, the Boolean logic AND using VCSEL and GaAs Metal-Insulator-Semiconductor-Switch (MISS). The Ultra-Thin semi-Insulating layer (UTI) in the GaAs MISS is formed by using oxidation of AlAs, which is grown by Molecular Beam Epitaxy (MBE). The accurate control of UTI layer and the processing compatibility between VCSEL and MISS are solved by this growth procedure. If a VCSEL is connected with two MISSs, the integrated device can be used as a photonic AND gate. A low optical switching power (10μW) for an AND gate has been achieved. We also can fabricate photonic switch or NOT logic gate by integrating VCSEL and MISS, more complex Boolean functions can be carried out by cascading sequential logic gate arrays. The hybrid integrated photonic AND gate can be applied in optical calculation or free space optical interconnection.

2 Device design and fabrication

2.1 Fabrication and characterizations of GaAs VCSEL

The GaAs/AlGaAs VCSEL structure was grown by MBE on an Si-doped ($3\times10^{18}cm^{-3}$) GaAs substrate. The top mirror consists of a 16 periods Be-doped ($3\times10^{18}cm^{-3}$) $AlAs/Al_{0.1}Ga_{0.9}As$ Distributed Bragg Reflector (DBR) containing $Al_{0.4}Ga_{0.6}As$ step-layers to reduce the series resistance associated with the heterobarrier offset, followed by Be-doped $1/2\lambda$-thick $Al_{0.25}Ga_{0.75}As$ ($3\times10^{18}cm^{-3}$) cladding layer, an undoped 2λ-thickness GaAs active layer and a Si-doped $1/2\lambda$-thick $Al_{0.25}Ga_{0.75}Ga_{0.75}As$ ($2\times10^{18}cm^{-3}$) cladding layer, and the bottom mirror is composed of a 30.5 periods Si-doped ($2\times10^{18}cm^{-3}$) quarter-wave $AlAs/Al_{0.1}Ga_{0.9}As$ DBR.

The processing steps of VCSEL structure were as follows: first, the wafer was nonselectively etched passing through p-DBR and active layer down to n-DBR, to from a $70\times70\mu m^2$ square measas. Then the active layer, which was transversely etched into $36\times36\mu m^2$ by using ($NH_4OH+H_2O_2$) selective solution. The ratio of selective etching rates K is 35 for $x\geq0.16$ (K = etching rate of GaAs/etching rate of $Al_xGa_{1-x}As$), when pH = 8.35 ± 0.05. Therefore, only active region was etched. Then the space layers of $Al_{0.25}Ga_{0.75}As$ and $Al_{0.4}Ga_{0.6}As$ were nonselectively etched by using $H_3PO_4+H_2O_2+H_2O$ solution. After that, the two AlAs layers adjacent to active layer were exposed. Then, at 420℃, the two exposed AlAs layers, including the AlAs layers in the p-DBR region, were laterally oxidized by the H_2O vapor carried by Nitrogen, leaving the GaAs in active region and $Al_xGa_{1-x}As$ in DBR region unoxidized. The oxidized regions in the two AlAs layers serve as current constriction layers. The oxidation rate was 1.0μm/min. Therefore, after 16min of oxidation, the current aperture of $4\times4\mu m^2$ was formed in the center of the active region and the un-oxidized region of p-DBR was $38\times38\mu m^2$, which formed the conducting path. It decreases the series resistance and optical leakage from the waveguide. The polyimide was glued to bind mesas to enhance the mechanical strength of the VCSEL structure, and a thick patterned

SiNO layer was deposited to isolate devices on the wafer. At last, the p contact was made with Cr/Au and the n contact with AuGeNi/Au, respectively.

The *I*-*V* characteristics of VCSEL are same as the *I*-*V* characteristics of the typical diode. Their forward voltages are about 1.2~1.4V, and the reverse breakdown voltages are larger than 6.0V, the series resistance are about 60~80Ω, the lasing wavelength is 860nm, the typical threshold current is 6mA. The minimum threshold current is 3.8mA, which is contributed to the small current aperture ($4\times4\mu m^2$) on both sides of AlAs layers adjacent to the active region and the index waveguide formed by the index step between un-oxidized region (2.96) and oxidized region (1.6) in the AlAs layers. The output optical powers are larger than 1mW, the angles of divergence are less than 7.8°. The rise times of output optical pulses is estimated to be less than 100ps.

2.2 Fabrication and characterizations of GaAs MISS

The structure of MISS is shown in Fig. 1. The attractive features of MISS device include suitable current, voltage and output power levels for OEIC (Opto-Electronic Integrated Circuit), high switch speed and high sensitivity to light or current injection. In general, on silicon substrate, dry oxidized SiO_2 was employed as the Ultra-Thin semi-Insulating layer (UTI) of MISS. The thickness of UTI is about 3~5nm. Obviously, it is very difficult to control the thickness and uniformity of UTI layer by this oxidation procedure. We implemented MISS directly on GaAs substrate, considering the compatibility of processing and light wavelength. The epi-structure of GaAs MISS was grown by MBE on a p-type GaAs substrate. It consists of a 0.5μm-thick Be-doped GaAs buffer layer (1×10^{19}cm), a 1.4μm-thick Si-doped (1×10^{16}cm) GaAs layer and 3nm-thick AlAs layer. The UTI of the GaAs MISS was formed by using wet oxidation of the AlAs layer, the oxidation process is same as that was used in fabricating VCSEL. The wafer planar process consists of four steps: 1) forming UTI Al_xO_y layer by wet oxidation, 2) etching V-groove for electrical insulation, 3) depositing patterned dielectric SiNO on Al_xO_y layer, 4) evaporating top and bottom electrodes.

The performance of the device is determined by the thickness of the structure layers and the doping concentration. The designed device works in the punchthrough mode, its leakage current at forward-biased high-impedance state is given by

$$I = \frac{nA}{\tau_g}\left(\frac{q\epsilon_s V}{2N_d}\right)^{1/2}, \tag{1}$$

where n_i is the intrinsic carrier concentration, A is the area of the upper electrode, τ_g is the life of minority in the surface depletion region, q is electron charge, V is the biased voltage, N_d is the dopant concentration in the n-type layer, ϵ_s is the dielectric constant of the semiconductor.

The switching voltage V_s of MISS (in dark) is given by

$$V_s = qN_d(W_n - W_j)^2/2\epsilon_s, \tag{2}$$

where W_n is the thickness of n-type epitaxial layer, W_j is the depletion layer width of the p-n junction.

The characteristics of devices depend on UTI layer thickness. Figure 1 shows the I-V characteristics of MISS. Two stable states, a high impedance "off" state and a low impedance "on" state, in a certain region are evident. At the switching point s, the switching voltage V_s is near 8.5V, and current I_s is 0.005mA, and at the lowest holding point h, the holding voltage V_h is 2.2V, and current I_h is 0.01mA, the switching time τ is less than 1ns.

Figure 2 shows the changing of V_s of MISS with incident optical power P_{in}. The experimental variation V_s with P_{in} was obtained by directing a GaAs semiconductor laser beam onto the light window of MISS. In Fig. 2, the threshold optical power required to reduce the switching voltage to 90% of its intrinsic value is 6μW.

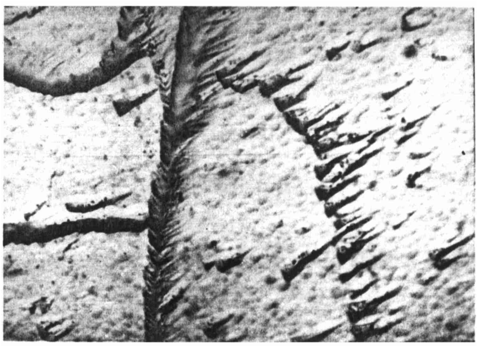

Figure 1 I-V characteristics of MISS
The insert is the schematic structure of MISS

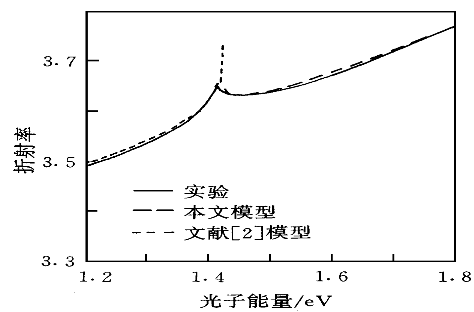

Figure 2 The change of switching voltage of MISS with the incident optical power
The wavelength of incident optical is 850nm

The optical control sensitivity of MISS is given by:

$$S_b = \frac{\partial V_s}{\partial P_{in}}. \tag{3}$$

From Fig. 2, in the linear region, we get: $S_b = 0.5V/\mu W$. But, if $V_s < 6.0V$, the sensitivity is reduced. The reason is that the incident optical power can not be absorbed effectively within the surface depletion region when V_s is less than 6.0V. Consequently, more optical power is required to switch the device. This emphasizes the importance of designing the MISS such that maximum absorption of the optical radiation occurs within the surface depletion region.

2.3 Fabrications and characterizations of the hybrid integrated photonic AND gate

Figure 3 shows the diagram of photonic AND gate based on the hybrid integration of VCSEL and MISSs and its equivalent circuit. Two GaAs MISS are connected with one GaAs VCSEL. The Integrated VCSEL/MISS (IVM) device is biased at a voltage below V_s ($V_s = 8.5V$, $V_{EC} = 7.0V$). In the dark, two MISSs are at "off" state. When the incident light ($\lambda = 850nm$) power is larger than 10μW, the two MISSs can be switched from high-impedance low-current "off" state to low-impedance high-current "on" state.

In Fig. 3, when the incident light power is larger than 10μW, A or B-MISS can be switched on, the current flows through the A or B-MISS and the VCSEL can be estimated as follows:

$$I_A = \frac{V_{EC} - V_j - V_h}{R_L + R_V + R_A + r_A}, \tag{4}$$

where $V_{EC} = 7.0V$, $V_j = 1.4V$, $V_h = 2.2V$, r_A is the "on" state resistance of MISS, $r_A \cong 1\Omega$, R_V is the differential resistance of VCSEL on its lasing mode, $R_V \cong 100\Omega$, $R_L = 200\Omega$.

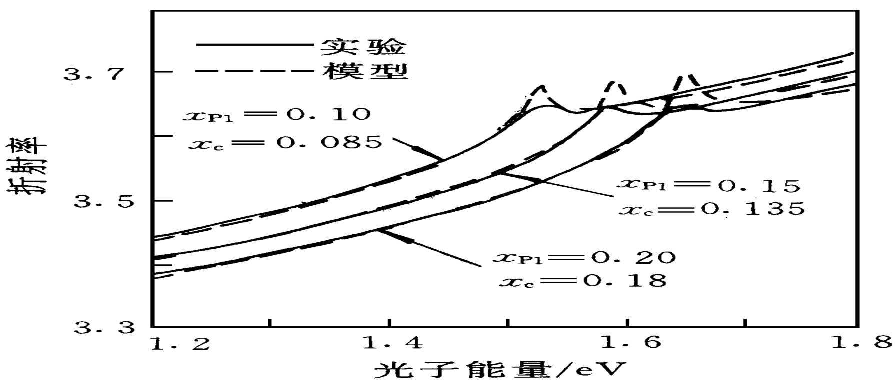

Figure 3　The schematic structure of the hybrid integrated device of a VCSEL and a GaAs MISS and its equivalent circuit

(a) the cross section of the hybrid integrated device of VCSEL/MISS,

(b) the equivalent circuit of "AND" gate.

For performing the AND logic, I_A and I_B should be given by:

$$\begin{cases} I_A = I_B < I_{th} \\ I_A + I_B > I_{th} \end{cases} \tag{5}$$

or:

$$1/2 I_{th} < I_A = I_B < I_{th}. \tag{6}$$

Using typical values given above, we get $265\Omega < R_A < 832\Omega$ and $3.0mA < I_A$ (or I_B) $< 6.0mA$. In this case, only one MISS (A or B-MISS) is switched on by the incident light ($P_{in} > 10\mu W$), the current through the VCSEL is less than its threshold current. Therefore, the VCSEL is in a light-emitting-diode mode with small optical output. When two MISSs are switched on by the incident light at the same time, the current flow through the VCSEL is $I_A + I_B$, which is larger than the threshold current. And the VCSEL is driven to lasing. This constitutes the photonic logic AND function. The truth table of the photonic logic AND is shown in Table 1.

Table 1　The truth table of the photonic logic AND

P_A (A-MISS)	P_B (B-MISS)	P_{out} (VCSEL)
0	0	0
0	1	0
1	0	0
1	1	1

A proposed monolithic version of devices is under studying. The IVM devices can be processed by standard IC processes and selective etching. The operation of a two-dimensional array of the monolithic IVM devices requires only two electrical wires for one common electrical bias. The third wire (input data from previous IVM devices) will be supplied in the form of a laser beam array. Therefore, the electrical system integration will be simple. And the optical system will also be simple and robust.

3 Conclusion

In summary, we have demonstrated a photonic AND gate based on the integration of GaAs VCSEL and MISS devices. The GaAs VCSEL is fabricated by selective etching and selective oxidation. The UTI of the GaAs MISS is formed by using oxidation of AlAs that is grown by MBE. The accurate control of UTI thickness and the processing compatibility between VCSEL and MISS are solved by this procedure. Using one VCSEL and two MISSs, we constructed a photonic AND gate. The experiment results are discribed. This device can be applied in optical calculation or free-space optical interconnection. A proposed monolithic version of IVM devices is under studying.

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