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Experimental Evidence of Interface-Trap-Related SILC in Ultrathin (4nm- and 2.5nm-Thick) n-MOSFET and p-MOSFET Under Hot-Carrier Stress*

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Abstract: Stress-induced leakage current (SILC) of ultrathin gate oxide is investigated by observing the generation of interface traps for n-MOSFET and p-MOSFET under hot-carrier stress. It is found experimentally that there is linear correlation between the generation of interface traps and SILC for both types of MOSFET with different channel lengths (including 1, 0.5, 0.275, and 0.135μm) and different gate oxide thickness (4nm and 2.5nm). These experimental evidences show that the SILC has a strong dependence on interface traps.

Key words: SILC; hot carrier stress; ultra-thin gate oxide; MOSFET

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1 Introduction

Stress-induced leakage current (SILC) in ultrathin gate oxides thinner than 5 nm has attracted a great attention because it is the critical issue affecting the reliability in modern nonvolatile memory technologies and standard CMOS applications[1~4]. In recent years, it has been reported that SILC after Fowler-Nordheim (F-N) stressing has a close relationship with hydrogen[5~8], because the SILC and the interface-state generation after F-N stressing are clearly suppressed by the deuterium incorporation[9,10].

However, SILC generally are widely investigated after uniform stresses in the F-N regime and substrate hot hole injection (SHH). But in the practical application, where hot carrier degradation is presented during the writing or erasing steps in electrically erasable programmable read only memory cells (EEPROM)[11], SILC is also observed and plays important role on reliability of device. However, few studies concentrated on SILC in MOSFET under hot-carrier stress[9,11~13]. It is reported that localized channel hot hole injections are able to induce a SILC comparable to the one obtained in the case of uniform injections in F-N stress[11]. And Esseni *et al.*[13,14] compared SILC during F-N stress and hot-carrier stress. Therefore, further study is necessary to investigate the relationship between SILC and the interface damages under hot-carrier stress.

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In this paper, SILC in ultrathin 4nm- and 2.5nm-thick oxides is studied on both n-MOSFET and p-MOSFET under non-uniformed hot-carrier stress. Using standard I-V characteristics, we investigate the degradation of the transistors by studying the relationship between SILC and the generation of interface traps, which are monitored by charge pumping (CP) technique and direct-current current-voltage (DCIV) measurements.

2 Experiment

MOSFETs used in this study were fabricated using standard CMOS technology. Hot carrier stress was applied on MOSFETs with 4nm and 2.5nm gate oxides and different channel lengths, then SILC and interface traps generation were measured by interrupting hot-carrier stress periodically. Interface traps were measured by using CP technique and DCIV method.

In CP measurements, the gate pulse frequency was fixed to be 500kHz, and both the rise and fall time were maintained at a constant value of 150ns. The varying base voltage of the pulse was applied to the MOSFET and the charge pumping current, I_{CP}, was measured during the CP measurement, while the top level of the pulse was kept constant. In DCIV measurements, the source was connected to a high-resistor; the substrate was grounded; and the junction between the substrate and the drain was forward-biased (0.3V), while surface potential was controlled by the gate voltage (V_g). At the same time, the damage near the source was monitored by exchanging the electrical configuration applied on source and drain terminals in DCIV measurement.

In this work, the hot-carrier stress experiments were performed under the stress condition of $V_g = V_d$ for both n- and p-MOSFET, which favors hot-electron injection and hot-hole injection, respectively. And hot-carrier stress was applied with a range of stress drain voltages V_d. All stressing and monitoring measurements were performed at room temperature.

3 Results and discussion

3.1 n-MOSFET

Firstly, we compare SILC between during hot-carrier stress and during F-N stress in n-MOSFET with gate oxide thickness of 4nm. The SILC result is shown in Fig. 1. It is clearly seen that SILC during hot-carrier stress ($V_g = V_d = 4.6$V) is more serious than that of during F-N stress ($V_g = 4.6$V, and $V_d = 0$V) with the channel length of 1μm. It is indicated that the study of SILC under hot-carrier stress is also important for reliability of ultrathin MOSFET.

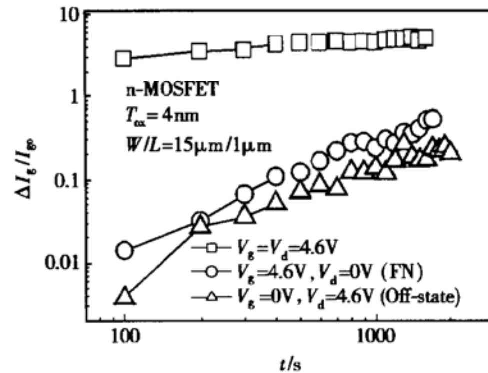

Fig. 1 Comparison of SILC (measured at V_g = 3.5V) between different stress conditions, including hot-carrier stress, F-N stress, and off-state stress for ultrathin gate oxide thickness

To confirm the question whether the degradation of SILC under hot-carrier stress is indeed induced by channel hot carriers, instead of F-N injection between the gate and the source, we monitor the interface trap densities with forward- and reverse-DCIV method. It is known that the base current (I_B) versus gate voltage (V_g) plot during the DCIV measurement in MOSFET consists of two peaks, one corresponding to the recombination current via interface traps in the channel region and the other to that in the drain (or source) space-charge region[15,16]. The results of DCIV measurements are shown in Fig. 2. From Fig. 2, it is observed that there is no change of the peak of I_B near

source terminal of device in reverse-DCIV measurement before and after hot-carrier stress, while the same increase of the peak of I_B in channel is observed for both forward- and reverse-DCIV method, and the increase of the peak of I_B near drain forward-DCIV measurement is most dominant. The result indicates that the most damage induced under hot-carrier is located near drain region, and the high stressing voltage between gate and source (like F-N stress) plays little roles on SILC under hot-carrier stress ($V_g = V_d$).

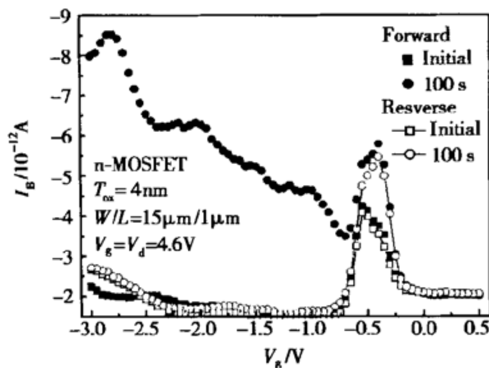

Fig. 2 Forward and reverse DCIV curves after hot-carrier stress

To further verify that SILC is induced indeed by channel hot carrier, instead of stressing voltage existed at overlap region between gate and drain, we performed off-state stress experiment ($V_g = 0$, and $V_d = 4.6$V) and the results are also shown in Fig. 1. The SILC induced by off-state stress is far smaller than that by $V_g = V_d$ stress. These results show the channel hot carrier, which is generated by the high electric field near drain junction, results in SILC under $V_g = V_d$ stress. Therefore, this effect of SILC under hot-carrier stress on reliability can not be neglected.

Figure 3 shows the gate current, (I_g) as a function of the gate voltage (V_g) before and after hot-carrier stress for 4nm-thick gate oxide. It is clearly found that the SILC increase with the stress time. It is also noted that the results were obtained by a direct measurement. The SILC measurements are performed carefully to obtain steady state SILC by a very slow V_g sweep rate. The reproducibility and the stability of SILC have been checked with I-V measurements performed several hours after the stress, which shows no variation compared to the one done just after stress.

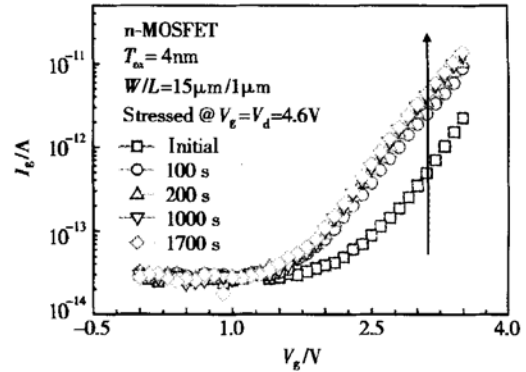

Fig. 3 Time evolution of SILC under hot-carrier stress on n-MOSFET

In order to investigate SILC more quantitatively, we performed experiments at high gate voltage stress conditions with varying the stress drain voltages. Figure 4 shows the generation of SILC for n-MOSFET under various stress drain voltages. The result shows that the SILC increase with stress drain voltage for identical stress time.

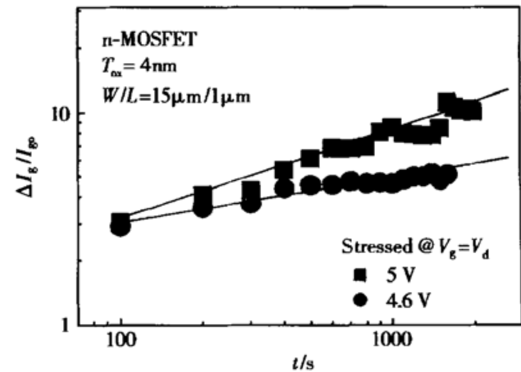

Fig. 4 SILC (measured at $V_g = 3.5$V) evolution for stress condition of $V_g = V_d$ with various V_d SILC is increased when V_d is increased.

The corresponding measurements of charge pumping current are shown in Fig. 5. The time indicated in the figure denotes the accumulated stress time. The maximum values of charge pumping current, I_{CP} in the CP spectra, which are proportional to the interface trap density, N_{it}, increase with the

stress time. It is also observed that the charge pumping current increase with higher stress drain voltage conditions for identical stress times.

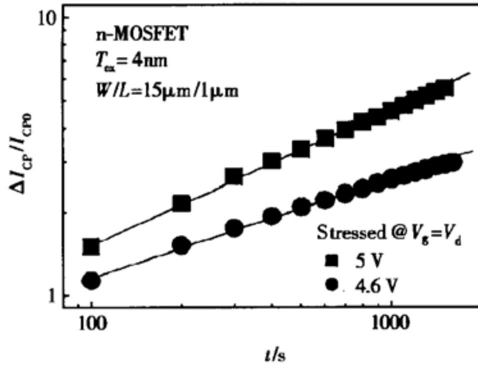

Fig. 5 Evolution of the maximum charge pumping current during hot-carrier stress under various stress drain voltages for a 4nm oxide in p-MOSFET

According to the fact that both SILC and interface trap density increase after hot-carrier stress and increase with stress drain voltage, some relationship between the two variables may exist. From experimental results, an interesting fact is observed that there is a unified linear correlation between the degradation of SILC and the generation of interface trap, as shown in Fig. 6, even though the stress drain voltage varies. The unified linear correlation suggests the mechanism of SILC is same for the stress mode at $V_g = V_d$.

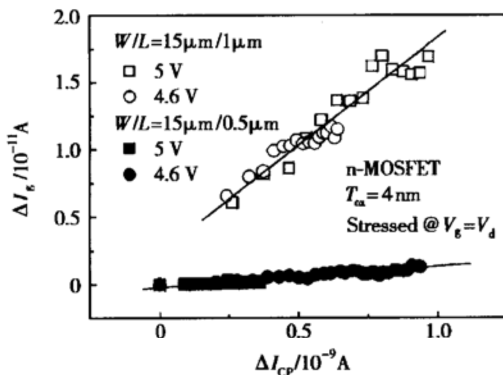

Fig. 6 SILC (measured at $V_g = 3.5$V) variations versus I_{CP} variations under hot-carrier stress for n-MOSFET with gate oxide thickness of 4nm and channel lengths of 1 and 0.5μm

Figure 6 also shows the generation of SILC as a function of interface traps density for n-MOSFET of channel length 0.5μm under hot-carrier stress. It is clearly seen that there is a unified linear relation between SILC and the generation of interface traps with varied stress drain voltages, even though the slope of the curves differs for different channel lengths.

3.2 p-MOSFET

In order to study the degradation mechanism of SILC, we also performed the same stress mode ($V_g = V_d$) on p-MOSFET with same gate oxide thickness. The result is shown in Fig. 7. It is clearly observed that there also is a unified linear correlation between SILC and the generation of interface traps for p-MOSFET, which is consistent with the previous results of n-MOSFET.

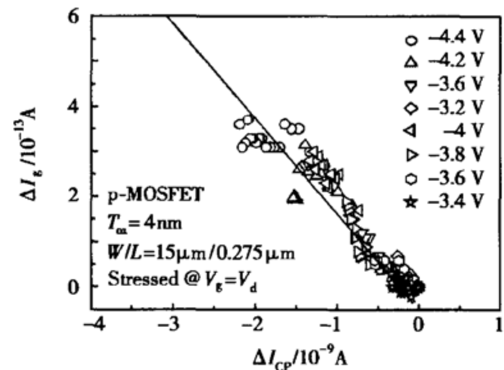

Fig. 7 SILC (measured at $V_g = 3.5$V) variations versus I_{CP} variations under hot-carrier stress for p-MOSFET with gate oxide thickness of 4nm and channel lengths of 0.275μm

To further investigate this linear relationship between SILC and the generation of interface traps, we also implemented the CP measurement with 2.5nm gate oxide on p-MOSFET, as shown in Fig. 8. The strong correlation of SILC with the generation of interface traps is confirmed again.

3.3 Discussion

In our experiments, it has been found that there is a linear correlation between SILC and generated interface traps for both of n-MOSFET and p-MOSFET under hot-carrier stress, with different

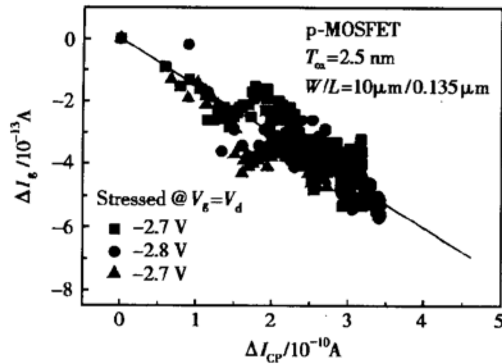

Fig. 8　SILC (measured at V_g = 3.5V) variations versus I_{CP} variations under hot-carrier stress for p-MOSFET with gate oxide thickness of 2.5nm and channel lengths of 0.135μm

channel lengths (including 1, 0.5, 0.275, and 0.135μm) and different gate oxide thickness (4nm and 2.5nm). And more, the linear dependence of SILC on the generation of interface traps keeps unchanged for the same channel length with varied stress drain voltages, and the slope of the curves is constant.

It is noted that, in our experiments, the SILC values were measured at the different gate voltages. The gate voltages were about 3.5V for 4nm n-MOSFET, 3V for 4nm p-MOSFET, and − 1.2V for 2.5nm p-MOSFET, respectively, and were constant during the stress time studied in this experiment. Therefore, the linear dependence of SILC on generation of interface traps was independent on measuring gate voltages of SILC.

In Ref. [13], the authors studied SILC under hot hole injection (HHI) stress condition for n-MOSFET, and they thought SILC has the same origin as the generation of interface traps and it is rate limited by hot hole injection, which agrees with the anode hole injection (AHI) model. It is known that for p-MOSFET, high stress V_g condition also favors hot-hole injection into the gate oxide. In our experiments, the result of p-MOSFET under the stress condition of V_g = V_d seems to agree with the conclusion by Esseni *et al*. However, at the same time, we observe the unified linear correlation for n-MOSFET under hot-carrier stress at V_g = V_d. And it is known that hot electron injection dominates the degradation for n-MOSFET under such high gate voltage stress, where the generation of interface traps is mainly attributed to hot electrons, instead of hot holes. The linear correlation between SILC and the generation of interface traps for n-MOSFET under hot-carrier stress can not be interpreted by hot hole injection model.

So we think that SILC is directly related to the generation of interface traps for both n- and p-MOSFET under hot-carrier stress. The generation of interface traps could be induced by either channel hot electron or channel hot hole, however, this does not change the linear relationship between SILC and the generation of interface traps.

With the reduction of gate oxide thickness, it is reported that near-interface-trap-assisted tunneling mechanism can be used to predict breakdown[17]. In our experiments, the linear dependence of SILC on the generation of interface traps could be also interpreted by such near-interface-trap-assisted tunneling mechanism. And further investigation on physical mechanism of interface-trap-related SILC under hot carrier stress will be performed in future study.

4 Conclusion

The SILC of ultrathin gate oxide was investigated by observing the generation of interface trap under hot-carrier stress. It has been found that there is a linear correlation between SILC and the generation of interface traps for n-MOSFET and p-MOSFET with different channel lengths (including 1, 0.5, 0.275, and 0.135μm) and different gate oxide thickness (4nm and 2.5nm). And the linear dependence of SILC on the generation of interface traps keeps unchanged for the same channel length with varying stress drain voltages, and the slope is constant.

These experimental evidences support that the mechanism of SILC under hot-carrier stress is directly due to the generation of interface traps by

channel hot electron or channel hot hole.

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超薄栅MOS器件热载流子应力下SILC的产生机制*

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摘要: 通过测量界面陷阱的产生, 研究了超薄栅nMOS和pMOS器件在热载流子应力下的应力感应漏电流(SILC). 在实验结果的基础上, 发现对于不同器件类型(n沟和p沟)、不同沟道长度(1、0.5、0.275和0.135μm)、不同栅氧化层厚度(4和2.5nm), 热载流子应力后的SILC产生和界面陷阱产生之间均存在线性关系. 这些实验证据表明MOS器件减薄后, SILC的产生与界面陷阱关系非常密切.

关键词: 应力感应漏电流; 热载流子应力; 超薄栅氧化层; MOS器件

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