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Drain and Source on Insulator MOSFETs Fabricated by Local SIMOX Technology*

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Abstract: To overcome the floating-body effect and self-heating effect of SOI devices, the drain and source on insulator (DSOI) structure is fabricated and tested. The low dose developed recently and low energy local SIMOX technology combined with the conventional CMOS technology is used to fabricate this kind of devices. Using this method, DSOI, SOI, and bulk MOSFETs are successfully integrated on a single chip. Test results show that the drain induced barrier lowering effect is suppressed. The breakdown voltage drain-to-source is greatly increased for DSOI devices due to the elimination of the floating-body effect. And the self-heating effect is also reduced and thus the reliability increased. At the same time, the advantage of SOI devices in speed is maintained. The technology makes it possible to integrate low voltage, low power, low speed SOI devices or high voltage, high power, high speed DSOI devices on one chip and it offers option for developing system-on-chip technology.

Key words: SIMOX; MOS devices; silicon on insulator technology; floating-body effect
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1 Introduction

The self-heating effect and floating-body effect are the most serious drawbacks of the SOI devices. As the dimensional length of the device shrinks, the power-density of the IC increases. However, the low thermal conductivity of the buried-oxide along with the Si/SiO_2 interface thermal resistance[1] obtracts the heat to transfer to the environment and thus the working temperature of SOI devices is greatly increased comparing to conventional bulk devices. This limits the performance and reliability of the SOI device too. The floating-body effect is another noticeable disadvantage, which results in severe DIBL effect and low BV_{DSS}. These drawbacks restrict the use of SOI device only to low supply voltage and low power applications. However, the need to integrate low voltage, low power or high voltage, high power devices onto a single chip is increasing[2], especially in the digital and RF mixed systems.

In order to overcome these drawbacks, the drain and source on insulator (DSOI) structure[3], only with buried-oxide under source and drain has been proposed as shown in Fig. 1.

Since there is no oxide layer under the channel, the floating-body effect and self-heating effect are overcome. As SIMOX (separation by implantation of oxygen) is being developed, low dose and low energy implantation has been widely used[4].

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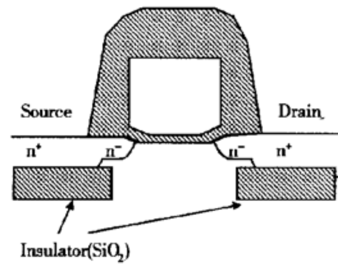

Fig. 1 Drain and source on insulator MOSFET

This makes it possible to realize DSOI structure by local SIMOX[5] technology. By this technology, experimental DSOI devices have firstly been successfully fabricated and SOI, bulk and DSOI devices are integrated on a single chip. We can test and compare the characteristics and the performance of three kinds of devices on a same chip. Only one additional mask is needed to form the local SIMOX, other fabrication processes are fully compatible with conventional CMOS technology. The DIBL (drain induced barrier lowing) effect, characteristics of output, BV_{DSS}(breakdown voltage of drain to source), working temperature in the device and gate delay of ring oscillator in three kinds of devices were compared. The results were analyzed.

2 Fabrication

Figures 2(a), (b), and (c) illustrate the procedure of fabrication. First, a thermal SiO_2 layer with the thickness of 500nm was grown on the wafer as a mask for selective implantation. Then the windows for implantation were formed. Oxygen was implanted with the energy for implantation ranging from 70keV to 140keV and the dose of oxygen from $2.5\times10^{17}cm^{-2}$ to $9.0\times10^{17}cm^{-2}$ for different wafers (100mm in diameter). The temperature of the substrate was set to 600℃ during the implantation. After the implantation, the wafers were annealed at 1300℃ for 6h in Ar/0.5% O_2 gas. The thin oxide was formed during this anneal removed. The routine inspections of the samples with microscope show that the product wafers are flat and crystal perfect. After that, a conventional 0.5μm-CMOS technology was used to manufacture the devices. A series of structures had been made out with different buried-oxide thickness and silicon thickness. The devices were nMOSFETs with a gate oxide thickness of 20nm, a junction depth about 300nm and W/L from 30/0.5 to 30/30. For comparison, bulk, conventional SOI and DSOI devices were made on a same chip.

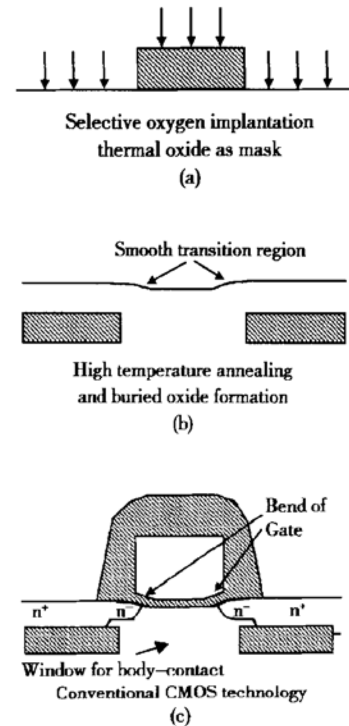

Fig. 2 DSOI device and its fabrication The floating-body effect is eliminated and the self-heating effect is greatly reduced

3 Test results

Figure 3 shows the SEM photograph of a DSOI device with Si film with the thickness of 120nm and buried-oxide thickness of 55nm. Good formation of buried-oxide under source and drain can be clearly seen. No lateral expansion of the buried-oxide can be seen. In fact, the end edge of the buried-oxide is a little apart from the gate edge. Since the concentration of implanted oxygen at the edge is less than that at the central part and during the oxide formation in annealing, the buried-oxide shrinks a bit at the edge. This indi-

cates that the technology can be used to fabricate DSOI CMOS devices with much shorter gate length. The source and drain regions with buried-oxide under what this stands for are slightly raised due to the volume expansion during the oxide formation, but the transition is smooth. The results of device simulation[6,7] show that the existence of the transition region will decrease the electrical field near the source and drain edges. The lowering field at the source region will decrease the current density against source gate voltages and will increase the parasitic resistance of the shallow junction. On the other hand, lowering field at the drain region is beneficial to the device reliability and increase the breakdown voltage. The latter is also beneficial to device for high speed and high power applications. The source and drain elevation shown in Figure 3 is not so serious as expected. In fact, during the oxygen implantation, some of the top silicon film is sacrificed due to sputter and oxidation. During the annealing, if the thermal oxide mask is not removed, some of the top silicon film on source and drain regions will be converted into oxide because

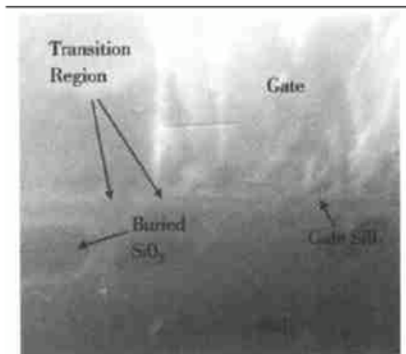

Fig. 3 SEM picture of the DSOI device Good formation of buried oxide and smooth transition region can be clearly seen.

of oxygen existence in the annealing gas. Therefore, the elevation of the implanted region can be accurately controlled, and eliminated by careful design of the technical process. Source/drain elevation is useful for very short channel devices to reduce the contact resistance, so the above phenomena have a practical application in some cases.

Figure 4 shows the characteristics of the electric current I_{ds} between drain and source against the voltage V_{gs} between the gate and source for the three kinds of devices with W/L of 30/0.6. The thickness for the silicon film and buried-oxide was 300nm and 90nm before the CMOS processes. Under these conditions, the SOI devices work in a partially depleted state. All of the test results are in following. From Fig. 4 we can see that the DIBL of DSOI is greatly suppressed compared to SOI device due to the elimination of the floating-body effect and is even better than the bulk device because of the elevated drain and source. To amplify the described effect, a large V_{ds} = 3V was used for ΔV_{th} measurement. Since the CMOS device technology is not optimized here, the DIBL effect is quite larger even for the bulk device, but the improvement of DSOI still confirms us its advantage over SOI. Figure 5 shows the measured ΔV_{th} versus gate length for the three different kinds of devices. Figure 6 demonstrates the comparison of the BV_{DSS} versus gate length for three kinds of devices in which significant improvement of BV_{DSS} in the DSOI from SOI can be seen. The fact that BV_{DSS} in the DSOI devices is even larger than the bulk devices can be considered as a result of the raised drain and source.

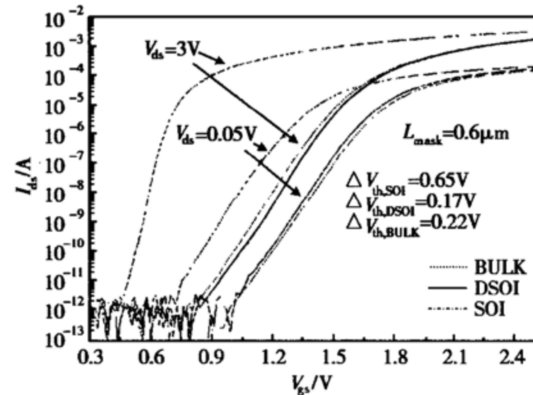

Fig. 4 Comparison of the DIBL effect of three kinds of devices The DIBL effect of the DSOI devices is greatly reduced.

The output characteristics of the DSOI and SOI devices are shown in Fig. 7. At low gate volt-

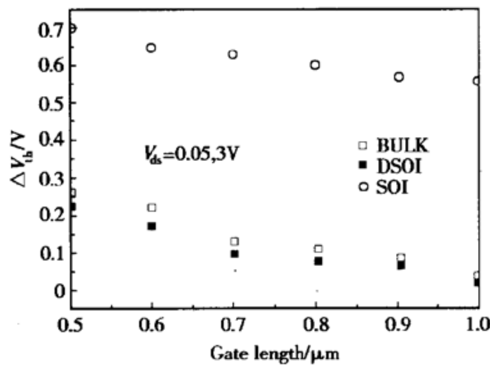

Fig. 5 DIBL effect versus gate length in three kinds of devices The DIBL effect of the DSOI devices is greatly reduced.

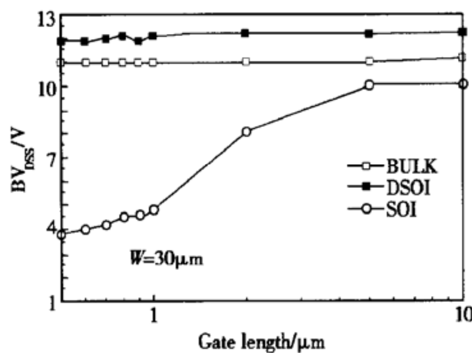

Fig. 6 BV_{DSS} in three kinds of devices The BV_{DSS} of the DSOI devices is obviously increased.

ages, the drive current I_{ds} of the DSOI is somewhat smaller than that of the SOI device because of the bending of the gate in the DSOI. At higher gate and drain voltages, the I_{ds} of the SOI device is reduced by the self-heating effect and is lower than that corresponding to DSOI device with less self-heating effect. In order to investigate the influence of the buried oxide to self-heating effect, the working temperature of three kinds of devices is measured using the method in Ref. [8], and the experimental results are shown in Fig. 8. From Fig. 8 we notice that, though the buried oxide layer is quite thin (90nm), temperature differences between devices are still quite significant. Because there is no buried oxide layer under the channel of DSOI, the working temperature of DSOI device is obviously lower than that of SOI device, and is close to that of the bulk device. The larger thermal resistance associated with relatively thin buried oxide film probably comes from the existence of the larger interface thermal resistance of Si and SiO_2 interface[1].

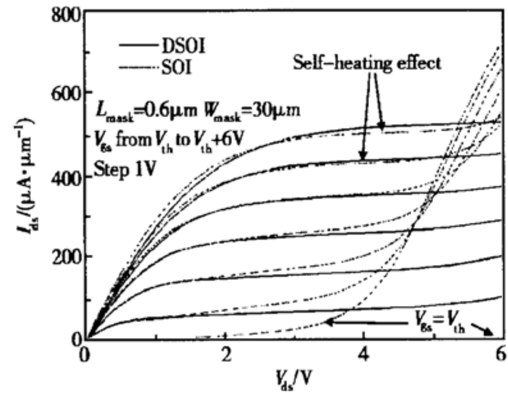

Fig. 7 Output characteristics of DSOI and SOI device At high gate and drain voltages, the drive currents I_{ds} of the SOI devices are greatly reduced due to the self-heating effects.

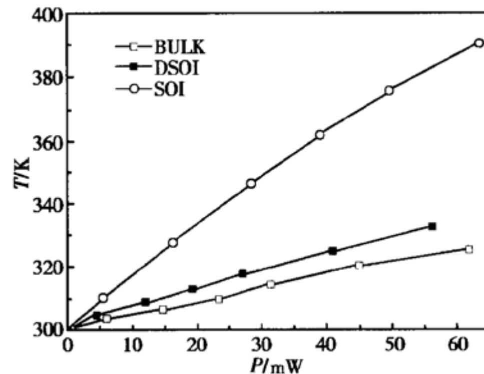

Fig. 8 Working temperature of three kinds of devices with $W/L=0.6$ The working temperature of DSOI device is obviously lower than that of SOI device, and close to that of bulk device.

The gate delays of the nMOS inverter were measured by use of 101-stage ring oscillators for different devices on the same chip. The results are shown in Fig. 9. Since the BV_{DSS} of SOI devices is low, the supply voltage to SOI devices is set below 4V. But the supply voltage for DSOI and bulk devices can reach quite a high level. It can be seen that the gate delay of DSOI device is much smaller than bulk devices and is only a little bit larger than that of SOI devices at the same supply voltage.

And when the supply voltage of DSOI devices increases, the gate delay can decrease steadily until the value as small as that of SOI devices. This implies that DSOI device could be used in high speed and high voltage applications. Figure 9 gives a information of the ultimate delay in DSOI much better than that in SOI. The reason is that the inverter is a saturation loaded n-type, which limits the real working gate voltage of the drive devices. In other words, the ultimate delay of DSOI in Fig. 9 corresponds much lower V_{DS} rather than possible higher values. Further, since the DSOI device is not optimized, the parasitic resistance of shallow junction may introduce much delay. We expect by use of CMOS inverter and a good optimized DSOI device structure, the performance of DSOI at high voltage can be made much higher than that SOI can achieve.

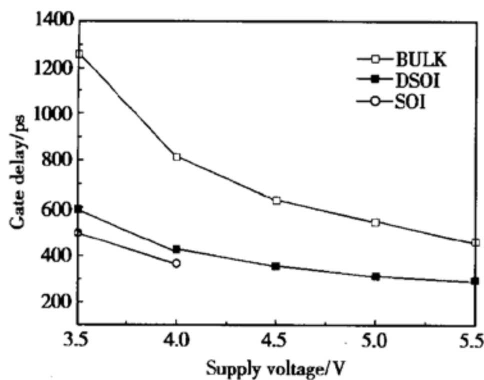

Fig. 9 Gate delay for nMOS inverter that builds up the 101-stage ring oscillator of three kinds of devices The gate delay of DSOI device is close to that of SOI device

4 Discussion and conclusion

Based on the local SIMOX technology, DSOI structure is realized and is successfully integrated with SOI and bulk devices on a single die. Their regular characteristics and performance of either devices obtained from experiments prove that the proposed process of the local SIMOX with a low dose, low energy implantation is a possible method for the MOS project. Although the technology is far away from really application, but test results clearly show that the floating-body effect and self-heating effect of DSOI are overcome in DSOI structure. Due to the expansion of the SiO_2, the source and drain region is slightly raised and a smooth transition regions is observed between the oxide and the bulk silicon. The performance of the device will deteriorate a bit by existence of this transition region, but the reliability is increased. It is possible to control and eliminate the elevation of the implanted oxide region by a proper process regulation. We can use this "self" source and drain elevation technique for the benefit of device characteristics and performance. The success of integrating DSOI, SOI and bulk devices on a single die makes possible to integrat low voltage and low power devices or high voltage high power devices of high speed on a single chip. The highest performance of the DSOI devices should be much higher than its bulk and SOI devices due to the reduced drain and source parasitic capacitance and use of possible higher supply voltage. This work only shows the possible advantage of the proposed technology. For pushing forward this technology to practical application, a series of careful studies is needed and room for both technical and structural optimization exist. First, a self-aligned technology for CMOS should be used for deeper submicron devices. Then, the optimization of the source/drain elevation, the length of the transition region should be made. These are what we focus in further investigation.

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一种采用局域注氧技术制备的新型DSOI器件*

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摘要: 为了克服传统SOI器件的浮体效应和自热效应, 采用创新的工艺方法将低剂量局域SIMOX工艺及传统的CMOS工艺结合, 实现了DSOI结构的器件. 测试结果表明, 该器件消除了传统SOI器件的浮体效应, 同时自热效应得到很大的改善, 提高了可靠性和稳定性. 而原先SOI器件具备的优点得到了保留.

关键词: DSOI; SOI; 局域注氧技术; 自热效应; 热阻

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