第 24 卷第 7 期 半 导 体 学 报 Vol. 24, No. 7
2003 年 7 月 CHINESE JOURNAL OF SEMICONDUCTORS July, 2003

A Method to Separate Effects of Oxide-Trapped Charge and Interface-Trapped Charge on Threshold Voltage in pMOSFETs Under Hot-Carrier Stress*

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Abstract: A simple new method based on the measurement of charge pumping technique is proposed to separate and quantify experimentally the effects of oxide-trapped charges and interface-trapped charges on threshold voltage degradation in p-channel metal-oxide-semiconductor field-effect transistors (pMOSFETs) under hot-carrier stress. Further, the experimental results verify the validness of this method. It is shown that, all three mechanisms of electron trapping effect, hole trapping effect and interface trap generation play important roles in p-channel MOSFETs degradation. It is noted that interface-trapped charge is still the dominant mechanism for hot-carrier-induced degradation in p-channel MOSFETs, while a significant contribution of oxide-trapped charge to threshold voltage is demonstrated and quantified.

Key words: MOS device; oxide trap; interface trap; hot-carrier degradation; threshold voltage
PACC: 7220J; 7340Q
CLC number: TN43 **Document code**: A **Article ID**: 0253-4177(2003)07-0673-07

1 Introduction

It is well known that the hot-carrier effect becomes an important reliability issue with the dimensions of the MOSFET devices scaling down to submicrometer level[1~3]. Due to the hot-carrier effect, threshold voltage (V_{th}) of the device can be shifted, which will degrade the speed and current drive of device.

Under hot-carrier stress, threshold voltage degradation is caused by hot-carrier-induced Coulomb scattering centers[4,5]: interface-trapped charge and oxide-trapped charge. Understanding the roles these charges play in threshold voltage degradation is essential for prediction of threshold voltage behavior under hot-carrier stress. It is well known that interface-trapped charge and oxide-trapped charge have different time dependencies of buildup and different annealing properties[6]. As a result, different hot-carrier stress modes give rise to different relative amounts of interface-trapped charge and oxide-trapped charge. Therefore, it is necessary to quantify the effects of both trapped charge components separately. However, it is difficult due to the fact that the effect of oxide charge

* Project supported by State Key Development Program for Basic Research of China (No. G2000-036503)

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Received 26 November 2002, revised manuscript received 28 February 2003

trapping on device degradation is normally combined with, and masked by, the effect of interface traps. Moreover, it has been proposed that electrons generated by impact ionization can be injected into the oxide along with the injection of channel holes. Oxide charge is created when electrons and holes are trapped in the oxide. For a better understanding of degradation mechanisms and modeling of hot-carrier-induced damage, it is desirable to develop a technique to quantitatively determine the effects of interface trap generation and oxide charge trapping on device degradation.

In recent studies[7,8], Cheng *et al*. proposed a new technique to separate and quantify the effects of hot-carrier-induced interface trap creation and oxide charge trapping on the degradation in pMOSFETs by using the hydrogen/deuterium isotope effect. However, no clear relation between threshold voltage shift (ΔV_{th}) and oxide trapped charges (ΔN_{ot}) was obtained by this method. And their method is complex in nature due to additional annealing process in H_2 and D_2. In addition, other studies[9] show that electron injection exists under all of hot-carrier stress conditions in pMOSFETs, which was also observed in our experiments. It indicts that it is difficult to find a stress condition, where the generation of interface trap is the only degradation mechanism, as a criterion in Cheng's method.

In this paper, a simple and effective method to separate the effects of oxide-trapped charge and interface-trapped charge on threshold voltage in pMOSFETs under hot-carrier stress is demonstrated. The validness of this method is demonstrated by applying it to quantify the effects of interface trap generation and oxide charge trapping on the threshold voltage shift in deep submicron pMOSFETs.

2 Method description

It is well known that the total threshold voltage shift, $\Delta V_{th}(t)$, is due to two factors: (1) the evolution of the net gate oxide trapped charge, ΔN_{ot}, (located at a distance x_d from the Si/SiO_2 interface) and (2) the generation of the Si/SiO_2 interface trap charge, ΔN_{it}[10]. Assuming that x_d is close to the Si/SiO_2 interface[11], the threshold voltage degradation can be expressed as a function of two variables, ΔN_{ot} and ΔN_{it}. The corresponding total threshold voltage shift, $\Delta V_{th}(t)$ due to hot-carrier stress can be expressed as the sum of two components: the effect of oxide-trapped charge, $\Delta V_{th,Not}(t)$, and the effect of interface-trapped charge, $\Delta V_{th,Nit}(t)$. Then, for different devices under different stress conditions, we have:

$$\Delta V_{th}^{1}(t) = \Delta V_{th,Not}^{1}(t) + \Delta V_{th,Nit}^{1}(t) \quad (1)$$

$$\Delta V_{th}^{2}(t) = \Delta V_{th,Not}^{2}(t) + \Delta V_{th,Nit}^{2}(t) \quad (2)$$

where the superscript 1 and 2 represent different devices under different stress conditions, respectively. Further, according to above equations, the difference of threshold voltage shift between these two transistors is expressed as

$$\Delta V_{th}^{1}(t_1) - \Delta V_{th}^{2}(t_2) = (\Delta V_{th,Not}^{1}(t_1) - \Delta V_{th,Not}^{2}(t_2)) + (\Delta V_{th,Nit}^{1}(t_1) - \Delta V_{th,Nit}^{2}(t_2)) \quad (3)$$

To simplify this equation, a condition is added to our analysis. It is known that when equal numbers of interface traps are created in these two transistors,

$$\Delta N_{it}^{1}(t_1) = \Delta N_{it}^{2}(t_2) \quad (4)$$

where t_1 and t_2 represent the stress time required to generate a given number of interface traps under different stress conditions, respectively. The threshold voltage shifts due to interface trap creation are the same in both devices,

$$\Delta V_{th,Nit}^{1}(t_1) = \Delta V_{th,Nit}^{2}(t_2) \quad (5)$$

Combining Eqs. (3) and (5), one can obtain

$$\Delta V_{th}^{1}(t_1) - \Delta V_{th}^{2}(t_2) = (\Delta V_{th,Not}^{1}(t_1) - \Delta V_{th,Not}^{2}(t_2)) \quad (6)$$

It is noted that the result obtained from Eq. (6) is the difference of ΔV_{th} between two modes, not the contribution of all oxide-trapped charge under hot-carrier stress to the degradation of V_{th}.

Equation (6) indicates that if the same number of created interface traps is given, the differ-

ence of $\Delta V_{th,Not}$ between the two stress conditions is uniquely due to oxide charge trapping, while the difference of corresponding oxide-trapped charge, ΔN_{ot}, can be experimentally obtained by CP technique. Hence, the relation between the difference of $\Delta V_{th,Not}$ and difference of ΔN_{ot} can be obtained. Then, $\Delta V_{th,Not}(t)$ can be calculated from the time dependence of ΔN_{ot} obtained by CP method, while $\Delta V_{th,Nit}(t)$ can be given by Eq. (1).

3 Experiment

The devices used in our experiments are surface-channel p^+-poly gated pMOSFETs with the gate length of 0.275μm and the gate oxide thickness of 4nm. The transistors were then subjected to channel-hot-hole stress with a fixed drain stress voltage $V_d = -4.6$V and various gate stress voltage V_g from $V_d/2$ to V_d. The source and the substrate were grounded at all stress conditions. Interface trap density and oxide trapped charge density were periodically measured during stress by the charge pumping technique[12~14], and the threshold voltage V_{th} was determined by the conventional I_d-V_g characteristics with $V_d = -50$mV. All of our experiments are performed in the dark at room temperature.

4 Results and discussion

Figures 1(a), (b), and (c) show the interface trap creation, $\Delta N_{it} = N_{it} - N_{it0}$, the evolution of the number of oxide-trapped charge, $\Delta N_{ot} = N_{ot} - N_{ot0}$, and the threshold voltage shift, $\Delta V_{th} = V_{th} - V_{th0}$, vary with stress time, respectively.

It is clear that, ΔN_{it} and ΔV_{th} are always larger for stress condition at $V_g = V_d$ than at $V_g = V_d/2$. It is interesting in Fig. 1 (b) that, for stress condition at $V_g = V_d$, the oxide trapped charge is few negative, and becomes positive after long stress time. In pMOSFETs, the electron trapping leads to positive V_{th} shift, while hole trapping results in negative V_{th} shift. The phenomenon could be attributed to the combination of electron trapping effects and hole trapping effects, interpreted in our previous study (unpublished). The existence of negative oxide charge in initial stress period has also been reported in other work[9].

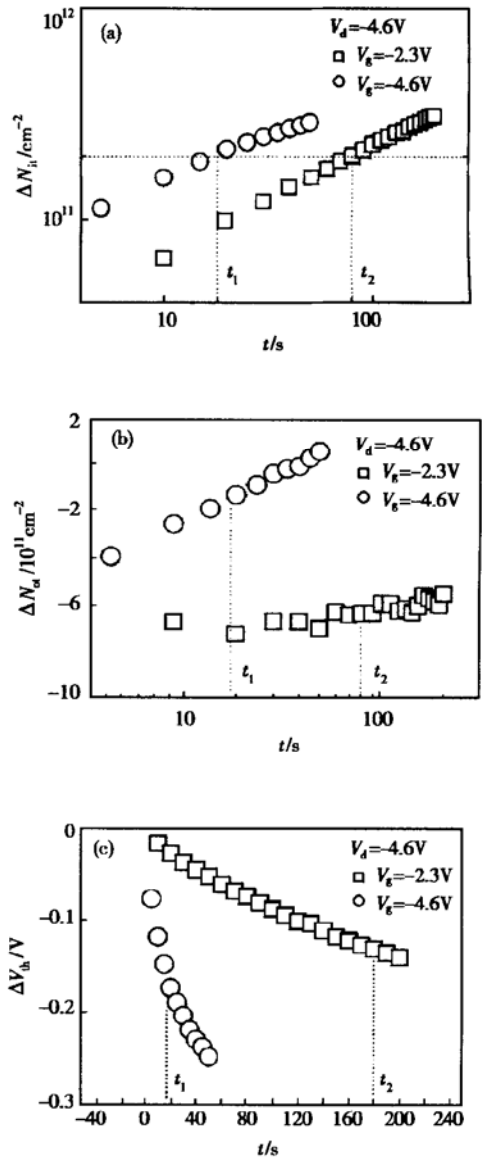

Fig. 1 Hot-carrier-induced interface trap creation (a), hot-carrier-induced oxide trapped charges (b), and threshold voltage shift (c) in pMOSFETs under two hot-carrier stress conditions

From Fig. 1 (b), electron trapping is dominant in oxide charging under both stress conditions, so one would expect an increase of V_{th} (positive ΔV_{th}).

However, in Fig. 1 (c) a negative ΔV_{th} is observed after stress. This is due to the fact that as a significant number of interface traps are generated, they cause negative V_{th} shift and overshadow the effect of electron trapping. And more, when the gate stress voltage V_g is increased to $V_g = V_d$, hole trapping also plays an important role resulting in more negative V_{th} shift during the device degradation.

According to our method, ΔV_{th} and ΔN_{ot} are plotted as function of ΔN_{it} and shown in Fig. 2(a) and (b), respectively.

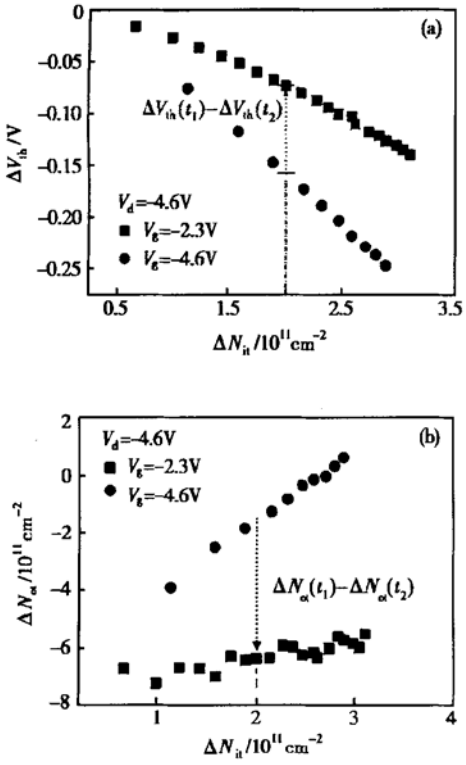

Fig. 2 Correlation of threshold voltage shift and interface trap creation (a) and correlation of oxide trapped charges and interface trap creation (b) under various gate voltage stress conditions

4.1 Effect of N_{ot} on V_{th}

By using our method to calculate the contribution of oxide trapped charges, ΔN_{ot}, to threshold voltage shift, $\Delta V_{th,Not}$, for different stress conditions in Fig. 2, one can readily obtain the relation between threshold voltage shift $\Delta V_{th,Not}$ and oxide trapped charges ΔN_{ot}. And typical result is shown in Fig. 3. A good linear relation between $\Delta V_{th,Not}$ and ΔN_{ot} can be clearly seen

$$\Delta V_{th,Not} = -\alpha \Delta N_{ot}$$

While, according to Possion's equation, $\Delta V_{th,Not}$ can be expressed as

$$\Delta V_{th,Not} = -\frac{q}{C_{ox}} \overline{\Delta N_{ot}}$$

where q is unit electron charge, $C_{ox} = \epsilon_0 \epsilon_{SiO_2}/t_{ox}$ is the oxide capacitance, t_{ox} is the oxide thickness, ϵ_0 is the permittivity of vacuum, and ϵ_{SiO_2} is the SiO_2 relative dielectric constant.

From Fig. 3, the coefficient α, which is the slope of $\Delta V_{th,Not}$ versus ΔN_{ot}, is 1.81×10^{-13} and is very close to the theory value of q/C_{ox}, 1.85×10^{-13}, which in turn verify the validation of our method.

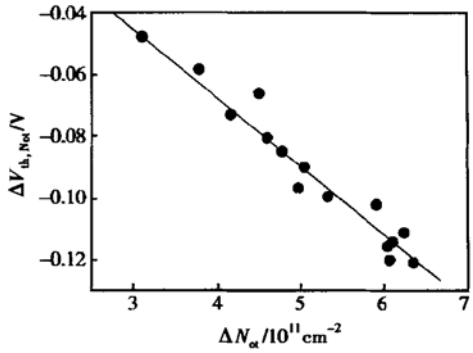

Fig. 3 Extracted relation of threshold voltage shift $\Delta V_{th,Not}$ and oxide trapped charges ΔN_{ot} in pMOSFETs under hot-carrier stress

4.2 Effect of N_{it} on V_{th}

Once the contribution of oxide charge trapping, $\Delta V_{th,Not}$, is known, one can simply extract the contribution of interface trap creation, $\Delta V_{th,Nit}$, by subtracting $\Delta V_{th,Not}$ from the total V_{th} shift. The result is shown in Fig. 4. Similarly with the result in Fig. 3, the linear relation of $\Delta V_{th,Nit}$ and ΔN_{it} is observed as well. It is worth noting that in Fig. 4, the V_{th} shift due to interface trap generation in device stressed at $V_g = V_d/2$ are very close to the result in device stressed at $V_g = V_d$, which further verify the validation of the proposed method.

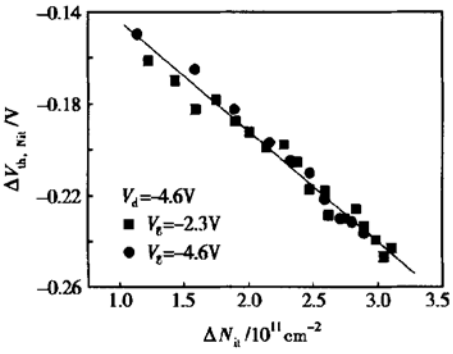

Fig. 4 Extracted relation of threshold voltage shift $\Delta V_{th,Nit}$ and interface trap generation ΔN_{it} in pMOSFETs under hot-carrier stress

4.3 Applications

The time dependence of both ΔN_{ot} and ΔN_{it} can be extracted by charge pumping technique simultaneously, then, $\Delta V_{th,Not}$ and $\Delta V_{th,Nit}$ as a function of stress time, can be obtained as well. The results are shown in Figs. 5 (a) and (b).

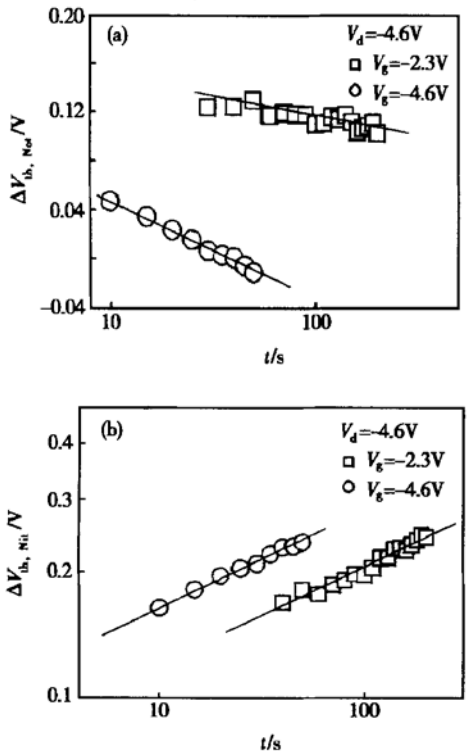

Fig. 5 (a) Extracted time dependence of the threshold voltage shift $\Delta V_{th,Not}$ due to oxide-trapped charges ΔN_{ot}; (b) Extracted time dependence of the threshold voltage shift $\Delta V_{th,Nit}$ due to interface-trapped charges ΔN_{it} in pMOSFETs under hot-carrier stress

In Figs. 5 (a) and (b), the threshold voltage shift due to oxide-trapped charge, $\Delta V_{th,Not}$, agrees to the logarithmic time dependence, while the threshold voltage shift, $\Delta V_{th,Nit}$, due to interface trap generation, increases with stress time by power-law. Because the experimental results show that the total threshold voltage shift can not be interpreted by the unique effect of either interface trap generation or oxide-trapped charge, both of interface states or oxide-traps affect the total threshold voltage shift.

It is seen in Figs. 5 (a) and (b) that at stress of $V_g = V_d/2$, more sever electron trapping occurs while few interface trap are generated than at stress of $V_g = V_d$. And it is also observed that at both stress conditions, the effect of generated interface trap on threshold voltage degradation is greater than the effect of oxide-trapped charges. Since in pMOSFETs, the electron-trapped charge leads to positive V_{th} shift, while interface-trapped charge results in negative V_{th} shift, the stress condition of $V_g = V_d/2$ shows few negative threshold voltage shift. This can interpret why the stress condition of $V_g = V_d$ degrades worse than that of $V_g = V_d/2$.

Although interface-trapped charge is the dominant mechanism for hot-carrier-induced degradation in p-channel MOSFETs, a significant contribution of oxide-trapped charge to threshold voltage is demonstrated in Fig. 5, especially for the stress of $V_g = V_d/2$.

It is worth noting that in our method, there is not a limit on the hot-carrier stress conditions, and the only thing is that at least two transistors are stressed at different stress conditions. It indicts that our method is more convenient and its application range is wide.

5 Conclusion

In summary, by using the charge pumping technique, we have investigated the degradation mechanisms in pMOSFETs. We present a new approach to distinguish and quantify the effects of

generated interface trap and oxide trapped charge on hot-carrier-induced degradation in pMOSFETs. It is found that neither interface-trapped charge alone nor oxide-trapped charge alone could properly account for hot-carrier-induced threshold voltage instability. Based on the method we developed, the sum of interface-trapped charge and oxide-trapped charge should be used in threshold voltage modeling. The significant contribution of oxide-trapped charge to threshold voltage is demonstrated, while the interface-trapped charges are the dominant mechanism for hot-carrier-induced degradation in p-channel MOSFETs.

Acknowledgement Thanks to Motorola Company for providing experiment samples and measurement equipments.

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一种用于分离 pMOS 器件热载流子应力下氧化层陷阱电荷和界面陷阱电荷对阈值电压退化作用的方法*

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摘要: 在电荷泵技术的基础上, 提出了一种新的方法用于分离和确定氧化层陷阱电荷和界面陷阱电荷对 pMOS 器件热载流子应力下的阈值电压退化的作用, 并且这种方法得到了实验的验证. 结果表明对于 pMOS 器件退化存在三种机制: 电子陷阱俘获、空穴陷阱俘获和界面陷阱产生. 需要注意的是界面陷阱产生仍然是 pMOS 器件热载流子退化的主要机制, 不过氧化层陷阱电荷的作用也不可忽视.

关键词: MOS 器件; 氧化层陷阱; 界面陷阱; 热载流子退化; 阈值电压

PACC: 7220J; 7340Q

中图分类号: TN43　　**文献标识码**: A　　**文章编号**: 0253-4177(2003)07-0673-07

* 国家重点基础研究发展规划资助项目(No. 2000-036503)

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2002-11-26 收到, 2003-02-28 定稿