Polysilicon Emitter Double Mesa Microwave Power SiGe HBT

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Abstract: A new 125nm UHV/CVD SiGe/Si epitaxy equipment SGE500 capable of commercialization is constructed and device-level SiGe HBT material is grown. A polysilicon emitter (PolyE) double mesa microwave power SiGe HBT showing excellent low current DC characteristics with $\beta = 60\times V_{CE}/I_{C} = 9, 0.0V/300\mu A$, $\beta = 100\times V_{CE}/50mA$, $BV_{CEO} = 22V, f_{t} = 5.4GHz, 7GHz@ 3V/10mA$ is demonstrated. The PolyE SiGe HBT needs only 6 lithographical steps and cancels the growth of the thick emitter epitaxy layer, both of which show great potential for volume production. A 60-finger class A SiGe linear power amplifier (PA) with 22dBm of 1dB compress point output power ($P_{out}$) 11dB of power gain ($G_{p}$) and 26.1% of power added efficiency (PAE) @ 900MHz, 3.5V/0.2A is demonstrated. Another 120-finger class A SiGe PA with 33.5dBm (2.1W) of $P_{out}$, 10 dB of $G_{p}$ and 33.9% of PAE @ 900MHz, 11V/0.5A is also demonstrated.

Key words: SiGe; HBT; microwave power amplifier

EEACC: 2520M; 2560L; 1350F


1 Introduction

The high-performance, high-integration, high-volume, and high-efficient SiGe IC could produce small factor form, long battery life, fast information and data transmission rate and high communication quality of service. Since SiGe was introduced into the industry in 1998, it has firmly involved into mainstream and created one of the most successful semiconductor miracles in such a short period of less than five years. SiGe explosively increased its market share in almost all the RF communication fields like 2G/3G mobile communication, 2.4GHz Bluetooth, 2.4 ~ 5.0GHz IEEE802.11a/b/g, up to 40Gbps optical communication, GPS, TV tuners, high-speed ADC and even ultrafast 5GHz FPGA.\(^{1}\)

The revised Johnson limitation says $BV_{CEO} \times f_{t}$ approximately equals $300GHz \cdot V$, which is a basic obstacle for RF power amplifier (PA), especially for high-breakdown case. SiGe technology now begins to challenge the role of GaAs and LDMOS in mobile communication base station PA. Recently Johansson et al.,\(^{2}\) reported a 25V/20W SiGe power transistor under 2GHz AB class CW condition for Cellular base station.

2 SGE500 and device structure

The soul of SiGe HBT is the strained Si/ SiGe/Si multilayer structure, the crystal quality, and material parameters of which are directly determined by the
epitaxy equipment. A new 125mm single-wafer UHV/CVD SiGe epitaxy equipment SGE500 capable of commercialization is constructed. Compare to its predecessor SGE400\(^3\), SGE500 obtains a considerable improvement. It adds a pre-loaded chamber to further isolate the reactive chamber from the atmosphere environment, and the base vacuum of the reactive room could reach beyond \(5 \times 10^{-7}\) Pa. SGE500 could raise the temperature at a rapid speed of up to 150\(^\circ\)C/min and the precisely controllable temperature range is broadened to 500 ~ 900\(^\circ\)C. The SiGe layer growth rate is typically 3~8nm/min.

The vertical structure of the PolyE SiGe HBT is shown in Fig. 1. The n\(^+\) (100) silicon substrate is chosen to reduce the bottom collector series resistance. The thickness \((W_c)\) and doping concentration \((N_c)\) of the n\(^-\) collector are chosen to satisfy the application specific demands of BV\(_{CEO}\) and maximum collector current density \((J_c)\). Key parameters of the base are germanium content \(x\) (at present, we just chose the constant \(x\) across base zone to simplify the material growth process), base thickness \(W_b\), and base doping concentration \(N_b\). The main design factors are DC current gain \((\beta)\), base intrinsic sheet resistance \((R_b)\) and \(f_t\). When \(W_b\) dropped, \(\beta\) and \(f_t\) would rise while \(R_b\) increased, then we could raise \(N_b\) to maintain rational \(R_b\). Unlike Si BJT, SiGe HBT could provide additional \(x\) to increase \(\beta\) exponentially, and therefore permit thinner \(W_b\) and heavier \(N_b\) (two orders higher than that of Si BJT) to ensure proper \(\beta\), optimized \(f_t\) and pretty lower \(R_b\), and thus optimized maximum oscillation frequency \((f_{max})\). The thin i-SiGe layers across both BE and BC junction are carefully designed to prohibit out-diffuse of boron from base to undoped emitter layer (I.E) and light-doped collector. The I.E layer would form true light-doped emitter layer after total post anneal steps, which could greatly reduce the BE junction capacitance as to improve \(f_t\). On the other hand, it must be thin enough for the poly impurity to diffuse into it and to ensure low emitter resistance. Present design selects a thickness of about 20 ~ 30nm. The top 200nm thick polysilicon layer is deposited using LPCVD, which will be discussed in the next section. Please Refer to Refs. [3, 4] for the detailed SiGe HBT material growth process.

The lateral structure is a little different from the one discussed in Ref. [5]. The emitter mesa is 1.6\(\mu\)m wide, the distance between the emitter mesa and B-hole is 1.2\(\mu\)m, and the B-hole and E-hole are both 0.8\(\mu\)m wide. The emitter stripe is 40\(\mu\)m long which is chosen to provide higher current and power output capabilities.

![Fig. 1  Vertical structure of PolyE SiGe HBT](image1)

![Fig. 2  Lateral structure of PolyE SiGe HBT](image2)

3 PolyE double mesa SiGe HBT process

The process is somewhat like the one reported in Ref. [5], the main improvement would be:

1. PolyE process. 200nm thick polysilicon (poly) is carefully deposited using LPCVD at 625\(^\circ\)C, which is then implanted with phosphorus at a dose of \(5 \times 10^{15}\) cm\(^{-2}\) and energy of 70keV. The clean step before poly deposition, the ion implantation and post anneal thermal budget have to be carefully designed to
satisfy the multiple demands of the transistor, which would be further reviewed in list (4).

(2) Sidewall process. Lateral size of the sidewall is a key step to the trade-off between $R_b$ and BE junction leakage current. A 300nm LPCVD SiO$_2$ is deposited and then anisotropical RIE is used to maintain a lateral size of about 150–200nm.

(3) Hole dielectric and hole-drilling process. 150nm LPCVD SiO$_2$ and 200nm PECVD Si$_3$N$_4$ are deposited as the hole dielectric. When the hole dielectrics is RIE etched to about 10–20nm, 1:100 buffered HF solution is used to wet-etch the remain thin layer to acquire clean and damage-free hole. The compound hole dielectric and the two-step hole-drilling process greatly improve the low current performance and cut down the collector leakage current.

(4) Total thermal budget. The total low thermal budget required by SiGe material puts a stringent demand on the post annealing condition. The doping impurity in the poly has to be activated effectively and some part of it ought to diffuse into the E layer to form a light-doped emitter. Extrinsic base and emitter contact resistance need to be lowered rationally. Out-diffuse of boron in the base to the collector and E layer and relief of the strained SiGe base zone under somewhat high temperature have to be simultaneously considered carefully. A twostep solution is adopted to tackle all of the upper aspects. Low temperature furnace annealing is first made to activate the doping, reduce possible crystal defect, diffuse the doping impurity from poly to the E layer, then RTA further reduce the contact resistance and activate the doping.

(5) Metal process. 1μm thick Al is sputtered at a substrate temperature of about 250°C to permit the stable and good contact formation. The alloy condition is 430°C/30min, which is chosen according to the trade-off between contact resistance and collector current leakage based on a great deal of temperature change experiments.

(6) Compatible with the standard Si CMOS technology. It is meaningful to note that the whole PolyE SiGe HBT process is super simple with only 6 lithographical steps and compatible with the current CMOS process and now under the small volume production development. Figure 3 gives the final device structure.

![Fig. 3 Final HBT device structure](image)

### 4 DC characteristics

The transistor’s DC characteristic is measured using Keithley 4200. Figure 4 shows the reverse breakdown characteristic of E and C junctions. The BC junction breakdown voltage is about 22V, which is very hard and the leakage is pretty low (91nA@20V, 10-finger transistor). The BE junction breakdown voltage is about 3V and somewhat soft (3μA@–2V), which may be caused by the poly BE junction (E layer is very thin for the space-charge zone to easily extend across the poly layer).

Figure 5 shows the excellent low current DC characteristic $\beta = 60@V_{CE}/I_C = 5V/300μA$. When collector current increased, $\beta$ increased also, to about $\beta = 100@5V/50mA$.

Besides exponentially increased with $x$ in the SiGe base, the introduction of the wider-bandgap PolyE could also further increase $\beta$, e.g., a PolyE SiGe HBT with current gain beyond 800@5V/50mA is fabricated. The using of PolyE permits a smaller $x$ to provide higher thermal budget or heavier boron concentration to produce lower base resistance, which provides additional flexibility to trade between DC and RF performance.
After being packaged in a metal ceramic form, the scattering parameter of a 10-finger transistor (emitter area $10 \times (1.6\mu m \times 40\mu m)$) is measured using HP8510A, from which $f_t$ and $f_{\text{max}}$ is deduced (see Fig. 6). The initial result is somewhat lower than expected: $f_t/f_{\text{max}} = 5.5\text{GHz}/7.7\text{GHz} \@ 3V/10mA$, the detailed reason is under investigation.

Class-A linear PAs using 60-finger and 120-finger PolyE SiGe HBT are made. Figure 7 shows $P_{\text{out}}$, $G_{\text{m}}$, and PAE curves of the 60-finger PA at a pretty low DC bias ($900\text{MHz}$, $V_{CE}/I_C = 3.5V/0.2A$). At $1\text{dB}$ compression point, $P_{\text{out}}/G_{\text{m}}/\text{PAE} = 22\text{dBm}/11\text{dB}/26.1\%$, as bias increases, the 60-finger SiGe PA gives that of $29.3\text{dBm} (0.85\text{W})/9.3\text{dB}/22.6\% @ 9V/0.37A$, while the 120-finger SiGe PA gives that of $33.3\text{dBm} (2.1\text{W})/10.3\text{dB}/33.9\% @ 11V/0.52A$. 

Fig. 6  RF curves of 10-finger PolyE SiGe HBT
5 Conclusion

A new 125mm UHV/CVD SiGe/Si epitaxy equipment SGE500 capable of commercialization is constructed and device-level SiGe HBT material is grown. A PolyE double mesa microwave power SiGe HBT process showing excellent low current DC characteristics with $\beta = 60 @ 9V / 300\mu A$, $\beta = 100 @ 5V / 50mA$, $BV_{CEO} = 22V$, $f_l / f_{max} = 5.4GHz / 7.7GHz$ at 10-finger, 3V/10mA is first demonstrated. The poly emitter provides additional flexibility to trade-off between DC and RF performance. The whole process needs only 6 lithographical steps, and is compatible with current CMOS process, and cancels the growth of the thick emitter epitaxy layer, which shows great potential for volume production. A 60-finger class A SiGe linear PA with 22dBm of $P_{1dB}$, 11dB of $G_p$ and 26.1% of PAE @ 900MHz, 3.5V/0.2A is demonstrated. Another 120-finger class A SiGe PA with 33.5dBm (2.1W) of $P_{out}$, 10.3dB of $G_p$ and 33.9% of PAE @ 900MHz, 11V/0.52A is also demonstrated.

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References


多晶发射极双台面微波功率 SiGe HBT

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摘要：研制成功了可商业化的75mm单片超低空白酸气相淀积硅外延设备 SiGe500，并生长了器件级 SiGe HBT 材料。研制了具有优良小电流特性的多晶发射极双台面微波功率 SiGe HBT 器件，其性能为：$f_c / f_{m} = 9V \times 300\text{mA}$, $p_{d} = 100\text{V/V}$, $50\text{mA}$, $B_{v3d}= 22V$, $f_{m} = 5.4\text{GHz} / 7.7\text{GHz} @ 10$ 拆, 3V/10mA。多晶发射极可进一步提供直流和射频性能的叠加，该工艺总共只有 6 步光刻，与 CMOS 工艺兼容且(因多晶发射极无需发射极外延层)的生长，这些优点使其适合于商业化生产。利用 60 指和 120 指的 SiGe HBT 制作了微波功率放大器，60 指功放在 900MHz 和 3.5V/0.2A 时的在 1dB 压缩点时给出 $P_{m} / G_{y}$ 和 PAE = 22dBm/11dB/26.1%。120 指功率发 900MHz 工作时给出了 $P_{m} / G_{y}$ 和 PAE = 33.3dBm (2.1W) / 11.3dB/33.9% @ 11V/0.52A。

关键词：硅基；异质结双极晶体管；微波功率放大器

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