Low-Microwave Loss Coplanar Waveguides Fabricated on High-Resistivity Silicon Substrate *

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Abstract: Three kinds of coplanar waveguides (CPWs) are designed and fabricated on different silicon substrates ——common low-resistivity silicon substrate (LRS), LRS with a 3μm-thick silicon oxide interlayer, and high-resistivity silicon (HRS) substrate. The results show that the microwave loss of a CPW on LRS is too high to be used, but it can be greatly reduced by adding a thick interlayer of silicon oxide between the CPW transmission lines and the LRS. A CPW directly on HRS shows a loss lower than 2dB/cm in the range of 0～26GHz and the process is simple, so HRS is a more suitable CPW substrate.

Key words: coplanar waveguides; high-resistivity silicon; microwave loss; high frequency; optoelectronic packaging

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1 Introduction

With the rapid development of the internet and wireless communication, there has been a great demand for low-loss, low-cost, and small-size radio frequency (RF) and microwave circuits, which are necessary for supplying the devices and modules with high speed drive during the course of optoelectronic and microelectronic packaging. In microwave circuits, the coplanar waveguide (CPW) is one of the most popular microwave components. A qualified CPW should have low loss, high transmission power, wide working bandwidth, and low cost.

Silicon has been the preferred substrate material for CPWs because of its many advantages, such as mature technology, good thermal conductivity, easy integration with the microelectronic devices, and low cost[1～4]. However, transmission lines and passive components on standard low-resistivity silicon substrate have high loss because of its semiconductor characteristics. To overcome this problem, many approaches have been used. One is to use a material with a low dielectric constant, such as silicon oxide or polyimide, as the interlayer between the transmission lines and silicon substrate to reduce the attenuation[5,6]. Though it has been approved as an effective way, it makes the process more complicated and is incompatible with other processes. The other straightforward approach that directly fabricates microwave transmission lines on the high-resistivity silicon (HRS) substrate is preferable because the process is simple, and the price of HRS is comparable with standard low-resistivity silicon now, which is around $15 for a 100mm wafer with a resistivity of around 4000Ω·cm. According to Refs. [7,8], a resistivity of over 2500Ω·cm is enough for the demand of low loss at high frequencies for transmission line.

In this paper, three kinds of CPWs were made on high-resistivity silicon substrate, standard low-resistivity silicon (LRS) substrate, and LRS substrate with a silicon oxide interlayer. The design and fabrication of CPWs are introduced.

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2 Design

In the packaging of optoelectronic devices, CPWs with an impedance of 50Ω are very popular for meeting the impedance match. The common CPW structure is shown in Fig. 1(a), in which the impedance of the CPW is related to the parameters W, G, T, and H. In this paper, microwave office software was used to determine these parameters with the existing CPW model to make sure the impedance of the CPW is 50Ω. Also taking the convenience of measurements into consideration, the parameters were determined to be $W = 120\mu m$, $G = 75\mu m$, $H = 500\mu m$, and $T = 2\mu m$. The structure of the CPW on the substrate with the interlayer is shown in Fig. 1(b).

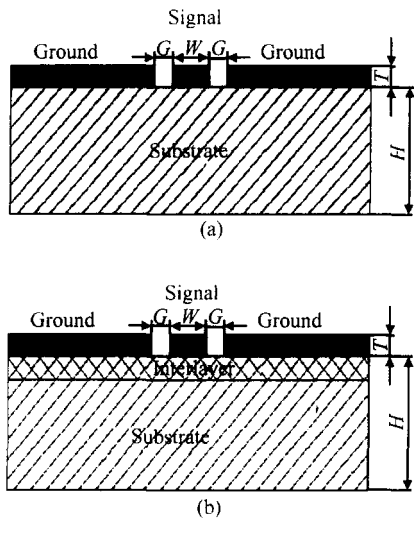

Fig. 1 (a) Cross section geometries of the standard CPW; (b) Cross section geometries of the CPW with an interlayer

3 Fabrication

In the experiment, we fabricated the CPW transmission lines on LRS, LRS with a silicon oxide interlayer, and HRS. The three kinds of sample substrates used in the experiments were all 500μm thick, the resistivity of the HRS used was around 4000Ω·cm, the LRS was 3～5Ω·cm, and the silicon oxide interlayer between the transmission lines and the LRS substrate was 3μm thick, which was obtained through thermal oxidation in the LRS wafer. The same fabrication process was used for all samples. First, a 300nm thick CrAu was deposited on the wafers through evaporation. Then the resist was coated. After exposure and wet etching, the CPW pattern was formed. Finally, a 2μm of Au was electroplated onto the CPW transmission lines.

4 Results and discussion

The measurements were taken on wafers using an HP 8510C network analyzer and high frequency coplanar probes. The S parameters S_{21} and S_{11} of three kinds of CPWs were obtained and are shown in Figs. 2 and 3. The attenuation was calculated and is plotted, see Fig. 4.

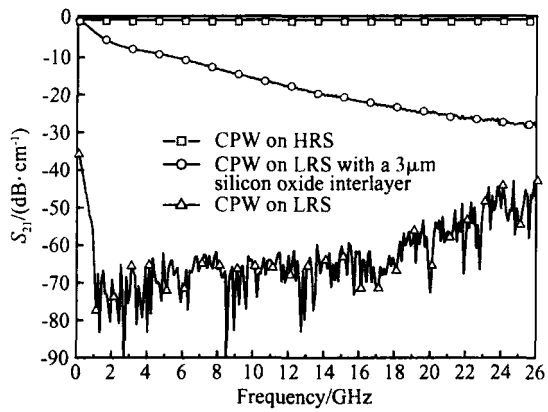

Fig. 2 S_{21} of the CPWs on HRS, LRS, and LRS with a 3μm interlayer

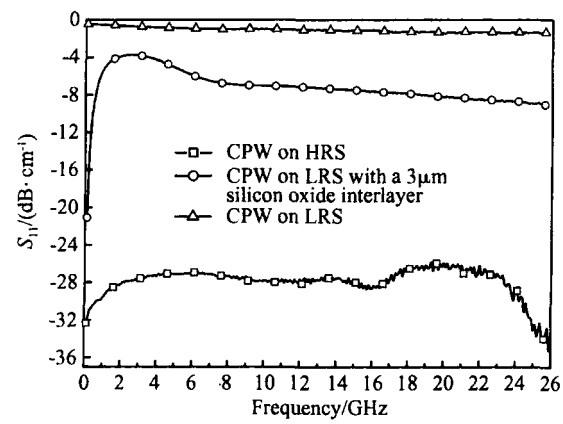

Fig. 3 S_{11} of the CPWs on HRS, LRS, and LRS with a 3μm interlayer

From the figures, we can see that the performance of the CPW on the LRS substrate is very poor because of the low resistivity, which leads to "through state" between the signal and ground lines at high frequencies. The loss is more than 200dB/cm, which is too high for use as a CPW substrate. When a 3 μm silicon oxide interlayer is add-

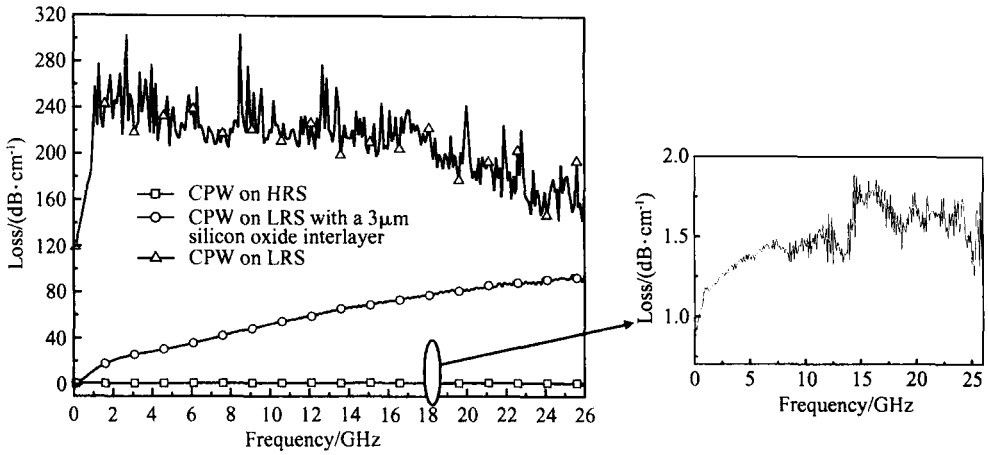

Fig. 4　Loss of the CPWs on HRS, LRS, and LRS with a 3μm interlayer

ed between the transmission lines and the LRS, because of its insulating character, the performance is improved greatly and the loss is reduced to less than 100dB/cm in the frequency range of 0～26GHz, but it is still too high for practical use. A thicker silicon oxide layer is needed, which means a longer oxidation time. Not only does this increase the cost, but a thick silicon oxide layer would be an obstacle for other processes. The CPWs on HRS show good performance because of the limit of measurements. They demonstrated a loss lower than 2dB/cm in the frequency range of 0～26GHz, which we predict will be still lower at higher frequencies. The HRS is therefore a more suitable low microwave loss substrate for CPWs.

5　Conclusion

In this paper, three kinds of CPWs were made on HRS substrate, standard LRS substrate, and LRS substrate with a silicon oxide interlayer. The results show that the LRS is unsuitable for high frequency coplanar waveguides because of the high microwave loss. Adding a silicon oxide interlayer between the coplanar waveguide transmission lines and the LRS substrate, the loss can be greatly reduced, but a thick silicon oxide layer is necessary, which will increase the cost and complicate other processes. The coplanar waveguide made directly on HRS has a very low loss at high frequencies, proving to be an effective way to obtain a high frequency and low loss coplanar waveguide.

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在高阻硅衬底上制备低微波损耗的共面波导*

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摘要: 分别在普通的低阻硅衬底、带有 3μm 厚氧化硅介质层的低阻硅衬底和高阻硅衬底上设计并制备了微波传输共面波导. 结果表明,低阻硅衬底导致过高的微波损耗从而不能使用,通过加氧化硅介质层,微波损耗可以大大减少,但是需要较厚的氧化硅厚度. 直接制备在高阻硅衬底上的共面波导在所测试的 26 GHz 的频率范围内获得低于 2dB/ cm 的微波损耗,而且工艺十分简单.

关键词: 共面波导; 高阻硅; 微波损耗; 高频; 光电子封装

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