# Monolithically Integrated Optoelectronic Receivers Implemented in 0.25μm MS/RF CMOS*

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**Abstract:** A monolithically integrated optoelectronic receiver is presented. A silicon-based photo-diode and receiver circuits are integrated on identical substrates in order to eliminate the parasitics induced by hybrid packaging. Implemented in the present deep sub-micron MS/RF (mixed signal, radio frequency) CMOS, this monolithically OEIC takes advantage of several new features to improve the performance of the photo-diode and eventually the whole OEIC.

**Key words:** monolithically integrated; OEIC; CMOS process
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## 1 Introduction

The demand for high volume data transmission in a short time in the present age of information has brought on a huge need for optical interconnection, which has been proven to be the best way to transmit data at extremely high speeds. Nowadays, the area of optoelectronic devices is dominated by compound semiconductor materials, due to their intrinsic characteristics. Since most transmitted data are processed on silicon chips, chips on different materials have to be packaged together to realize the whole optical interconnection system. Hybrid packaging either by wire bonding or by flip-chip bonding has introduced several undesired effects, which inevitably limit the utility and performance of the system. Because of the disadvantages mentioned above, the industry has been relentless in its quest to integrate the functions of optoelectronic systems onto a single chip. Monolithic integration on compound semiconductor substrate has been put into practical use for many years[1], but integration on silicon in general IC processes is preferred because of its low-cost and large-scale integration, especially in LAN (local area network) and VSR (very short reach) applications. The motivation and potential to realize such full integration in CMOS has increased markedly as the speed of CMOS circuits has made them viable candidates for Gbit rate data communication[2,3]. In this paper, we review the issues associated with fabricating photo-diodes in CMOS. Some new features offered by present MS/RF CMOS are employed to improve the performance of such photo-diodes. The front-end circuits of fiber communications are integrated with this novel photo-diode, including TIA's (trans-impedance amplifiers) and LA's (limiting amplifiers).

## 2 Design of photo-diodes in MS/RF CMOS

Fabricating a high performance photo-diode in CMOS is regarded as the bottleneck in realizing a monolithically integrated receiver, because the design technique of such an optoelectronic device is restricted to a narrow space not only by the optical properties of the material but also by the technology process. Fortunately, CMOS processes

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themselves are continually progressing. Many new features have been added to the basic process in order to expand the available functions. They can also be taken advantage of in the design of photo-diodes. In this section, we frame the problem by describing important features of the silicon materials and semiconductor process technologies as they relate to the problem of realizing photo-diodes.

The optical properties of silicon are well known. In particular, the absorption coefficient ($\alpha$) with a gradual onset owing to silicon's indirect bandgap structure is of primary importance. In contrast, the absorption onsets of direct bandgap materials are more abrupt. This unique feature causes the absorption length ($1/\alpha$) to vary significantly with wavelength, and to be much larger than that of direct bandgap materials for wavelengths in the vicinity of the bandgap. The photon absorption process creates electron-hole pairs in the bulk silicon; but only those generated in a region of electric field, or close enough to diffuse into the region, can contribute to the output photo-current. Otherwise, they will eventually recombine in the absence of an electric field. Compared with the field-aided drift component, diffusion-based carriers are transported at a much slower velocity, which will significantly affect the time-response of the photo-diode.

The basic photo-diode is a simple pn junction with a depletion region width W. For an incident optical power ($P_{opt}$), the photo-generated current ($I_g$) is related to the responsivity (R) by

$$I_g = RP_{opt} \tag{1}$$

$$R = \frac{I_g}{P_{opt}} = \eta \frac{q\lambda}{hc} \tag{2}$$

$$\eta = (1 - P_{ref})\, e^{-\alpha d} \left( 1 - \frac{e^{-\alpha W}}{1 + \alpha L} \right) \tag{3}$$

where $\eta$ is the external quantum efficiency, and L is the minority carrier diffusion length in the region with a relatively low doping rate. As described in Eqs. (1～3), L and $1/\alpha$ are characteristic lengths associated with photo-generated carriers. For W on the order of $1/\alpha$, most photo-generated carriers are collected by the electric field, and the diffusive component can be ignored. With the carriers drifting with the aid of the field, the photo-diode can operate at a very high speed. Unfortunately, the absorption length is about 14μm for a wavelength of 850nm, which is much deeper than the junction depth that can be achieved in a normal CMOS process. Therefore, the diffusive component will contribute a large part to the photo-generated current and will consequently introduce an undesired effect on the time-response of the photo-diode.

### 2.1 Double photo-diode in CMOS

As mentioned above, if the generated current purely contained drifting carriers, a better time-response would be attained. But unfortunately, CMOS processes are specialized for the fabrication of electric circuits. The source/drain implant process we usually use to make the photo-diode can only form a depletion region with a depth of about 5μm, for its high doping level of about $10^{16}$ $cm^{-3}$. Therefore, the time-response will be inevitably degraded by the slow transporting of the diffusive carriers generated in the bulk silicon. Methods for boosting the speed of CMOS compatible photo-diodes focus on how to eliminate these diffusive carriers. Such a method is illustrated in Fig. 1[4].

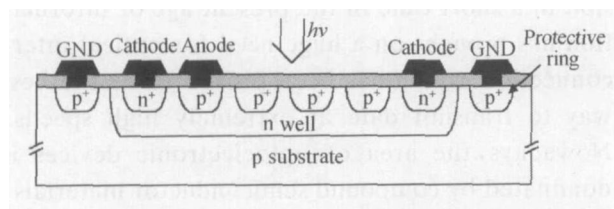


Fig. 1 Cross section of interdigitated photo-diode

As shown in Fig. 1, a photo-diode is implemented in a process identical to the formation of a p-type MOSFET. A $p^+$ region with an interdigitated lateral structure is designed as the anode of the photo-diode, which is originally implanted to form the source and drain of the MOSFET. An interdigitated structure is employed to broaden the depletion region, and makes as many of the photo-generated carriers as possible drifting. Another diode formed by an n-well and p-substrate also plays an important role in this structure. Called a screening diode, this diode prohibits the diffusive carriers generated in the bulk from contributing to the total generated current. This kind of screening scheme obviously trades responsivity for speed, because a large part of photo-generated carriers have been discarded. Fortunately, the degeneration of responsivity is not a serious problem in LAN and VSR applications, where the power

fade in the fiber is much less than in long-haul transmission applications.

### 2.2 Novel photo-diode implemented in MS/RF CMOS

Thanks to the rapid development of CMOS technology, we have many new ways to invent new photo-diodes. Having been predominant in digital circuit fabrication for many years, CMOS processes are attracting more and more attention in the area of MS/RF circuits. The deep-n-well is added to mitigate the influence of switching noise generated by digital circuits on the friable analog or RF part on the same chip. In conjunction with newly developed STI (shallow trench isolation) technology, this new feature can significantly improve the performance of CMOS-compatible photo-diodes. One example of novel structures based on MS/RF CMOS is given in Fig. 2, where a traditional DPD (double photo-diode) is surrounded by an STI circle and then buried in a deep-n-well.

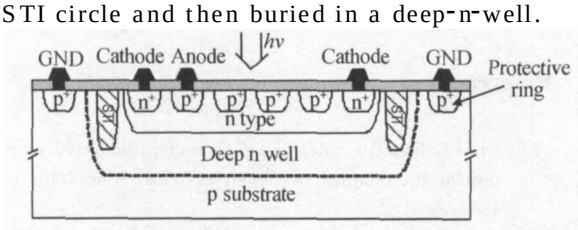


Fig. 2 Cross section of novel photo-diode in MS/RF CMOS

Compared with conventional DPDs, this novel structure has improvements in many aspects[5].

(1) Dark current: Some dark current is inevitable because it is impossible to get a perfectly defect-free silicon substrate. However, the dark current can be mitigated by isolating the laterally diffusive random carriers. Through the use of STI and the deep-n-well, the magnitude of the dark current is only about 1/5 of that in DPDs without these new features.

(2) Responsivity: Poor responsivity has been regarded as the main shortcoming of DPDs. It can be enhanced when an STI wall is introduced, since the photo-generated carriers are restricted inside the circle, where they can be efficiently used. The experiment has shown that the responsivity of the novel structure is 0.066A/W, compared to only 0.017A/W in conventional DPDs[5].

On the other hand, the concentration index variation in the n-well will increase the photo-diode capacitance, which may degenerate the bandwidth of the receiver circuit.

## 3 Receiver circuit design

The front-end of an optical receiver circuit usually consists of a TIA and an LA.

A regulated cascode (RGC) configuration is employed to realize the TIA. It has been proved that RGC can more effectively isolate the photo-diode capacitance from the bandwidth determination than other structures[6]. As shown in Fig. 3 (a), M1 and M2 make up the RGC input stage, significantly enhancing the input $g_m$, and consequently pulling the pole decided by the photo-diode capacitance and the input impedance out of dominance. The feedback resistor $R_f$ is applied from the output stage (M4) to the drain of M1, which not only boosts the output $g_m$ but also efficiently buffers the current at the input.

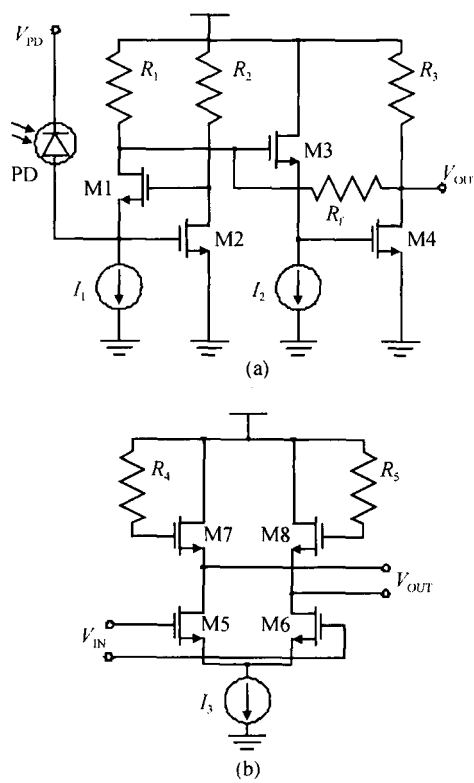


Fig. 3 (a) Schematic diagram of an RGC TIA; (b) Schematic diagram of one stage of an LA

The LA consists of an input stage, a gain stage and an output buffer. The gain stage is composed of 6 serially connected differential ampli-

fiers, one of which is given in Fig. 3 (b). All these differential amplifiers are loaded by active inductors consisting of an n-MOSFET operating in saturation plus a gate resistor, in order to broaden the bandwidth.

## 4 Chip design and measurement results

A monolithically integrated optoelectronic receiver is implemented in TSMC 0.25μm MS/RF CMOS technology. A chip photograph is shown in Fig. 4. The photo-diode is designed with an octagonal lateral configuration, which introduces less capacitance than a square one.

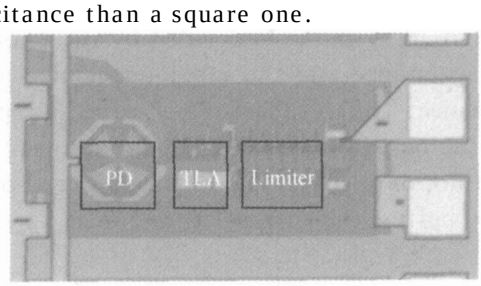


Fig. 4 A monolithically integrated optoelectronic receiver

The OEIC was tested with a sinusoidal modulated optical input with an incident power of 600μW at a wavelength of 850nm. The measured transient response is shown in Fig. 5. An amplitude of nearly 20mV is achieved at the output of the OEIC, which means that a trans-impedance of about 56dB ·Ω is attained by the front-end circuits.

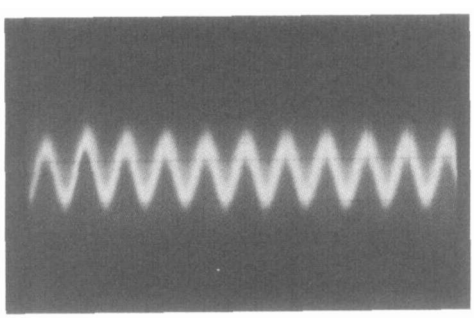

Fig. 5 Transient response of the OEIC at 150MHz

Figure 6 shows the frequency response of the monolithic optical receiver. Only a 400MHz 3dB-bandwidth has been achieved. The degeneration of the bandwidth can be attributed to the increment of the photo-diode capacitance. More effort should be devoted to the design of the TIA circuit in future work.

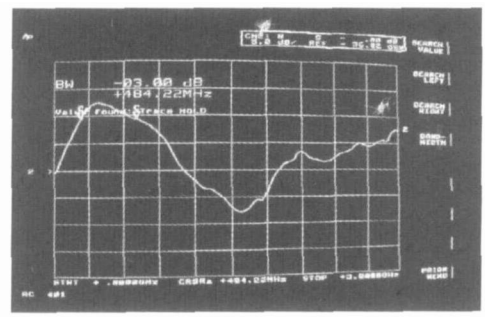


Fig. 6 Frequency response of the OEIC

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# 基于 0.25μm MS/RF CMOS 工艺的光电单片集成接收机设计*

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**摘要**：设计了一种单片集成的光电接收机芯片.在同一衬底上制作了基于同一工艺的光电二极管与接收机电路，以消除混合集成引入的寄生影响.这种单片集成接收机采用了先进的深亚微米 MS/RF(混合信号/射频) CMOS 工艺，利用这种新型工艺提供的新技术对原有光电二极管进行了改进，使其部分性能显著改善，并对整个光电集成芯片性能的提高有所帮助.

**关键词**：单片集成；光电集成电路；CMOS 工艺

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