A High Performance Sub-100nm Nitride/Oxynitride Stack Gate Dielectric CMOS Device with Refractory W/TiN Metal Gates

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Abstract: By complementing the equivalent oxide thickness (EOT) of a 1.7nm nitride/oxynitride (N/O) stack gate dielectric (EOT = 1.7nm) with a W/TiN metal gate electrode, metal gate CMOS devices with sub-100nm gate length are fabricated in China for the first time. The key technologies adopted to restrain SCE and to improve drive ability include a 1.7nm N/O stack gate dielectric, non-CMP planarization technology, a T-type refractory W/TiN metal stack gate electrode, and a novel super steep retrograde channel doping using heavy ion implantation and a double sidewall scheme. Using these optimized key technologies, high performance 95nm metal gate CMOS devices with excellent SCE and good driving ability are fabricated. Under power supply voltages of $V_{DS} = \pm 1.5$V and $V_{GS} = \pm 1.8$V, drive currents of 679μA/μm for nMOS and -327μA/μm for pMOS are obtained. A subthreshold slope of 84.46mV/dec, DIBL of 34.76mV/V, and V_{th} of 0.26V for nMOS, and a subthreshold slope of 107.4mV/dec, DIBL of 54.46mV/V, and V_{th} of -0.27V for pMOS are achieved. These results show that the combined technology has indeed thoroughly eliminated the boron penetration phenomenon and polysilicon depletion effect, effectively reduced gate tunneling leakage, and improved device reliability.

Key words: equivalent oxide thickness; nitride/oxynitride gate dielectric stack; W/TiN metal gate; non-CMP planarization

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1 Introduction

The down scaling of polysilicon gate lengths below 100nm and of the EOT of gate oxides below 2nm has led to a series of difficulties, including excessive direct tunneling current, a strong tendency for boron penetration, the poly gate depletion effect, and quantum mechanical effects[1~4]. Adopting Si_3N_4/SiO_2 (N/O) stack material as a gate dielectric combined with an improved sputtered tungsten/titanium nitride (W/TiN) gate electrode is one way to overcome these challenges. A high *k* gate dielectric can increase the thickness of the gate dielectric, thus reducing the gate tunneling leakage current and suppressing the boron penetration phenomenon[5]. In addition, an optimized sputtered W/TiN stack, as a refractory metal gate electrode, exhibits a lot of advantages, such as the elimination of poly-Si depletion and boron penetration, a great decrease in gate resistance, and high process compatibility. W/TiN, a mid-bandgap material, can be used as a gate material to fabricate both nMOS and pMOS[6]. A N/O stack dielectric with metal gate CMOS devices can be fabricated using a damascene gate process in which the processing temperature after sputtering the W/TiN metal gate can be lowered to below 450 ℃. In this paper, the characteristics of a N/O stack gate dielectric with a W/TiN gate electrode are analyzed in detailed. Experiments show that the 95nm-gate-length metal gate devices with N/O stack gate dielectric have excellent electrical properties.

2 Structure of 95nm CMOS device

A cross-section of the 95nm CMOS device with N/O stack gate dielectric and W/TiN metal gate electrode is shown in Fig. 1. The main features are as follows: (1) 1.7nm N/O stack gate dielectric with high reliability; (2) T-shape W/TiN stack metal gate electrode; (3) super-steep retrograde (SSR) channel doping profile[7]; (4) double sidewall scheme[7]. An SEM microphotograph of the

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dummy gate of the 95nm CMOS device with N/O stack gate dielectric and W/TiN metal gate electrode is shown in Fig. 2.

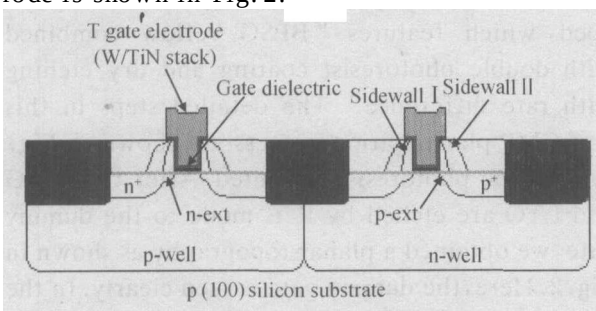

Fig. 1　Schematic of 95nm CMOS device with N/O stack gate dielectric and W/TiN metal gate

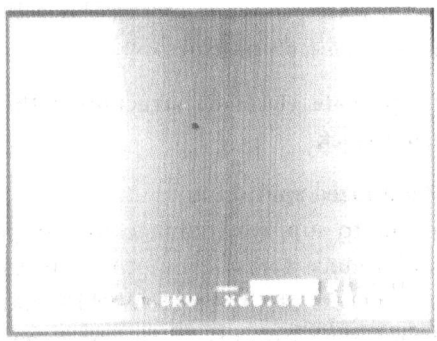

Fig. 2　SEM topograph of the dummy gate of CMOS device after planarization　The length of the dummy gate exposed is 75nm.

3　Investigation of key process

A local oxidation of a silicon (LOCOS) isolated 95nm CMOS metal gate device was fabricated as shown schematically in Fig. 1. The key process technologies are described as follows.

3.1　EOT of 1.7nm N/O stack gate dielectric[8]

To overcome the previously mentioned challenges, the adoption of oxynitride and high *k* material as gate dielectric has been reported by many authors. In our experiment, we adopt a combination of thermal oxynitride and LPCVD Si_3N_4 to fabricate ultra thin N/O stack dielectrics. The bottom oxynitride film (0.7～0.8nm) was formed by oxidation of N^+ implanted silicon substrate at 670 ℃ in N_2. Ultra thin Si_3N_4 films (1.2～1.6nm) were deposited using LPCVD deposition by SiH_2Cl_2 and NH_3 at a ratio of $SiH_2Cl_2/NH_3 = 1/6$ at 715 ℃ and a chamber pressure of 36.66Pa. The reasons that the oxynitride was grown on N-implanted silicon for N/O stack gate dielectric are as follows: First, the oxidation retardation effect greatly reduces the oxidation rate, making the oxynitride more dense and uniform, and resulting in a finer interface between the silicon and oxynitride[9]; Second, the introduction of N into the oxide films can be regarded as knitting up the broken chemical bonds, such as dangling bonds (O3 ≡Si ·) and oxygen vacancy bonds (≡Si · ·Si≡), to form a relatively strong Si-N bond structure to improve the interface characteristics[10]. Finally, LPCVD Si_3N_4 which has a higher dielectric constant and increases the physical oxide thickness, can also contribute to a lower gate leakage current and stronger resistance to boron penetration.

The $I_G - V_{OX}$ ($V_{OX} = V_G - V_{fb}$) curves for both p^+-gate/n-sub pMOS capacitors and W/TiN/n-sub pMOS capacitors with various EOT of stack N/O under the electron-accumulation conditions are shown in Fig. 3, and are compared with that for pure oxide. It can be clearly seen that when the EOT of the capacitors is reduced to the region where (direct tunneling DT) dominates, the N/O stack gate dielectric of 1.9nm with a poly gate shows a lower leakage current than thermal oxide with an EOT of 2.0nm by several orders of magnitude, while the N/O stack films of 1.7nm with a W/TiN gate shows more than one order of magnitude lower leakage current at lower fields. The reasons have already been mentioned above.

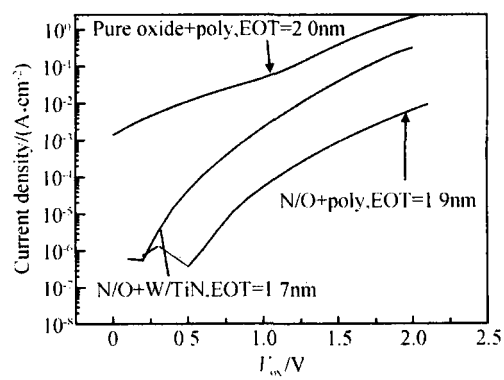

Fig. 3　Gate tunneling leakage density versus V_{ox} of pMOS capacitors with different gate dielectrics and different gate electrode materials under electron accumulation condition[7]

From Table 1, it can be seen that the samples of N/O stack gate dielectric show a much lower flatband voltage than that of pure oxide, which in-

dicates that the N/O stack layer greatly suppresses boron penetration due to the obstruction of the N/O stack layer and the higher N located in the oxynitride layer. And it should also be noted that the lower flatband voltage as shown in Table 1 and higher capacitance as shown in Ref. [8] indicate that the gate depletion effects and the boron penetration phenomenon are completely eliminated in the metal gate pMOS capacitor. The reason is that there is no introduction of boron ions in the metal gate material, which is responsible for inducing poly-Si depletion and boron penetration.

Table 1 Capacitor and flatband voltages[7]

Capacitor	Dose of BF_2 implantation/ cm^{-3}	RTA time/ s, temperature/ °C	Flatband voltage/ V
N/O stack with poly gate (EOT = 1.9nm)	1.5×10^{15}/ 2.0×10^{15}	4/8/16, 1005	0.723/0.734/ 0.761
N/O stack with W/TiN gate (EOT = 1.7nm)	—	—	0.105
Pure oxide with poly gate (EOT = 2.0nm)	1.5×10^{15}	4, 1005	1.31

Figure 4 gives the 10 year lifetime projection of N/O stack gate dielectric poly gate capacitors and N/O stack gate dielectric metal gate capacitors. The 10 year lifetime projected for such capacitors is at V_g = 2.7V (metal gate, EOT = 1.7nm) and V_g = 2.4V (poly gate, EOT = 1.9nm). The reason is that the metal gate electrode has completely eliminated boron penetration and poly-Si depletion, effectively reducing the trap density in the gate dielectrics.

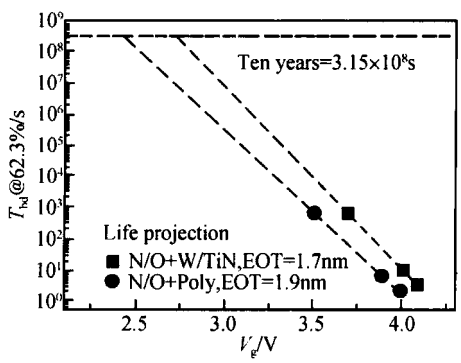

Fig. 4 Lifetime projection for the poly gate electrode and metal gate electrode capacitors

3.2 Non-CMP planarization

In order to make use of damascene technology to fabricate refractory metal gate electrode CMOS devices, a flat wafer surface is required[11]. CMP planarization is widely used, but it is expensive and requires special equipment. In our experiment, a non-CMP planarization process is developed, which features "BPSG reflow combined with double photoresist coating and dry etching with rate difference". The detailed steps in this non-CMP planarization process are shown in Fig. 5. Here the photoresist is diluted. After the BPSG and LTO are etched by RIE mode to the dummy gate, we obtained a planar topography as shown in Fig. 2. Here, the dummy gate is seen clearly. In the end, after the removing the dummy gate (Si_3N_4) by wet etching in hot H_3PO_4 solution, the depth of the gate groove is about 130nm. In addition, the length of the gate groove is spread about 20nm because of the wet etching isotropy.

3.3 T-type gate electrode structure with W/TiN metal stack

3.3.1 Optimized sputtering

In order to suppress damage to the gate dielectric and reduce stress from the interface, the sputtering process of the stack W/TiN metal gate electrode must be optimized. In our experiment, we reactively sputtered the bottom TiN using an $Ar + N_2$ gas mixture followed by metal W deposition in the Ar ambient. The optimized sputtering process is described in a previous paper[12]; its main points are as follows: (1) reduce the RF power to obtain a smaller sputtering rate and properly increase the ratio of the N/Ar in case of sputtering TiN to reduce the sputtering energy so as to restrain damage to the gate dielectric; (2) select proper TiN thickness in W/TiN stack structure to alleviate interface stress; (3) properly increase post anneal temperature to further eliminate damage. Table 2 gives the optimized sputtering condition used. The optimized thickness of TiN and W are 35 and 100nm respectively. With these optimized sputtering conditions, interface state charges N_{ss} can be kept below 10^{11} cm^{-2}.

Table 2 Optimized sputtering condition

RF power/ W	N_2/ Ar	Base vacuum/ Pa	Working pressure/ Pa
800	0.256	1.067×10^{-4}	0.533

3.3.2 T-type gate electrode

After the formation of the ultra thin N/O stack dielectric followed by the sputtering of the

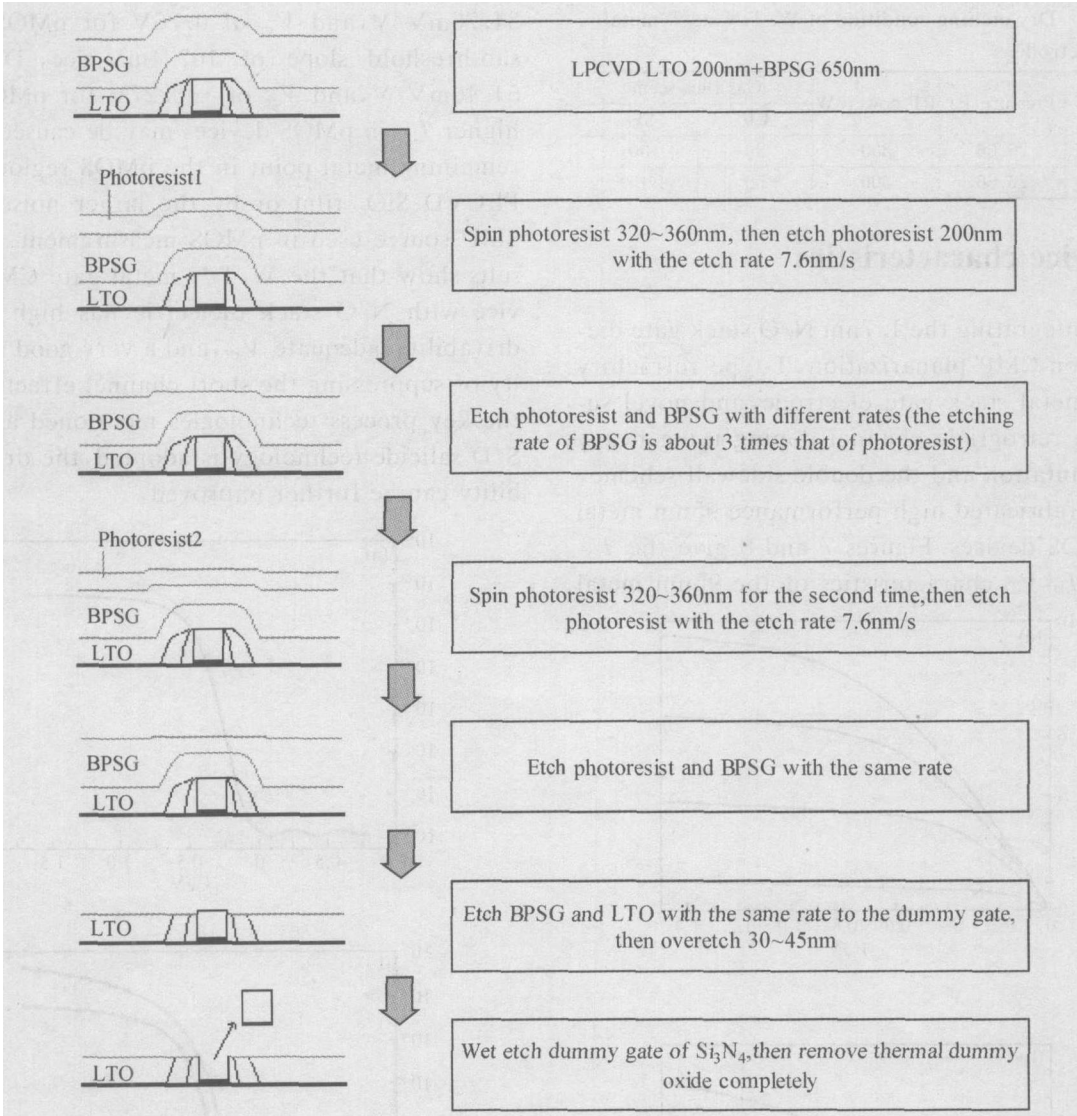

Fig. 5　Process steps of non-CMP planarization

refractory W/ TiN metal gate electrode, relevant photolithography and etching steps should be taken to form the T-type gate electrode structure shown in Fig. 6.

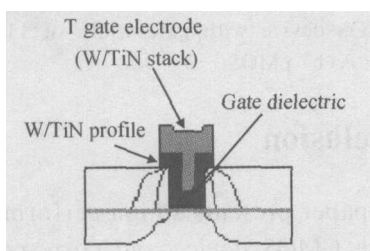

Fig. 6　Schematic of T-type gate metal gate CMOS device

The matching error between the system of electron beam lithography and stepper lithography was also taken into account in the design of the layout of T-type gate. The dry etching process after the T-type gate lithography is of great importance in fabricating the T-type gate electrode. In order to obtain a strictly continuous and smooth profile of W/ TiN, the W and TiN etching rate must be nearly constant in the main etching step. The corresponding etching condition is shown in Table 3. In this work, the etching is performed in a LAM Rainbow 4420. The main etching is accomplished in a gas mixture of Cl_2/ SF_6 with just the LTO exposed. The overetch is begun as soon as possible under the condition shown in Table 3 to completely remove the W/ TiN and get a higher etching selectivity to the LTO.

Table 3 Dry etching condition of W/ TiN stack metal gate electrode

Etch step	Pressure/ Pa	RF power/ W	Gas flux/ sccm	
			Cl_2	SF_6
Main etch	26.66	300	30	30
Over etch	26.66	300	50	10

4 Device characteristics

By integrating the 1.7nm N/O stack gate dielectric, non-CMP planarization, T-type refractory W/ TiN metal stack gate electrode, and novel super steep retrograde channel doping using heavy ion implantation and the double sidewall scheme, we have fabricated high performance 95nm metal gate CMOS devices. Figures 7 and 8 give the I_D-V_D and I_D-V_G characteristics of the 95nm metal gate CMOS

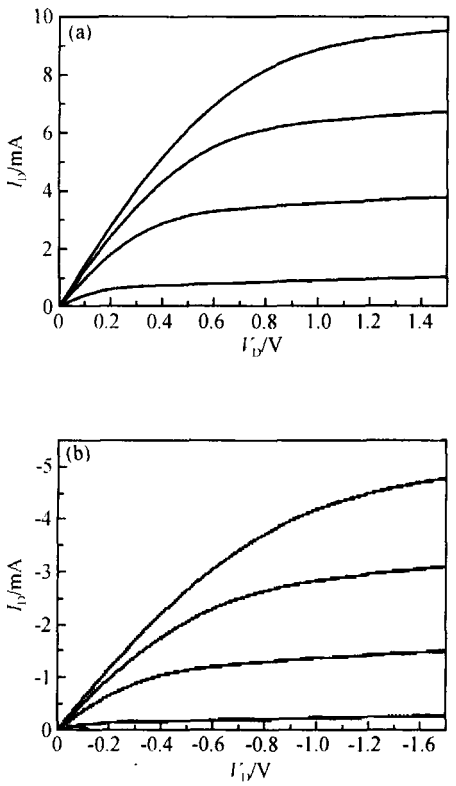

Fig. 7 I_D-V_D curves of 95nm metal gate CMOS device with gate width of 14μm (a) nMOS(+); (b) pMOS(-)

device with N/O stack dielectric respectively. It can be seen that the subthreshold and output characteristics are very good. At V_{DS} = ±1.5V and V_{GS} = ±1.8V, the measured saturation driving currents are 679μA/μm for nMOS and -327μA/μm for pMOS. From Fig. 7, we see a subthreshhold slope of 84.46mV/dec, DIBL of 34.76mV/V, and V_{th} of 0.26V for nMOS and a subthreshold slope of 107.4mV/dec, DIBL of 54.46mV/V, and V_{th} of -0.27V for pMOS. The higher I_{off} in pMOS devices may be caused by the remaining metal point in the pMOS region in the PECVD SiO_2 film or by the larger noise in the SMU source used in pMOS measurement. The results show that the W/ TiN metal gate CMOS device with N/O stack dielectric has high current drivability, adequate V_{th}, and a very good capability of suppressing the short channel effects due to the key process technologies mentioned above. If S/D salicide technology is adopted, the driving ability can be further improved.

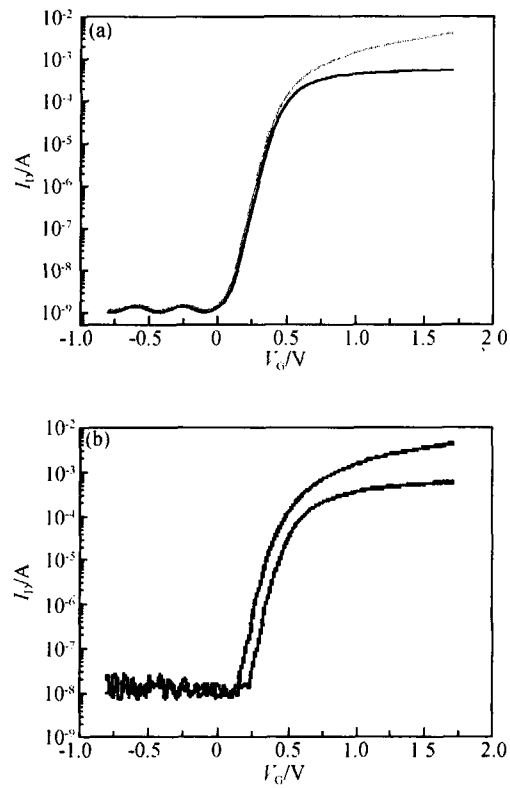

Fig. 8 Subthreshold characteristics of 95nm metal gate CMOS device with gate width of 14μm (a) nMOS (+); (b) pMOS(-)

5 Conclusion

This paper presents a high performance 95nm metal gate CMOS device and corresponding key technologies, which include a 1.7nm N/O stack gate dielectric, non-CMP planarization, a T-type refractory W/ TiN metal stack gate electrode, and novel super steep retrograde channel doping using heavy ion implantation and a double sidewall

scheme. The fabricated device effectively suppresses the SCE and has good driving ability and adequate threshold voltage. Experimental results show that these technologies are controllable and repeatable and will be candidates for the next generation of metal gate CMOS FETs.

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高性能亚 100nm 栅长氮氧叠层栅介质难熔 W/TiN 金属栅电极 CMOS 器件

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摘要: 在国内首次将等效氧化层厚度为 1.7nm 的 N/O 叠层栅介质技术与 W/TiN 金属栅电极技术结合起来,用于栅长为亚 100nm 的金属栅 CMOS 器件的制备. 为抑制短沟道效应并提高器件驱动能力,采用的关键技术主要包括:1.7nm N/O 叠层栅介质,非 CMP 平坦化技术,T 型难熔 W/TiN 金属叠层栅电极,新型重离子超陡倒掺杂沟道剖面技术以及双侧墙技术. 成功地制备了具有良好的短沟道效应抑制能力和驱动能力的栅长为 95nm 的金属栅 CMOS 器件. 在 V_{DS} = ±1.5V, V_{GS} = ±1.8V 下, nMOS 和 pMOS 的饱和驱动电流分别为 679 和 - 327μA/μm. nMOS 的亚阈值斜率, DIBL 因子以及阈值电压分别为 84.46mV/dec, 34.76mV/V 和 0.26V. pMOS 的亚阈值斜率, DIBL 因子以及阈值电压分别为 107.4mV/dec, 54.46mV/V 和 0.27V. 结果表明,这种结合技术可以完全消除 B 穿透现象和多晶硅耗尽效应,有效地降低栅隧穿漏电并提高器件可靠性.

关键词: 等效氧化层厚度; 氮氧叠层栅介质; W/TiN 金属栅; 非 CMP 平坦化

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