Low Voltage Flash Memory Cells Using SiGe Quantum Dots for Enhancing F-N Tunneling *

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Abstract: A novel flash memory cell with stacked structure (Si substrate/SiGe quantum dots/tunneling oxide/poly-Si floating gate) is proposed and demonstrated to achieve enhanced F-N tunneling for both programming and erasing. Simulation results indicate the new structure provides high speed and reliability. Experimental results show that the operation voltage can be as much as 4V less than that of conventional full F-N tunneling NAND memory cells. Memory cells with the proposed structure can achieve higher speed, lower voltage, and higher reliability.

Key words: flash memory; SiGe quantum dots; enhanced F-N tunneling
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1 Introduction

Although flash memory technology is highly developed, it faces critical challenges in achieving high speed and high density for the next generation. High-k dielectrics and novel program/erase mechanisms and structures have been studied for high density flash memory[1~3]. The main problem for high density memory is the relatively high operation voltage, which results in the necessity of a thick tunneling oxide and a complicated external high voltage circuit[4~6]. The tradeoff between high speed and reliability makes further down-scaling difficult.

F-N tunneling is an effective tunneling mechanism, but it requires a high voltage (~18V) which is not favorable for high density memory. Several years ago, a texture-like poly-dioxide film was proposed for enhancing F-N tunneling[7]. This reduced the operation voltage[8], but the quality of this kind of tunneling layer is too poor for use in real commercial devices[9].

Here we demonstrate a novel Si substrate/SiGe quantum dots/tunneling oxide/poly-Si floating gate stacked structure (flat or with self-aligned tips) for achieving enhanced F-N tunneling for both programming and erasing. Theoretically, higher speed, lower voltage, and higher reliability can be expected for memory cells with the proposed structure. Both simulation and experimental results show that the operation voltage can be as much as 4V less than that of conventional full F-N tunneling NAND memory cells.

2 Device structure and principles

Figure 1 shows schematics of a memory cell with the conventional structure and two cells with the new structure. Structure A is a standard flash memory cell. In structures B and C, SiGe quantum dots are fabricated directly on Si substrate with a UHV/CVD system to achieve enhanced F-N tunneling programming. The size and shape of the dots are controlled by growth parameters such as temperature, duration, and gas flux.

As shown in Fig. 1, structure A is a conventional full F-N tunneling NAND memory cell. In contrast to the flat floating gate in structure B, the poly-Si floating gate with self-aligned tips (structure C) is designed to achieve F-N tunneling for erasing and programming.

The fabrication process of the poly-Si floating gate with self-aligned tips is shown in Fig. 2. The Si film after the growth of SiGe dots (step 2) is designed to form a tunneling oxide layer. The oxida-

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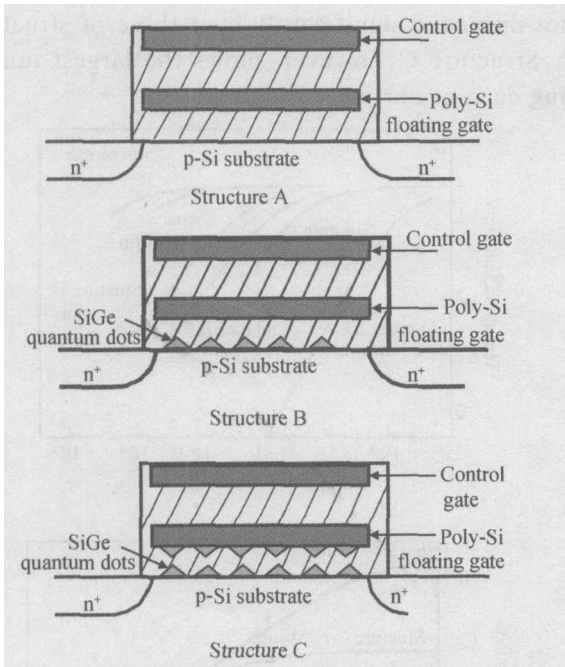

Fig. 1 Schematic structure of conventional full F-N memory cell (A) and the two proposed enhanced F-N tunneling memory cells (B and C)

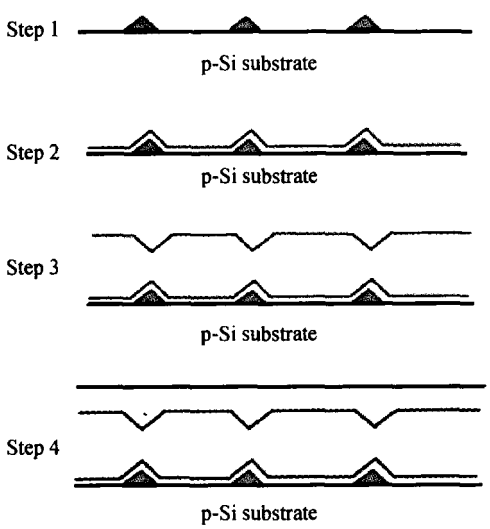

Fig. 2 Fabrication process of poly-Si floating gate with self aligned tips Step 1 : self-assembled SiGe dots ; Step 2 : Si films epitaxy ; Step 3 : oxidation ; Step 4 : poly-Si deposition

tion rate of the SiGe quantum dots is much lower than that of Si substrate so that after the Si film is consumed, faster oxidation of Si substrate around the quantum dots results in a tunneling oxide with self-aligned pits on the surface (step 3). Then the self-aligned floating gate tips are deposited using these pits as moulds. Step 3 is the most important process for fabricating a floating gate with self-aligned tips. For a flat poly-Si floating gate, the Si concentration in the dots and the thickness of the tunneling oxide should be carefully designed to obtain a tunneling oxide without pits.

The electric field between the SiGe quantum dots and floating gate was calculated in ANSYS. Figure 3 shows the local electrical field for structures B and C. For both structures, the local electric field near the SiGe quantum dots is significantly enhanced because of the F-N tunneling geometrical enhancement factor of the quantum dots. As indicated, the local field near the self-aligned tips in structure C is enhanced, and thus the tunneling current can be improved for erasing and programming.

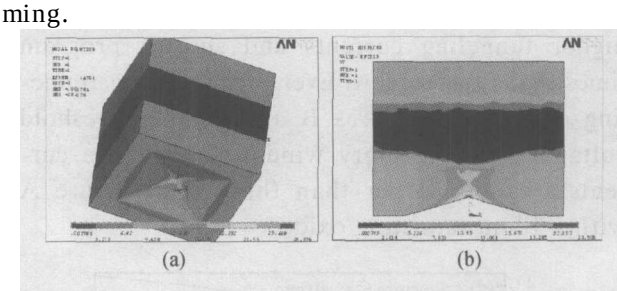

Fig. 3 Local electrical field (a) Structure B; (b) Structure C

The energy band diagrams for structures B and C are shown in Fig. 4. Bidirectional barriers for both programming (injecting electrons from the channel to the floating gate) and erasing (drawing electrons out of the floating gate) faced by electrons in structure C are effectively nar-

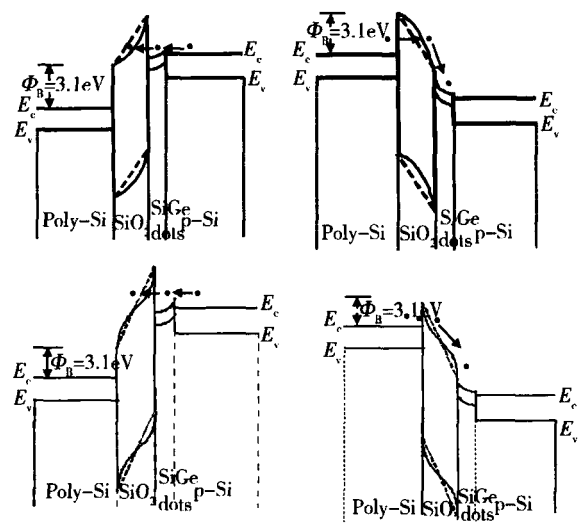

Fig. 4 Energy band diagrams of sturcture B (top) and C (bottom) Left for programming; right for erasing

rowed, and thus bidirectional F-N tunneling can be significantly enhanced. In structure B, however, only the barrier for programming is lowered, so F-N tunneling for erasing cannot be enhanced (actually, the local electric field near the flat floating gate is even slightly weaker than in structure A).

3 Results and discussion

Figure 5 shows the simulated threshold voltage shift and gate current during programming operations for the three structures (assuming only one Si Ge quantum dot in the channel for structures B and C, a gate voltage of 16V, and a tunneling area of 30nm ×30nm, which is much smaller than in real devices). Structures B and C yield higher tunneling currents and shorter program times than structure A. Even with a 14nm tunneling oxide in structures B and C, the threshold voltage shifts (memory windows) and gate currents are both larger than those of structure A with a 10nm tunneling oxide.

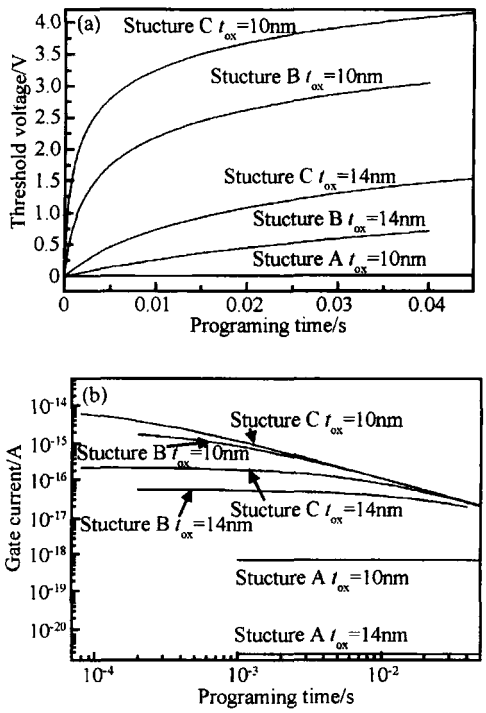

Fig. 5 Threshold voltage (a) and gate current (b) during programming processes Tunneling oxide thickness t_{ox} = 10, 14nm

Figure 6 shows the corresponding results for erasing operations. As expected, the threshold voltage and tunneling current of structure B are not improved significantly over those of structure A. Structure C, however, shows the largest tunneling current during erasing.

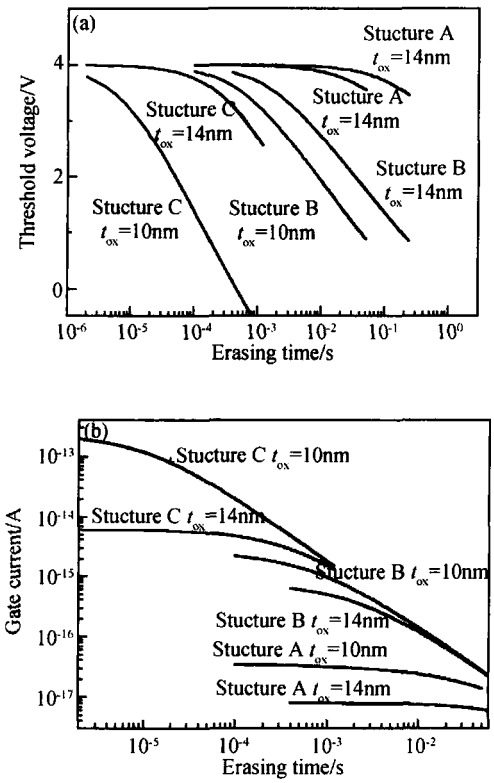

Fig. 6 Threshold voltage (a) and gate current (b) during erasing Tunneling oxide thickness t_{ox} = 10, 14nm

As shown in Fig. 7, the memory cells with a 10nm tunneling oxide with structures B and C show a larger threshold shift than conventional cells under relatively low control gate voltages. By extrapolation, V_{CG} can be reduced by about 4V without sacrificing the programming/erasing speed of the conventional structure.

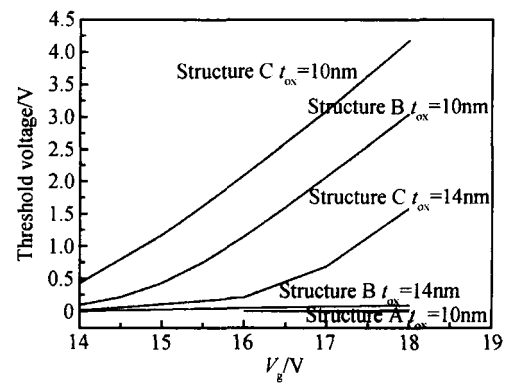

Fig. 7 Threshold voltage dependence on control gate voltage for the three structures Tunneling oxide thickness t_{ox} = 10, 14nm

For comparison, samples with the three structures (Fig. 1.) were fabricated with standard 0.8μm CMOS technology, and the tunneling current was measured. The measured gate currents of the three samples for both programming and erasing are shown in Fig. 8. They show the same trends observed in the simulation. The gate current during programming in samples B and C is more than 10^3 times better than that of sample A under a gate voltage of 12V. During erasing, only the gate current in sample C is improved significantly over sample A. This demonstrates the effectiveness of a floating gate with tips in enhancing F-N tunneling during erasing.

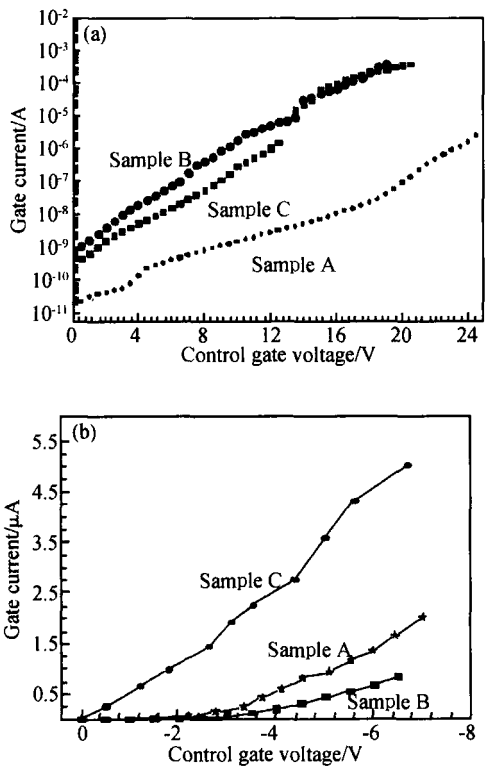

Fig. 8 Experimental results of gate current during programming (a) and erasing (b) for three structures

Finally, we explain how structure C improves reliability during programming and erasing. Because the mean electric field in the tunneling oxide is reduced by the enhanced F-N tunneling mechanism (for the same order of programming and erasing current), the strain induced by the local high electric field can be partially relaxed in the surrounding tunneling oxide, where the electric field is lower.

Furthermore, since a thicker tunneling oxide than in the conventional structure can be used with no loss of speed, the strain-induced leakage current (SILC) can be further reduced.

4 Summary

In summary, we propose two new structures for flash memory cells with the enhanced F-N tunneling effect of SiGe quantum dots and self-aligned tips of the floating gate. The two structures for full F-N programming/erasing show higher speed and lower operation voltage than the conventional structure without reducing the tunneling oxide thickness. Because of the low mean electric field in the tunneling oxide, higher reliability can be achieved for further scaling-down of the next generation flash memory.

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基于 SiGe 量子点实现增强 F-N 隧穿的低压闪速存储器 *

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摘要：提出了一种用于半导体闪速存储器单元的新的 Si/SiGe 量子点/隧穿氧化层/多晶硅栅多层结构，该结构可以实现增强 F-N 隧穿的编程和擦除机制. 模拟结果表明该结构具有高速和高可靠性的优点. 测试结果表明该结构的工作电压比传统 NAND 结构的存储器单元降低了 4V. 采用该结构能够实现高速、低功耗和高可靠性的半导体闪速存储器.

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